



128Kx32 SRAM/FLASH MODULE

PRELIMINARY*

FEATURES

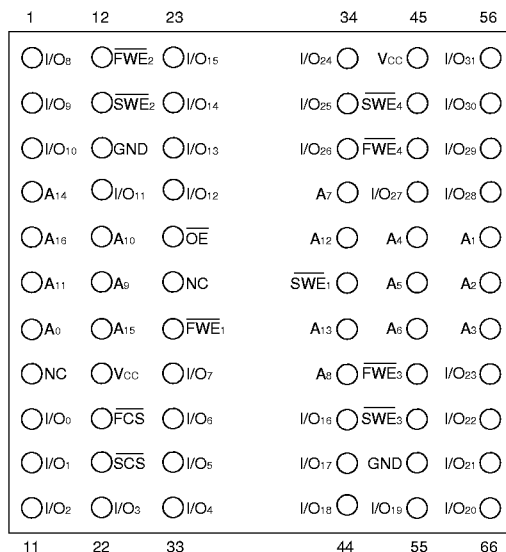
- Access Times of 25ns (SRAM) and 120ns (FLASH)
- Access Times of 25ns (SRAM) and 90ns (FLASH)
- Packaging:
 - 66-pin, PGA Type, 1.385 inch square HIP, Hermetic Ceramic HIP (Package 402)
- 128Kx32 SRAM
- 128Kx32 5V Flash
- Organized as 128Kx32 of SRAM and 128Kx32 of Flash Memory with common Data Bus
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 13 grams typical

FLASH MEMORY FEATURES

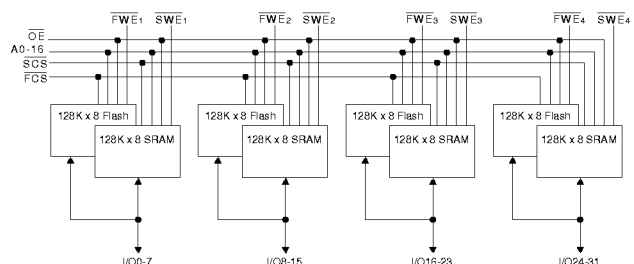
- 10,000 Erase/Program Cycles
- Sector Architecture
 - 8 equal size sectors of 16K bytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V $\pm$ 10% Supply
- Embedded Erase and Program Algorithms
- Hardware and Software Write Protection
- Page Program Operation and Internal Program Control Time.

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WSF128K32-XH2X**TOP VIEW****PIN DESCRIPTION**

D0-31	Data Inputs/Outputs
A0-16	Address Inputs
SWE1-4	SRAM Write Enables
SCS	SRAM Chip Select
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected
FWE1-4	Flash Write Enables
FCS	Flash Chip Select

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _I	-0.5	7.0	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

Parameter	
Flash Data Retention	10 years
Flash Endurance (write/erase cycles)	10,000

NOTE:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V

SRAM TRUTH TABLE

$\overline{\text{SCS}}$	$\overline{\text{OE}}$	$\overline{\text{SWE}}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

NOTE:

- $\overline{\text{FCS}}$ must remain high when $\overline{\text{SCS}}$ is low.

CAPACITANCE

(T_A = +25°C)

Test	Symbol	Condition	Max	Unit
$\overline{\text{OE}}$ Capacitance	C _{OE}	V _{IN} = 0V, f = 1.0MHz	80	pF
F/S $\overline{\text{WE}}$ 1-4 Capacitance	C _{WE}	V _{IN} = 0V, f = 1.0MHz	30	pF
F/S $\overline{\text{CS}}$ Capacitance	C _{CS}	V _{IN} = 0V, f = 1.0MHz	50	pF
D0-31 Capacitance	C _{I/O}	V _{IN} = 0V, f = 1.0MHz	30	pF
A0 - A16 Capacitance	C _{AD}	V _{IN} = 0V, f = 1.0MHz	80	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{\text{SCS}}$ = V _{IH} , $\overline{\text{OE}}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
SRAM Operating Supply Current x 32 Mode	I _{CCx32}	$\overline{\text{SCS}}$ = V _{IL} , $\overline{\text{OE}}$ = $\overline{\text{FCS}}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		670	mA
Standby Current	I _{SB}	$\overline{\text{FCS}}$ = $\overline{\text{SCS}}$ = V _{IH} , $\overline{\text{OE}}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		80	mA
SRAM Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4	V
SRAM Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4		V
Flash V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{\text{FCS}}$ = V _{IL} , $\overline{\text{OE}}$ = $\overline{\text{SCS}}$ = V _{IH}		220	mA
Flash V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\overline{\text{FCS}}$ = V _{IL} , $\overline{\text{OE}}$ = $\overline{\text{SCS}}$ = V _{IH}		280	mA
Flash Output Low Voltage	V _{OL}	I _{OL} = 12.0mA, V _{CC} = 4.5		0.45	V
Flash Output High Voltage	V _{OH1}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		V
Flash Output High Voltage	V _{OH2}	I _{OH} = -100 μA, V _{CC} = 4.5	V _{CC} - 0.4		V
Flash Low V _{CC} Lock Out Voltage	V _{LKO}		3.2		V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{\text{OE}}$ at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



SRAM AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-25		Unit
		Min	Max	
Read Cycle Time	t _{RC}	25		ns
Address Access Time	t _{AA}		25	ns
Output Hold from Address Change	t _{OH}	0		ns
Chip Select Access Time	t _{ACS}		25	ns
Output Enable to Output Valid	t _{OE}		15	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		12	ns
Output Disable to Output in High Z	t _{OHZ} ¹		12	ns

1. This parameter is guaranteed by design but not tested.

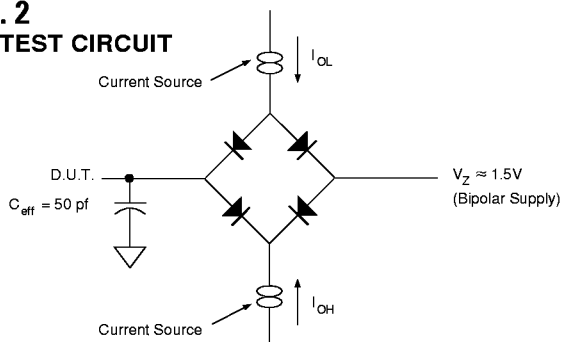
SRAM AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-25		Unit
		Min	Max	
Write Cycle Time	t _{WC}	25		ns
Chip Select to End of Write	t _{OW}	20		ns
Address Valid to End of Write	t _{AW}	20		ns
Data Valid to End of Write	t _{DW}	15		ns
Write Pulse Width	t _{WP}	20		ns
Address Setup Time	t _{AS}	0		ns
Address Hold Time	t _{AH}	0		ns
Output Active from End of Write	t _{OW} ¹	3		ns
Write Enable to Output in High Z	t _{WHZ} ¹		15	ns
Data Hold from Write Time	t _{DH}	0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

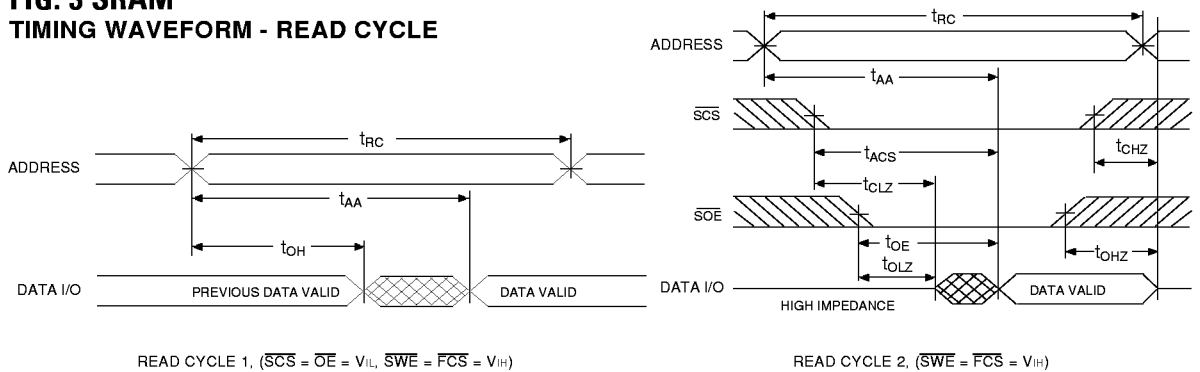
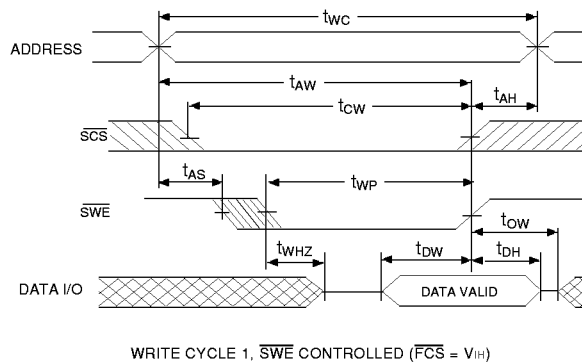
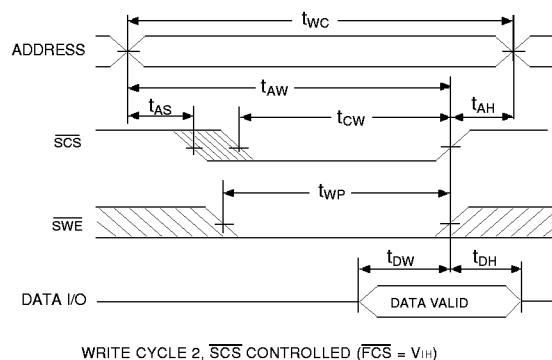
V_Z is programmable from -2V to +7V.

I_{OL} & I_{OH} programmable from 0 to 16mA.

Tester Impedance Z₀ = 75 Ω.

V_Z is typically the midpoint of V_{OH} and V_{OL}.

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

**FIG. 3 SRAM
TIMING WAVEFORM - READ CYCLE****FIG. 4 SRAM
WRITE CYCLE - $\overline{SWE}$ CONTROLLED****FIG. 5 SRAM
WRITE CYCLE - $\overline{SCS}$ CONTROLLED**



FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{\text{FWE}}$ CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		$\overline{\text{FWE}}$		$\overline{\text{FWE}}$		Unit
			Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	90		120		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	45		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	45		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		50		ns
Chip Select Hold Time	t _{WHEH}	t _{CH}	0		0		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		ns
Duration of Byte Programming Operation (min)	t _{WHWH1}		14		14		μs
Chip and Sector Erase Time	t _{WHWH2}		2.2	60	2.2	60	sec
Read Recovery Time Before Write	t _{GHWL}		0		0		μs
V _{CC} Set-up Time		t _{VCS}	50		50		μs
Chip Programming Time				12.5		12.5	sec
Output Enable Setup Time		t _{OES}	0		0		ns
Output Enable Hold Time (1)		t _{OEH}	10		10		ns

1. For Toggle and $\overline{\text{Data}}$ Polling.

FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		$\overline{\text{FWE}}$		$\overline{\text{FWE}}$		Unit
			Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	90		120		ns
Address Access Time	t _{AVQV}	t _{ACC}		90		120	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		90		120	ns
$\overline{\text{OE}}$ to Output Valid	t _{GLQV}	t _{OE}		40		50	ns
Chip Select to Output High Z (1)	t _{EHQZ}	t _{DF}		25		30	ns
$\overline{\text{OE}}$ High to Output High Z (1)	t _{GHQZ}	t _{DF}		25		30	ns
Output Hold from Address, $\overline{\text{FCS}}$ or $\overline{\text{OE}}$ Change, whichever is first	t _{AXQX}	t _{OH}	0		0		ns

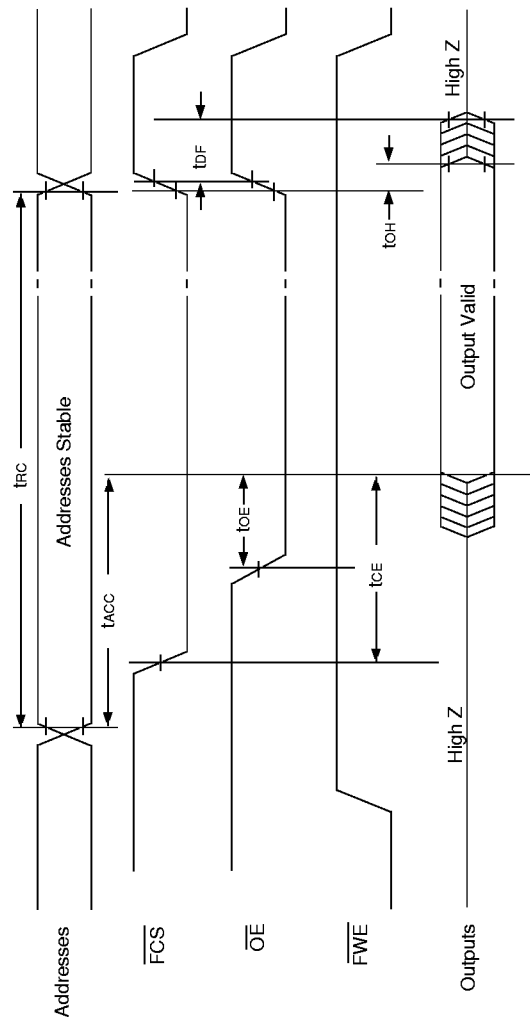
1. Guaranteed by design, not tested.

**FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{\text{FCS}}$ CONTROLLED**(V_{CC} = 5.0V, T_A = -55°C to +125°C)

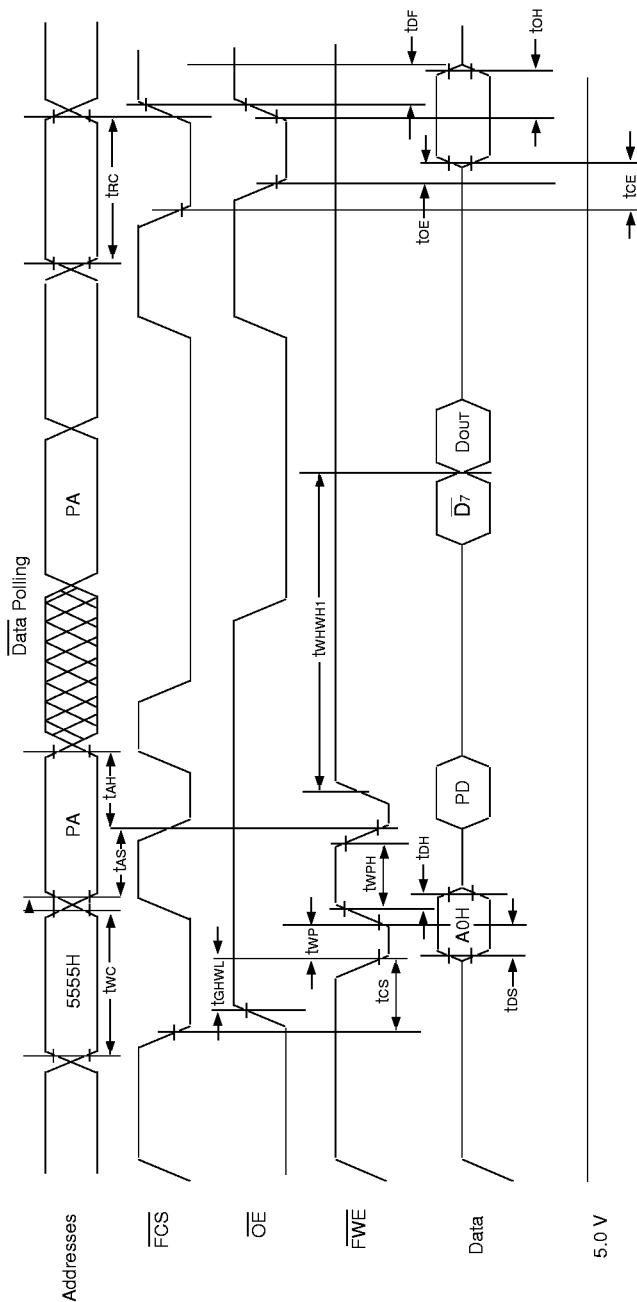
Parameter	Symbol		-90		-120		Unit
			Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	90		120		ns
$\overline{\text{FWE}}$ Setup Time	t _{WLLEL}	t _{WS}	0		0		ns
$\overline{\text{FCS}}$ Pulse Width	t _{ELEH}	t _{CP}	45		50		ns
Address Setup Time	t _{AVEL}	t _{AS}	0		0		ns
Data Setup Time	t _{DVEH}	t _{DS}	45		50		ns
Data Hold Time	t _{EHDX}	t _{DH}	0		0		ns
Address Hold Time	t _{ELAX}	t _{AH}	45		50		ns
$\overline{\text{FWE}}$ Hold from $\overline{\text{FWE}}$ High	t _{EHWH}	t _{WH}	0		0		ns
$\overline{\text{FCS}}$ Pulse Width High	t _{EHEL}	t _{CPH}	20		20		ns
Duration of Programming Operation	t _{WHWH1}		14		14		μs
Duration of Erase Operation	t _{WHWH2}		2.2	60	2.2	60	sec
Read Recovery before Write	t _{GHEL}		0		0		ns
Chip Programming Time				12.5		12.5	sec



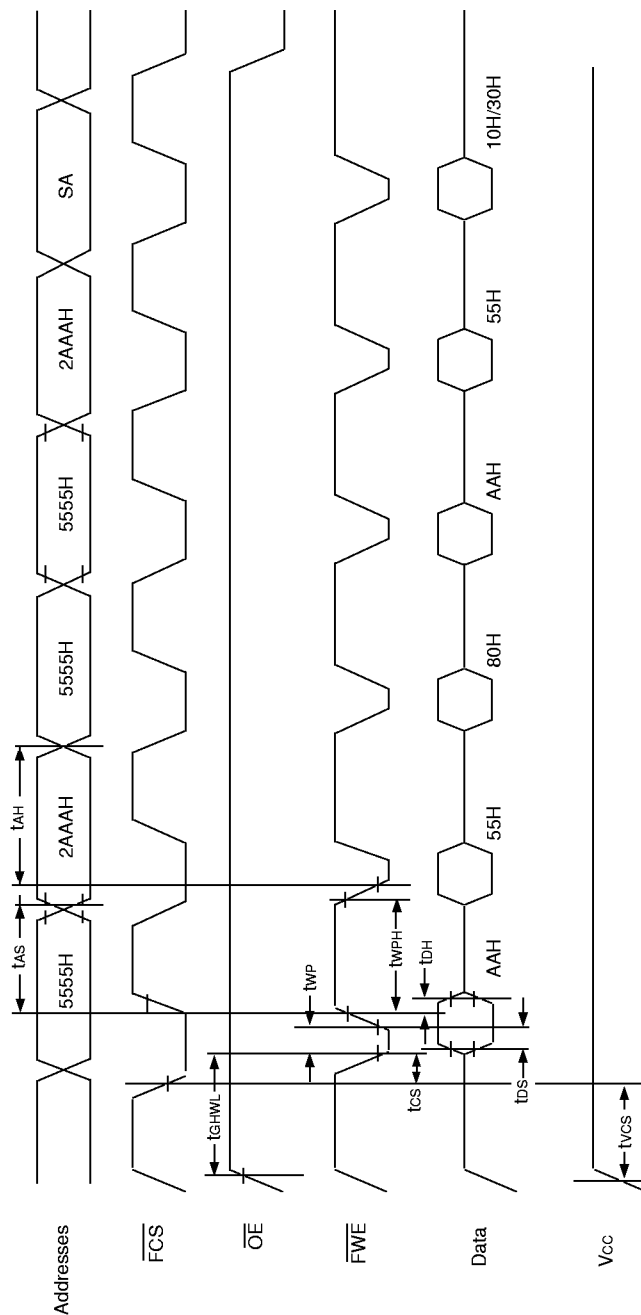
FIG. 6
AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS



NOTE: $\overline{SCS} = V_{IH}$

**FIG. 7****WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY $\overline{\text{FWE}}$ CONTROLLED****NOTES:**

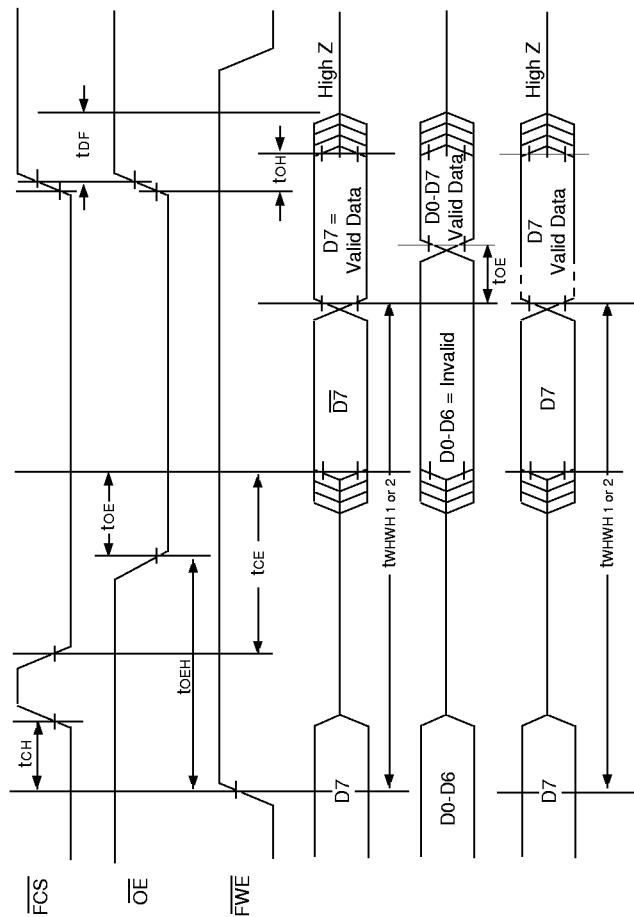
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{\text{D7}}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. $\text{SCS} = \text{V}_{\text{IH}}$

**FIG. 8****AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY****NOTES:**

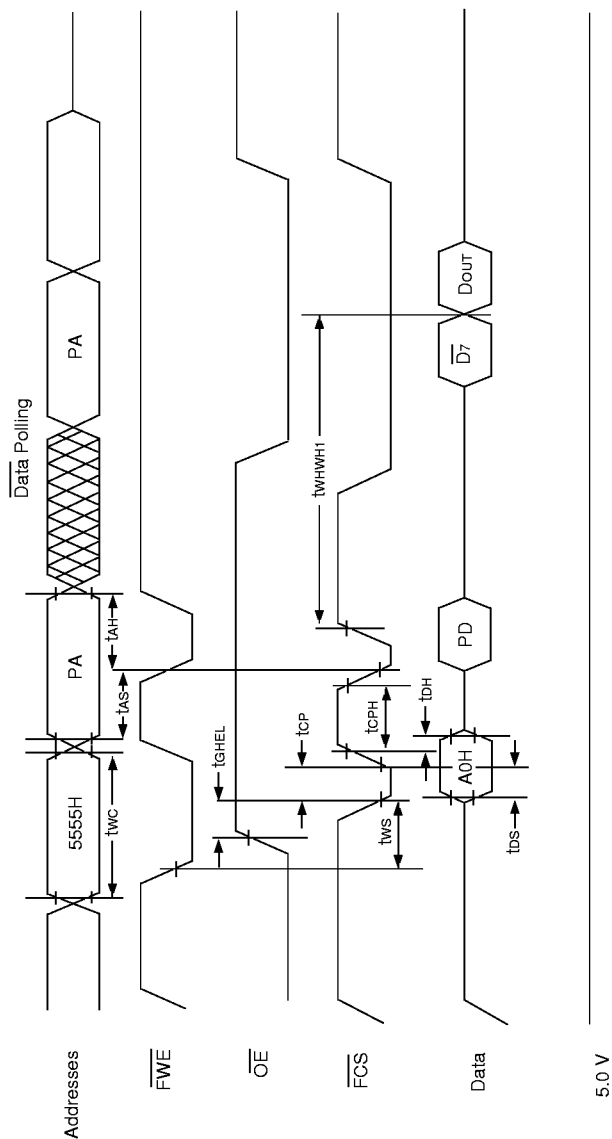
1. SA is the sector address for Sector Erase.
2. $\overline{SCS} = V_{IH}$



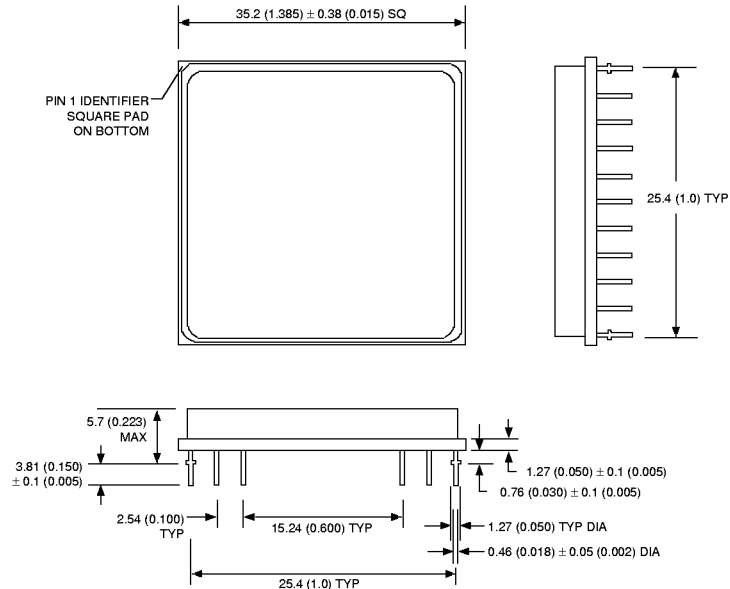
FIG. 9
AC WAVEFORMS FOR DATA POLLING DURING
EMBEDDED ALGORITHM OPERATIONS FOR
FLASH MEMORY



NOTE: $\overline{SCS} = V_{IH}$

**FIG. 10****WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY, $\overline{CS}$ CONTROLLED****NOTES:**

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.
6. $\overline{SCS} = V_{IH}$

**PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION**W S F 128K32 - XX H2 X X****LEAD FINISH:**Blank = Gold plated leads
A = Solder dip leads**DEVICE GRADE:**M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C**PACKAGE TYPE:**

H2 = Ceramic Hex In-line Package, HIP (Package 402)

ACCESS TIME (ns)22 = 25ns SRAM and 120ns FLASH
29 = 25ns SRAM and 90ns FLASH**ORGANIZATION, 128K x 32**

Flash PROM

SRAM

WHITE MICROELECTRONICS