IS32WV10008ALL
IS32WV10008BLL

1Meg x 8 LOW VOLTAGE, ULTRA LOW POWER PSEUDO RAM

ADVANCED INFORMATION
AUGUST 2002

FEATURES

- High-speed access time: 55ns, 70, 85, 100ns
- CMOS low power operation
- TTL compatible interface levels
- Single power supply
  - 1.65V--2.2V V_{DD} (32WV10008ALL)
  - 2.3V--3.6V V_{DD} (32WV10008BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available

DESCRIPTION

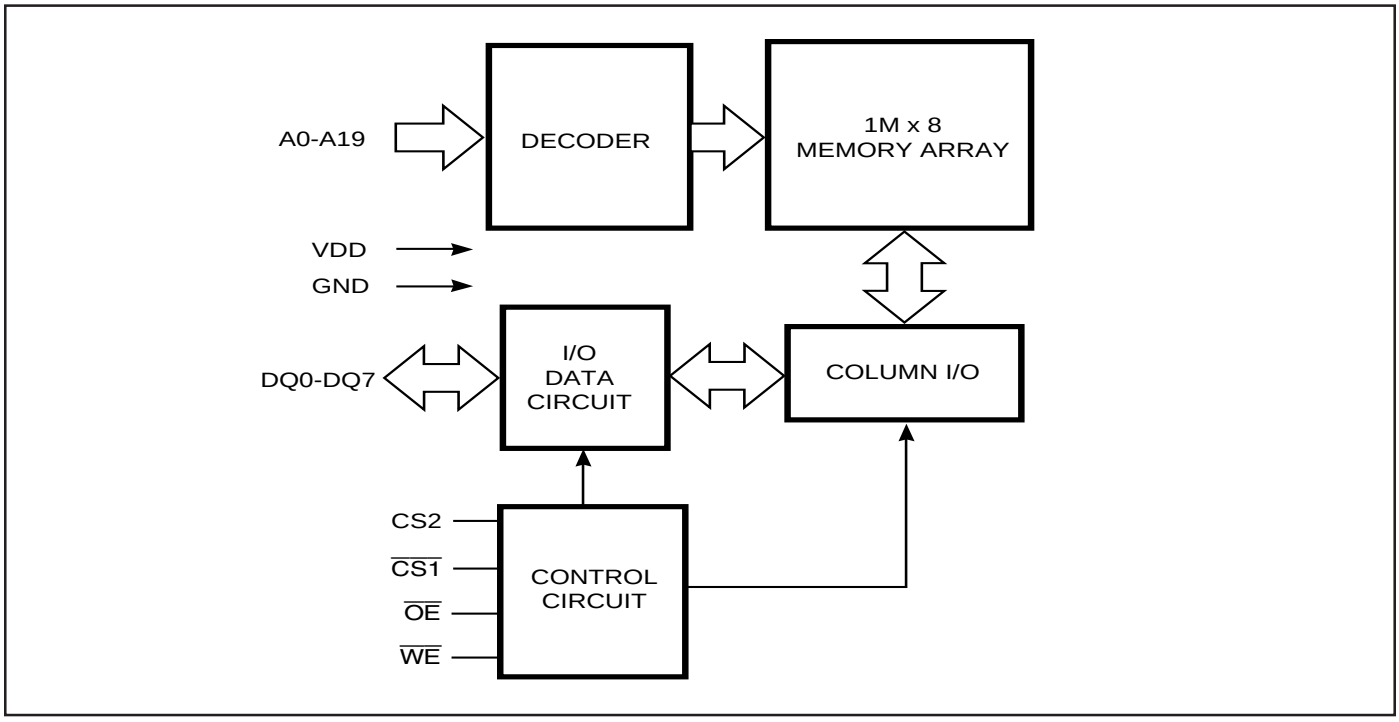
The *ISSI* IS32WV10008ALL/ IS32WV10008BLL are high-speed, 8M bit static RAMs organized as 1M words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected) or when $\overline{CS1}$ is LOW, CS2 is HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS32WV10008ALL and IS32WV10008BLL are packged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II).

FUNCTIONAL BLOCK DIAGRAM

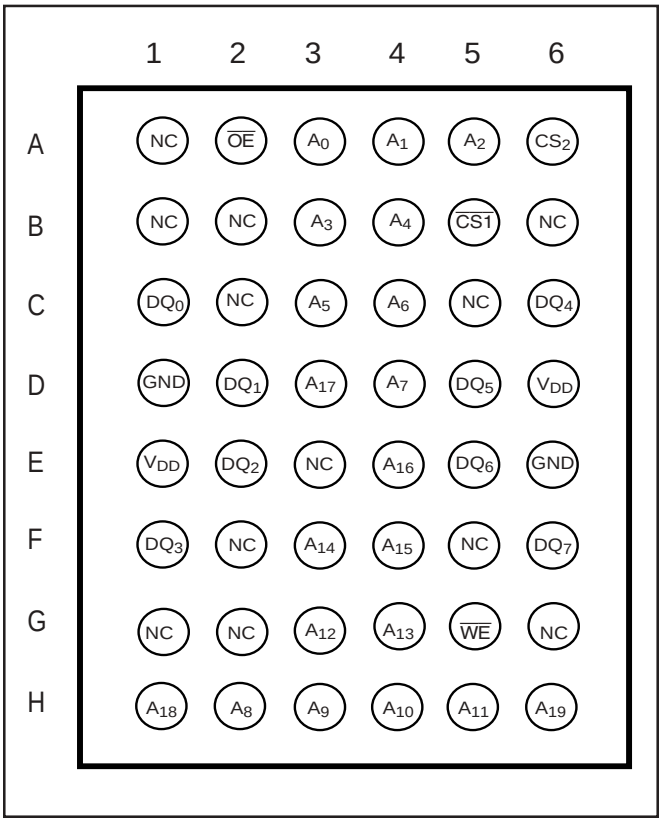


PIN DESCRIPTIONS

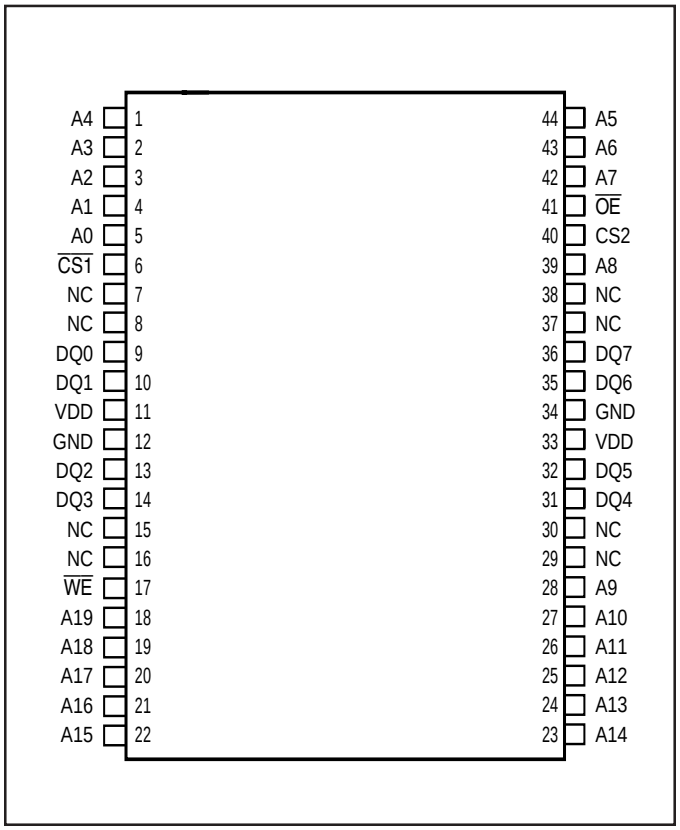
A0-A19	Address Inputs
$\overline{CS1}$	Chip Enable 1 Input
CS2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
DQ0-DQ7	Input/Output
NC	No Connection
V_{DD}	Power
GND	Ground

PIN CONFIGURATION

48-pin mini BGA (B) (6mm x 8mm)



44-pin TSOP (Type II)



OPERATING RANGE (V_{DD})

Range	Ambient Temperature	IS32WV10008ALL	IS32WV10008BLL
Commercial	0°C to +70°C	1.65V - 2.2V	2.3V - 3.6V
Industrial	–40°C to +85°C	1.65V - 2.2V	2.3V - 3.6V

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to V_{DD}+0.3	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
V_{DD}	V_{DD} Related to GND	–0.2 to +3.8	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
		I_{OH} = -1 mA	2.3-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
		I_{OL} = 2.1 mA	2.3-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
			2.3-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}[1]	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
			2.3-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –1.0V for pulse width less than 10 ns.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	32WV10008ALL (Unit)	32WV10008BLL (Unit)
Input Pulse Level	0.4V to V_{DD}-0.2	0.4 to 2.2V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	V_{DD}=1.65-2.2V	V_{DD}=2.3V-3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V_{REF}	0.9V	1.5V
V_{TM}	1.8V	2.8V

AC TEST LOADS

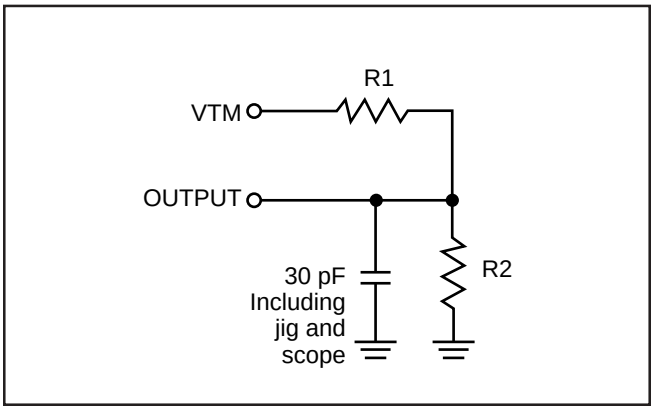


Figure 1

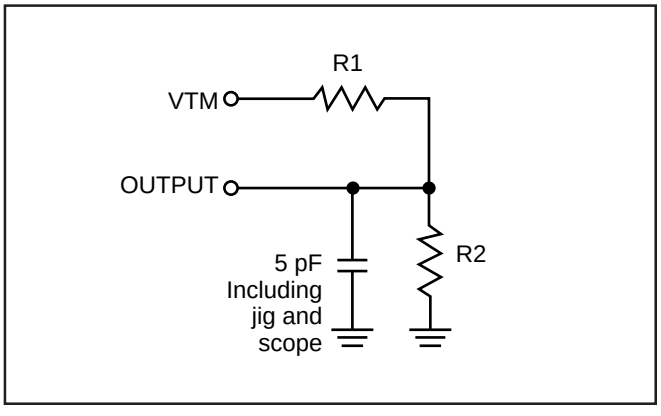


Figure 2

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

32WV10008ALL

Symbol	Parameter	Test Conditions		Max. 70	Max. 85	Max. 100	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	15 15	10 10	10 10	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0	Com. Ind.	3 3	3 3	3 3	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, f = 1 MHz	Com. Ind.	0.3 0.3	0.3 0.3	0.3 0.3	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1} \geq V_{DD} - 0.2V$, $CS2 \leq 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com. Ind.	40 40	40 40	40 40	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

32WV10008BLL

Symbol	Parameter	Test Conditions		Max. 55	Max. 70	Max. 85	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	15 15	15 15	10 10	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0	Com. Ind.	3 3	3 3	3 3	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, f = 1 MHz	Com. Ind.	0.3 0.3	0.3 0.3	0.3 0.3	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1} \geq V_{DD} - 0.2V$, $CS2 \leq 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com. Ind.	40 40	40 40	40 40	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

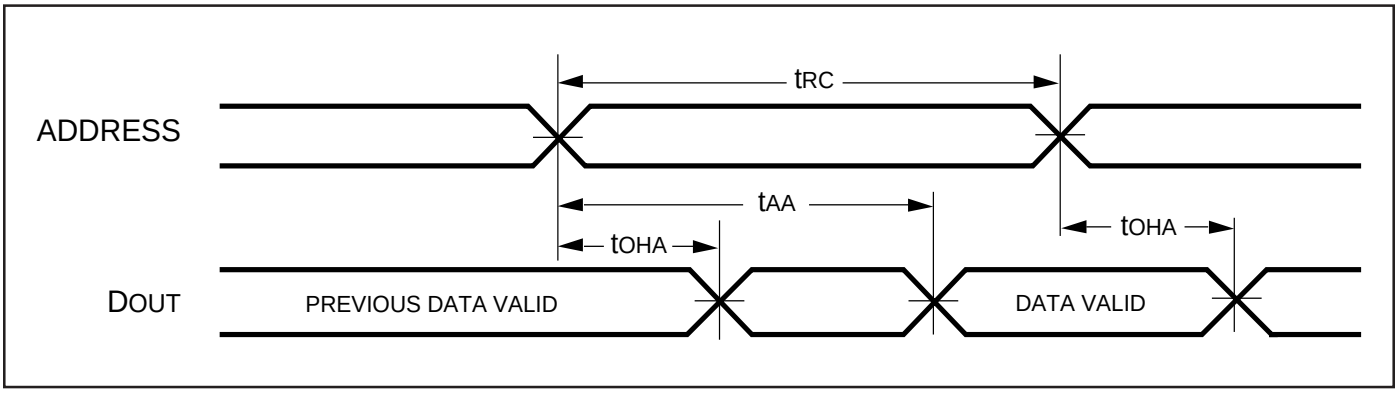
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	85ns Min.	85ns Max.	100ns Min.	100ns Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{OHA}	Output Hold Time	10	—	10	—	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	55	—	70	—	85	—	100	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	—	40	—	45	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	—	25	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	20	0	25	0	25	0	25	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	10	—	10	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

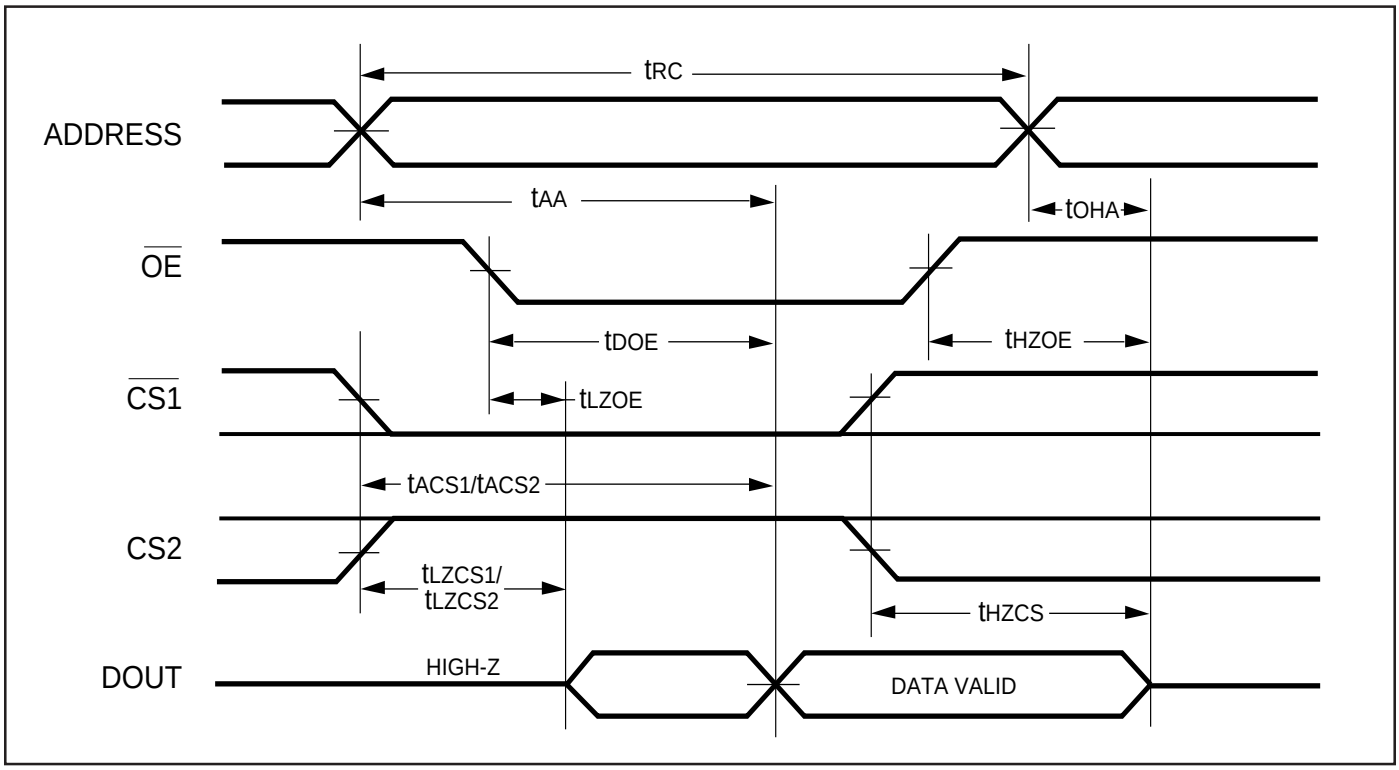
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{WE}$ = V_{IH})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$= V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW and CS2 HIGH transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

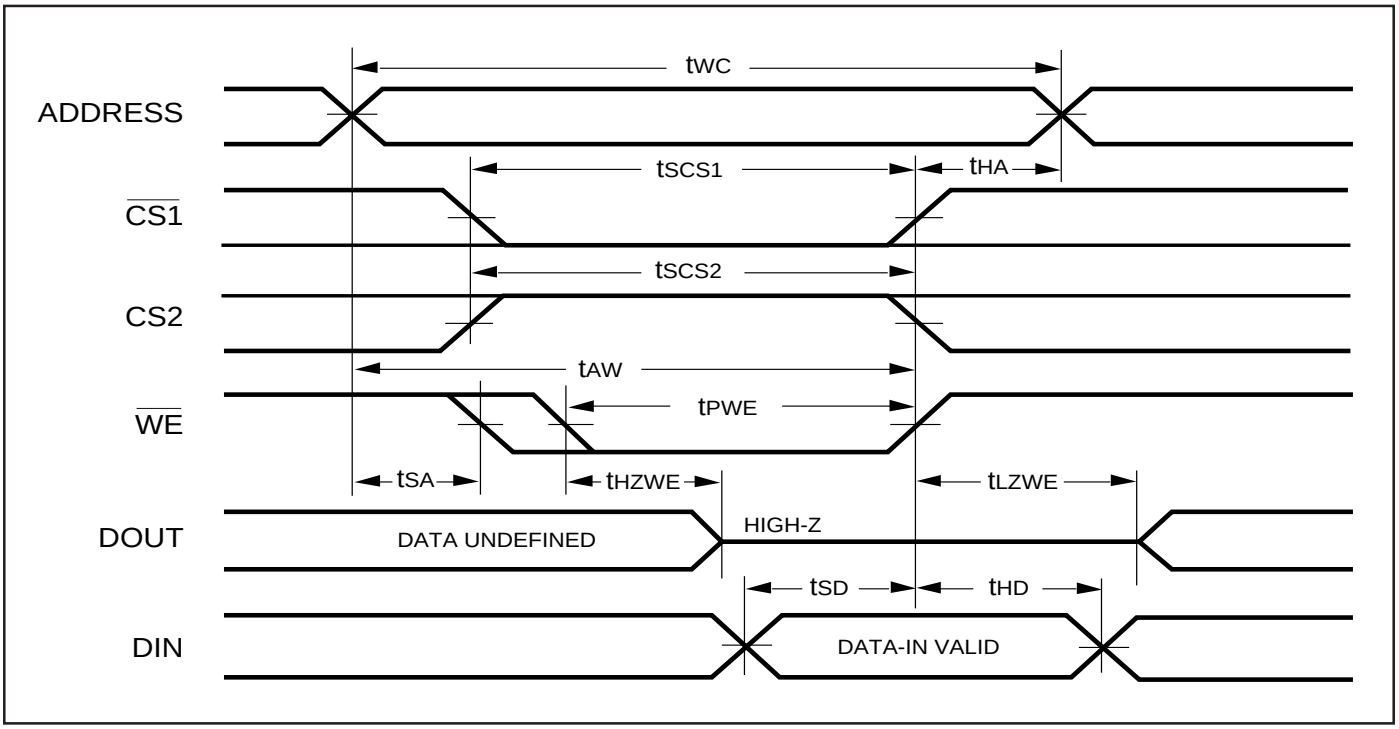
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	85 ns Min.	85 ns Max.	100 ns Min.	100 ns Max.	Unit
t_{WC}	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	45	—	60	—	65	—	70	—	ns
t_{AW}	Address Setup Time to Write End	45	—	60	—	65	—	70	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	40	—	50	—	60	—	60	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	35	—	40	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	20	—	20	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	5	—	ns

Notes:

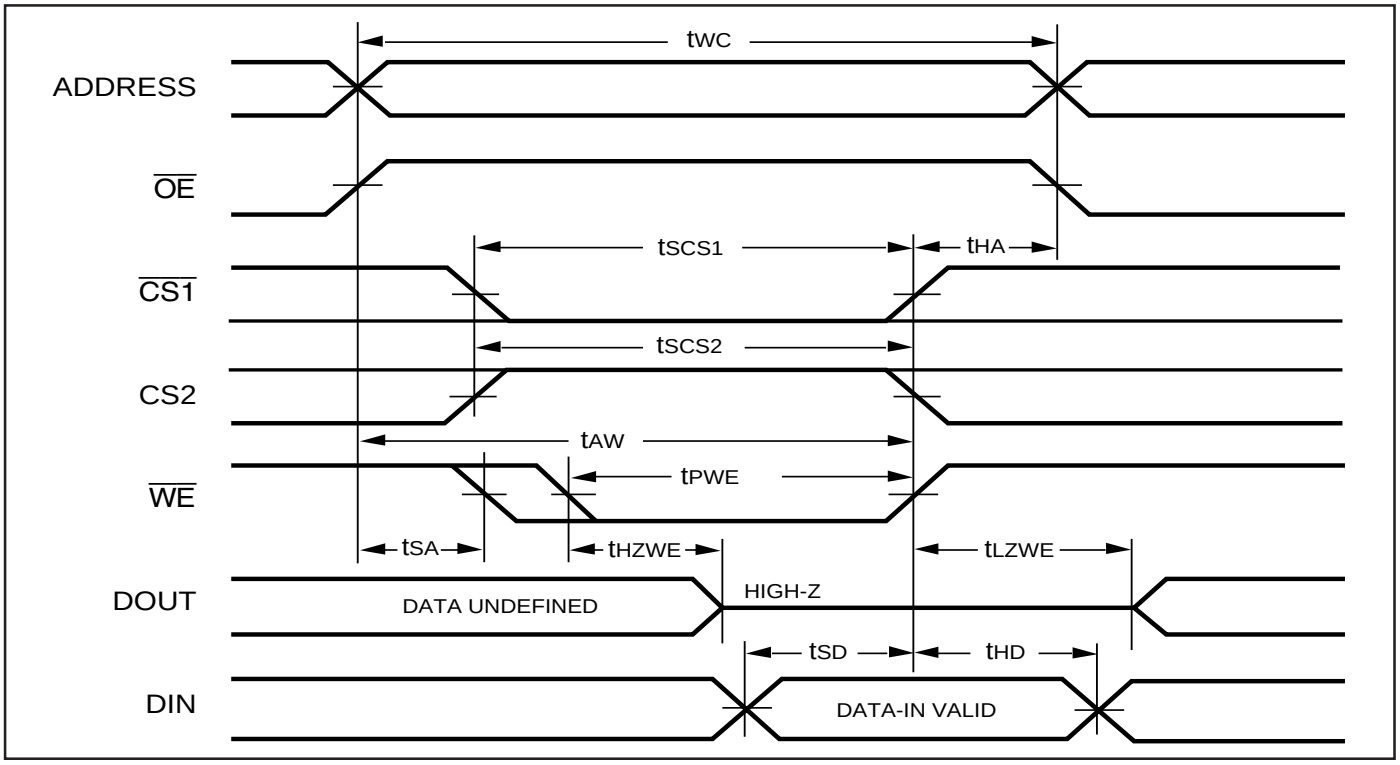
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

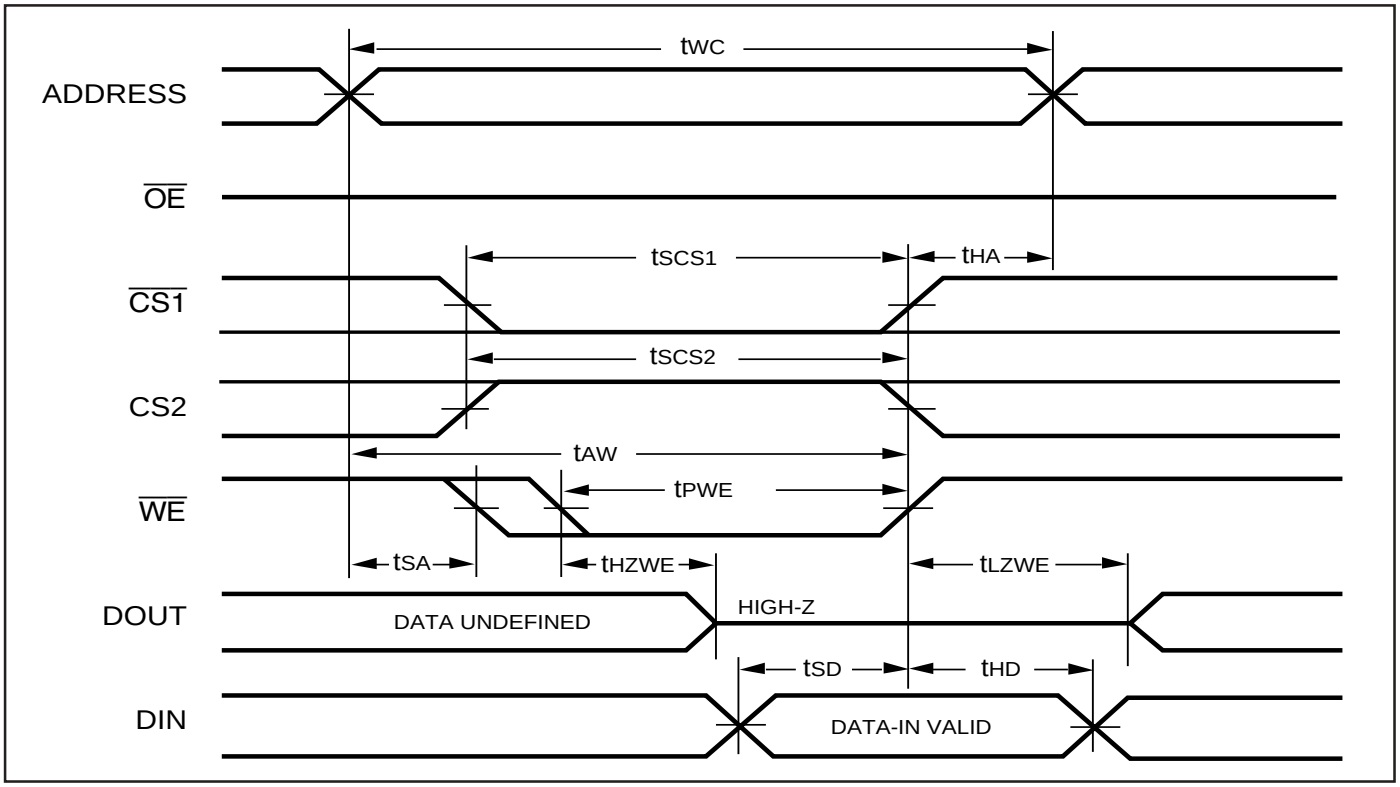
WRITE CYCLE NO. 1 ($\overline{CS1}$/CS2 Controlled, $\overline{OE}$ = HIGH or LOW)



WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



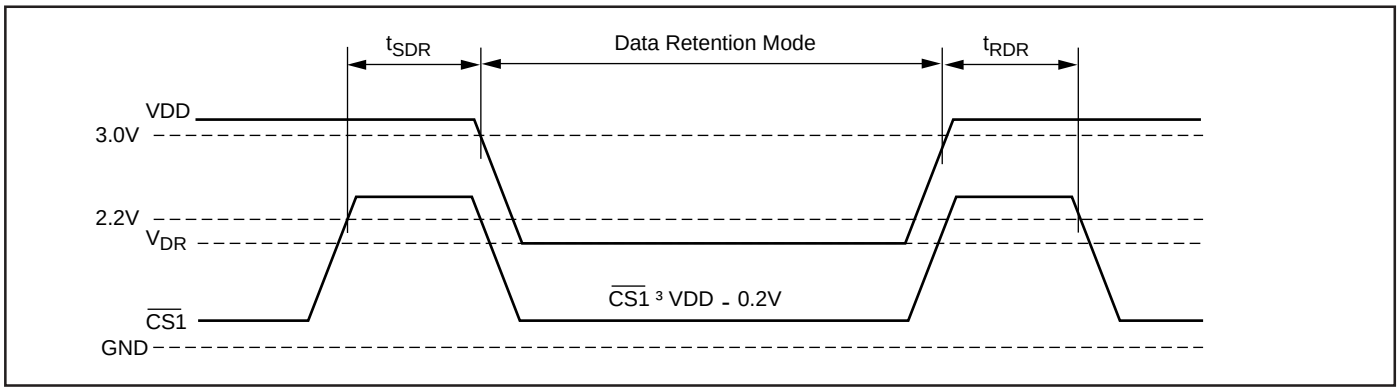
WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



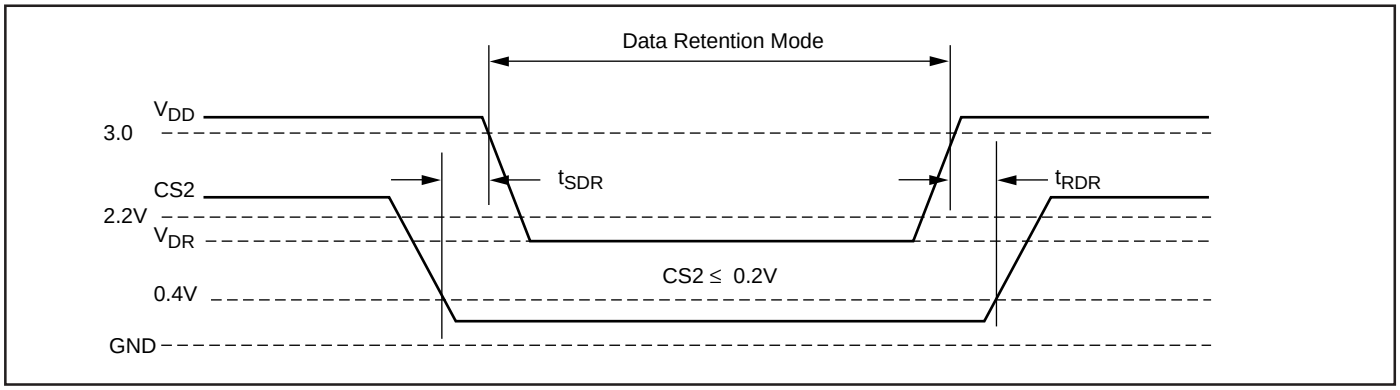
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	1.0	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 1.0V, $\overline{CS1}$/CS2 ≥ V_{DD} – 0.2V	—	15	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (CS2 Controlled)



ORDERING INFORMATION

IS32WV10008ALL (V_{DD} = 1.65V - 2.2V)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IS32WV10008ALL-70T	TSOP
	IS32WV10008ALL-70B	mini BGA (6mm x 8mm)
85	IS32WV10008ALL-70T	TSOP
	IS32WV10008ALL-70B	mini BGA (6mm x 8mm)
100	IS32WV10008ALL-70T	TSOP
	IS32WV10008ALL-70B	mini BGA (6mm x 8mm)

ORDERING INFORMATION

IS32WV10008ALL (V_{DD} = 1.65V - 2.2V)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS32WV10008ALL-70TI	TSOP
	IS32WV10008ALL-70BI	mini BGA (6mm x 8mm)
85	IS32WV10008ALL-70TI	TSOP
	IS32WV10008ALL-70BI	mini BGA (6mm x 8mm)
100	IS32WV10008ALL-70TI	TSOP
	IS32WV10008ALL-70BI	mini BGA (6mm x 8mm)

ORDERING INFORMATION

IS32WV10008BLL (V_{DD} = 2.3V - 3.6V)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IS32WV10008BLL-55T IS32WV10008BLL-55B	TSOP mini BGA (6mm x 8mm)
70	IS32WV10008BLL-70T IS32WV10008BLL-70B	TSOP mini BGA (6mm x 8mm)
85	IS32WV10008BLL-70T IS32WV10008BLL-70B	TSOP mini BGA (6mm x 8mm)
100	IS32WV10008BLL-70T IS32WV10008BLL-70B	TSOP mini BGA (6mm x 8mm)

ORDERING INFORMATION

IS32WV10008BLL (V_{DD} = 2.3V - 3.6V)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS32WV10008BLL-55TI IS32WV10008BLL-55BI	TSOP mini BGA (6mm x 8mm)
70	IS32WV10008BLL-70TI IS32WV10008BLL-70BI	TSOP mini BGA (6mm x 8mm)
85	IS32WV10008BLL-70TI IS32WV10008BLL-70BI	TSOP mini BGA (6mm x 8mm)
100	IS32WV10008BLL-70TI IS32WV10008BLL-70BI	TSOP mini BGA (6mm x 8mm)