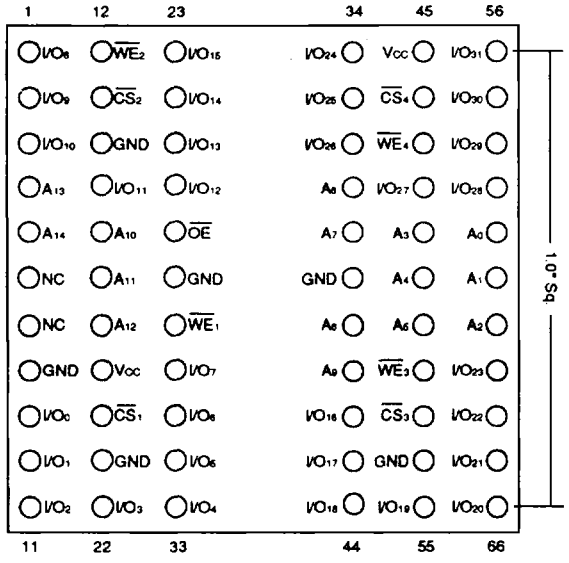

FIGURE 1 — Pin Configuration

I/O_{0-31}	Data Inputs/Outputs
A_{0-14}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

Pin Description

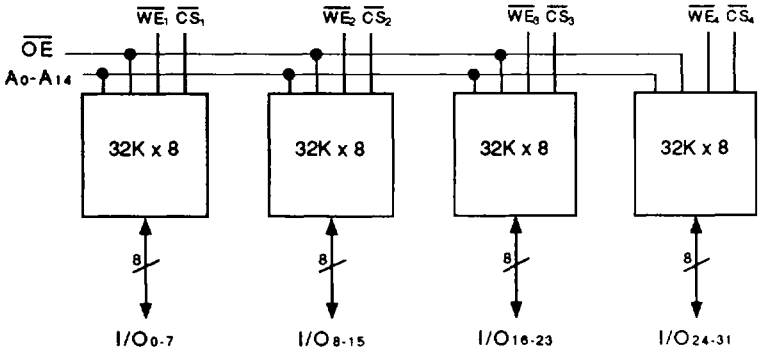

FIGURE 2 — Block Diagram

WS-32K32-XHX

1 Megabit CMOS SRAM Module

FEATURES

- **Access Times of 25nS to 120nS**
- **66-pin, PGA Type, 1.185 inch square HIP, Hermetic Ceramic Package**
- **User Configurable as 32Kx32, 64Kx16 or 128Kx8**
- **Battery Back-Up Operation**
- **Commercial, Industrial and Military Temperature Ranges**
- **TTL Compatible Inputs and Outputs**
- **Low Power CMOS Fully Static Design**
- **5 Volt Power Supply**
- **Built In Decoupling Caps and Multiple Ground Pins for Low Noise Operation**

DESCRIPTION

The White Technology WS-32K32-XHX is a 1-megabit CMOS SRAM module organized as 32K words by 32 bits; 64K x 16 or 128K x 8. The module is constructed on a multilayer ceramic substrate, hermetically sealed, with a welded metal cover, hex-in-line package (HIP) utilizing four 32K x 8 SRAM devices.

This device is part of White Technology's "WHIP" family of memory subsystems. These modules are compatible with most 66-pin HIP packaged SRAM, EEPROM and Flash memory modules.

The WS-32K32-XHX is available with access times of 25 to 120nS over the commercial and military temperature ranges.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both low. Reading the device is accomplished by taking the chip selects low while write enable remains high. Under these conditions the contents of the memory locations specified on the address pins will appear on the data input/output pins.

WHITS013

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Commercial	Military	Unit
Operating Temperature	T_A	0 to +70	-55 to +125	°C
Storage Temperature	T_{STG}	-40 to +85	-65 to +150	°C
Signal Voltage Relative to GND	V_G	-0.5 to +7.0	-0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}(1)	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

(1) V_{IL} (min.) = 3.0V for pulse width less than 20nS.

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby (deselect/power down)
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active (deselect)
L	X	L	Write	Data In	Active

CAPACITANCE

(@ T_A = 25°C)

Parameter	Symbol	Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	30	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	30	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Sym	Conditions	-25		-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}		15		15		15		15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		15		15		15		15	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		450		450		450		450	mA
Operating Supply Current x 16 Mode	I_{CC} x 16	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		280		280		280		280	mA
Operating Supply Current x 8 Mode	I_{CC} x 8	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		150		150		150		150	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		60		60		55		50	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = Min		0.4		0.4					V
		I_{OL} = 2.1mA, V_{CC} = Min						0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = Min	2.4		2.4						V
		I_{OH} = -1.0mA, V_{CC} = Min					2.4		2.4		V

Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}		15		15		15		15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		15		15		15		15	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		450		450		170		170	mA
Operating Supply Current x 16 Mode	I_{CC} x 16	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		280		280		110		110	mA
Operating Supply Current x 8 Mode	I_{CC} x 8	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		150		150		75		75	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		45		4		2.0		2.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.4		2.4		2.4		2.4		V

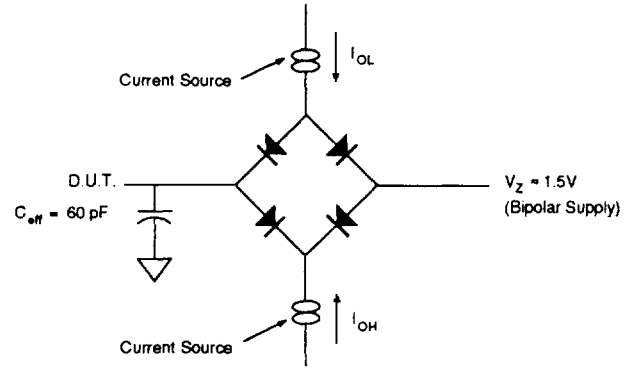

FIGURE 3 — AC Test Circuit

AC TEST CONDITIONS

Parameter	Typ.	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

Vz is programmable from -2V to +7V

I_{OL} & I_{OH} programmable from 0 to 16mA

Tester Impedance Z_0 = 75 Ω

Vz is typically the midpoint of V_{OH} and V_{OL} (i.e. (2.4 + 0.4)/2 = 1.4V)

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE Tester Includes Jig Capacitance

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter Read Cycle	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		55		nS
Address Access Time	t_{AA}		25		35		45		55	nS
Data Hold from Address Change	t_{OH}	4		4		4		4		nS
Chip Select Access	t_{ACS}		25		35		45		55	nS
Output Enable to Output Valid	t_{OE}		15		20		25		30	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]		12		15		20		25	nS
Output Disable to Output in High Z	t_{OHZ}[1]		12		15		20		25	nS

1. This parameter is guaranteed by design but not tested.

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		nS
Address Access Time	t_{AA}		70		85		100		120	nS
Data Hold from Address Change	t_{OH}	5		5		5		5		nS
Chip Select Access	t_{ACS}		70		85		100		120	nS
Output Enable to Output Valid	t_{OE}		35		40		45		50	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]		30		35		40		50	nS
Output Disable to Output in High Z	t_{OHZ}[1]		30		35		40		50	nS

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORMS

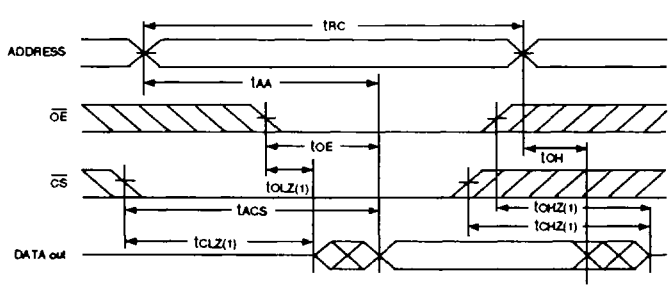

FIGURE 4 — Read Cycle Timing

1. Measured ± 200mV steady state; guaranteed by design but not tested.

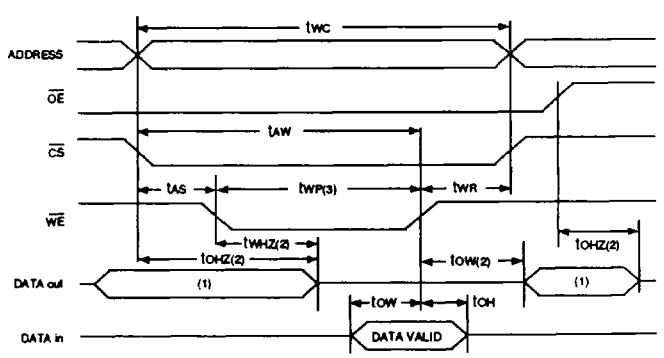

FIGURE 5 — Write Cycle Timing $\overline{WE}$ Controlled

1. I/O pins are in their output state, input signals must not be applied.
2. This parameter is guaranteed by design but not tested.
3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter Write Cycle	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		35		45		55		nS
Chip Select to End of Write	t_{CW}	20		30		40		45		nS
Address Valid to End of Write	t_{AW}	20		30		40		45		nS
Data to Write-Time Overlap	t_{DW}	15		18		20		25		nS
Write Pulse Width	t_{WP}	20		25		35		40		nS
Address Setup Time	t_{AS}	0		0		0		0		nS
Write Recovery Time	t_{WR}	0		0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		nS
Write to Output in High Z	t_{WHZ}[1]		10		15		15		20	nS
Data Hold from Write Time	t_{DH}	3		3		3		5		nS

1. This parameter is guaranteed by design but not tested.

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		nS
Chip Select to End of Write	t_{CW}	65		80		90		110		nS
Address Valid to End of Write	t_{AW}	65		80		90		110		nS
Data to Write-Time Overlap	t_{DW}	30		35		40		55		nS
Write Pulse Width	t_{WP}	45		50		55		65		nS
Address Setup Time	t_{AS}	5		5		5		5		nS
Write Recovery Time	t_{WR}	0		0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		nS
Write to Output in High Z	t_{WHZ}[1]		30		35		40		50	nS
Data Hold from Write Time	t_{DH}	5		5		5		5		nS

1. This parameter is guaranteed by design but not tested.

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	-25			-35			-45			-55			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		.5	8.0		.5	8.0		.5	8.0		.03	3.2	mA
	I_{CCDR2}	V_{CC} = 2V		.25	4.0		.25	4.0		.25	4.0		.02	2.1	mA

Parameter	Symbol	Conditions	-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		30	1200		10	1600		10	750		10	750	µA
	I_{CCDR2}	V_{CC} = 2V		20	900		7	1200		7	500		7	500	µA

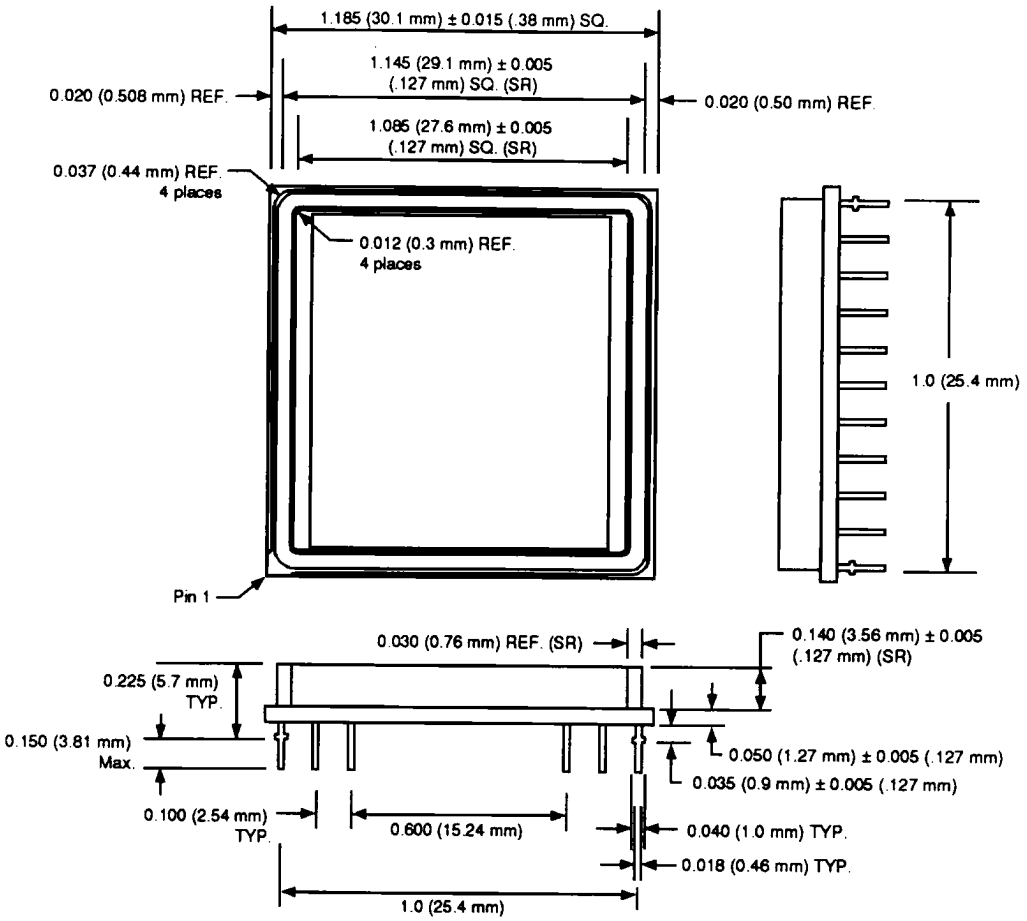

FIGURE 6 — Package Dimensions

ORDERING INFORMATION

W S - 32K 32 - XXX H X

DEVICE GRADE:
- Q = MIL-STD-883 Compliant
- M = Mil, -55°C to +125°C
- I = Industrial, -40°C to 85°C
- C = Commercial, 0 to 70°C

PACKAGE TYPE:
- H = Ceramic Hex in line package

ACCESS TIME IN nS

BITS PER WORD:
- x8, x16, x32

NUMBER OF WORDS:
- 128K, 64K, 32K

SRAM

WHITE TECHNOLOGY

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