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FUJITSU

F²MC-8L FAMILY MICROCONTROLLERS

MB89630 SERIES

HARDWARE MANUAL

F^{2}MC-8L FAMILY
MICROCONTROLLERS

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HARDWARE MANUAL

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PREFACE

The MB89630 series has been developed for application specific ICs (ASICs) and as a general-purpose, high-speed version of the F^{2}MC-8L (MB89600) family of 8-bit single-chip microcontrollers operating at low voltage.

This manual describes the functions and operation of the MB89630 series and should be read before use. For details of the instructions, refer to the MB89600 Series Programming Manual.

This manual consists of the following chapters:

Chapter 1 General

This chapter describes the MB89630 series' product lineup and product outline.

Chapter 2 Hardware Configuration

This chapter deals with the F^{2}MC-8L family's internal CPU configuration and operation modes, and the hardware specifications in the MB89630 series.

Chapter 3 Operation

This chapter explains the MB89630 series' use, reset sequence, interrupts, external bus operation, and low-power consumption modes.

Chapter 4 Instruction Overview

This chapter outlines the F^{2}MC-8L family's instructions.

Chapter 5 List of Mask Options

This chapter discusses the MB89630 series' mask options.

Appendix 1 I/O Map

This lists the registers in the I/O area.

Appendix 2 Write to MB89P637-based EPROM

This explains a write operation to an MB89P637-based EPROM.

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1. GENERAL

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The MB89630 series of single-chip microcontrollers use the F^{2}MC-8L CPU core for high-speed processing even at low voltages.

They contain resources such as timers, an UART, serial interfaces, an A/D converter, and an external-inter rupt input; they can be used widely in civil and industrial equipment, including portable equipment.

1.1 FEATURES

- High-speed processing even at low voltages
  Minimum instruction execution time: 0.4 μs at 3.5 V, 0.8 μs at 2.7 V
- F^{2}MC-8L CPU core
  Instruction system most suited to controller
  – Multiplication and division instructions
  – 16-bit arithmetic operation
  – Instruction test and branch instruction
  – Bit manipulation instruction, etc.
- Five types of timers
  – 8-bit PWM timer1 (usable as both reload timer and PWM timer)
  – 8-bit PWM timer2 (usable as both reload timer and PWM timer)
  – 8-bit pulse-width count timer (applicable to continuous measurement and remote control)
  – 16-bit timer/counter
  – 20-bit time-based counter
- UART
  Used for CLK synchronous and asynchronous data transfer (6, 7, and 8 bit length)
- Serial interface
  The transfer direction can be selected to communicate with various equipments.
- A/D converter
  – 10-bit resolution
  – Starting by external input or continuous start by internal timer
- External-interrupt input
  – Four channels
  – Four channels can be used independently to cancel the low-power consumption modes.
  – An edge-detection function is provided.
- Low-power consumption modes
  – Stop mode (Oscillation stops to minimize the current consumption.)
  – Sleep mode (The CPU stops to reduce the current consumption to about 30% of normal.)
- Bus interface function
  Supports Hold and Ready functions

1.2 PRODUCT SERIES

Table 1-1 lists the types and functions of the MB89630 series of microcontrollers.

Table 1.1 Types and Functions of MB89630 Series of Microcontrollers

Product Name	MB89635	MB89636	MB89637	MB89T635	MB89P637/W637	MB89PV630
Classification	Mass-produced product (Mask ROM product)			External ROM product	Temporal product/EPROM	Piggy back/ Evaluation and development
ROM capacity	16K × 8 bits (Internal ROM)	24K × 8 bits (Internal ROM)	32K × 8 bits (Internal ROM)	External ROM only	32K × 8 bits (Internal PROM, writable by general-purpose writers)	32K × 8 bits (External ROM)
RAM capacity	512 × 8bit	768 × 8bit	1024 × 8bit	512 × 8bit	1024 × 8bit	1024 × 8bit
CPU function	Number of basic instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum instruction execution time: 0.4 to 6.4 µs at 10 MHz and 61 µs at 32 kHz Interrupt processing time: 3.6 to 57.6 µs at 10 MHz and 562.5 µs at 32 kHz					
Number of ports	Input port: 5 (5 also used as resources) Output port (N-ch open drain): 8 (8 also used as resources) I/O port (N-ch open drain): 4 (4 also used as resources) Output port (CMOS): 8 (8 also used as bus-control pins) I/O port (CMOS): 28 (27 also used as both bus pins and resources) Total: 53					
PWM timer	8-bit reload timer operation (toggle output possible, operating clock cycle: 0.4 µs to 3.3 ms) × 2 ch 7/8-bit resolution PWM operation (conversion cycle: 51.2 µs to 839 ms) × 2 ch					
Pulse-width count timer	8-bit timer operation (overflow output possible, operating clock cycle: 0.4 µs to 12.8 µs) 8-bit reload timer operation (toggle output possible, operating clock cycle: 0.4 µs to 12.8 µs) 8-bit pulse-width measurement operation (continuous measurement possible: High and Low widths, and from ↑ to ↑ and from ↓ to ↓)					
Timer/counter	16-bit timer operation (operating clock cycle: 0.4 µs) 16-bit event counter operation (selectable from rising edge, falling edge, or both edges)					
Serial I/O	8-bit length Selectable from least significant bit (LSB) first or most significant bit (MSB) first Transfer clock (external, 0.8 µs, 3.2 µs, 12.8 µs)					
UART	Two system I/O can be used by software switching Transfer data length: 6, 7, 8 bits Transfer rate (300 to 62500 bps at original oscillation: 10 MHz)					
A/D converter	10-bit accuracy × 8 channels A/D conversion mode (conversion time: 13.2 µs) Sense mode (conversion time: 7.2 µs) Starting by external input or continuous start by internal timer					
External-interrupt input	Four independent channels (edge selection, interrupt vector, factor flag) Selectable from rising or falling edge Used for clearing stop or sleep mode (The edge can be detected even in the stop mode.)					
Standby mode	Sleep mode, stop mode, and watch mode					
Process	CMOS					
Package	DIP-64P-M01 FPT-64P-M06 FTP-64P-M09				P637 DIP-64P-M01 FTP-64P-M06 W637 DIP-64P-A06	MDP-64C-P02 MQP-64C-P01
Operating voltage	2.2 V to 6.0 V*			2.7 V to 6.0 V*		
EPROM used						MBM27C256A-20

* Varies according to conditions such as frequency. (See Recommended Operating Conditions, page 14.)

1.3 BLOCK DIAGRAM

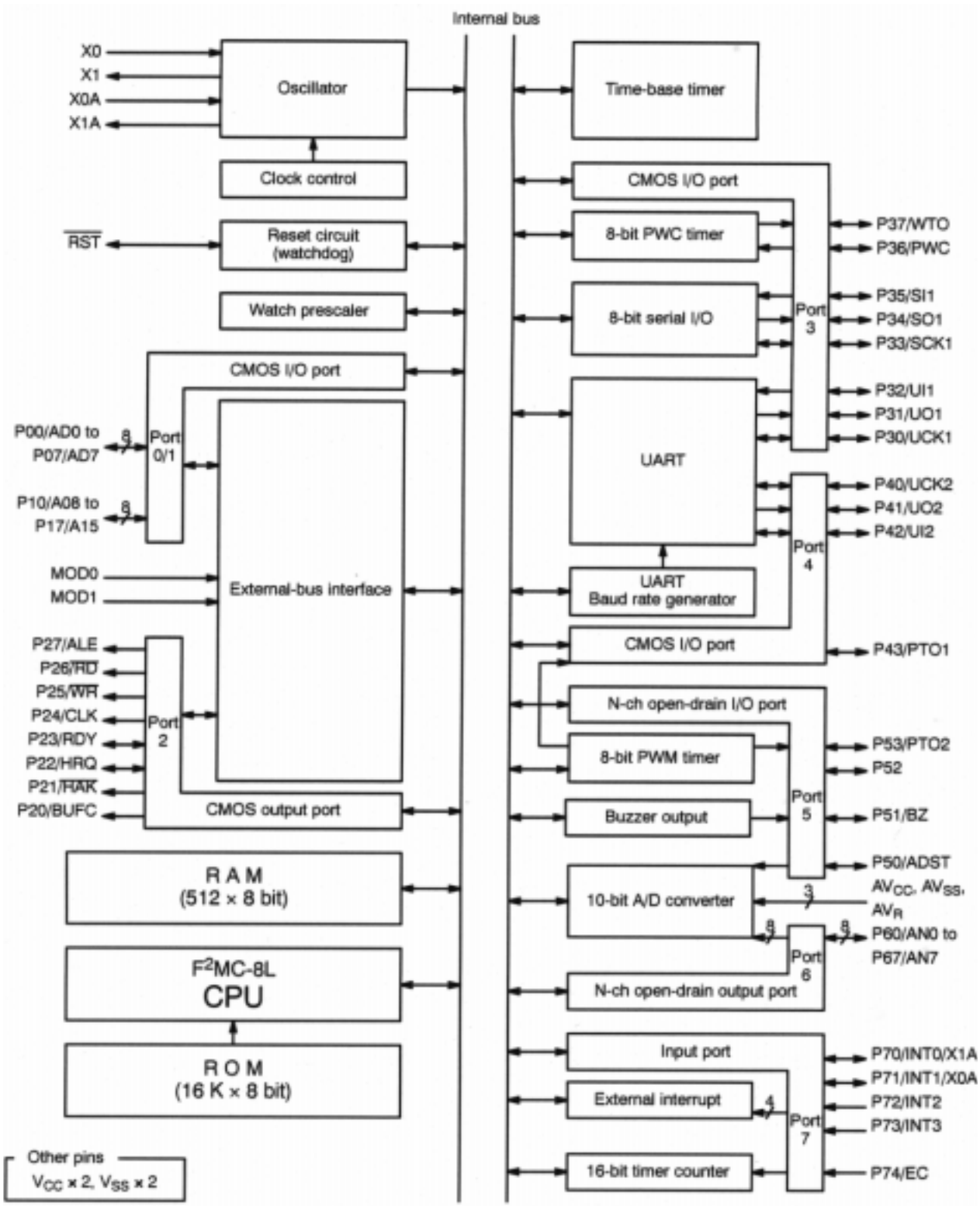


Fig. 1.1 Block Diagram (MB89635)

1.4 PIN ASSIGNMENT

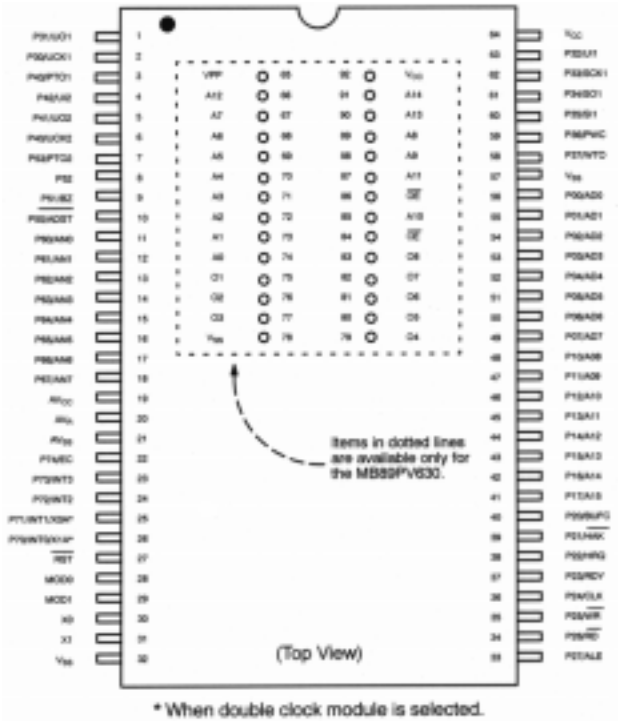


Fig. 1.2 Pin Assignment (DIP-64P-M01 and MDP-64C-P02)

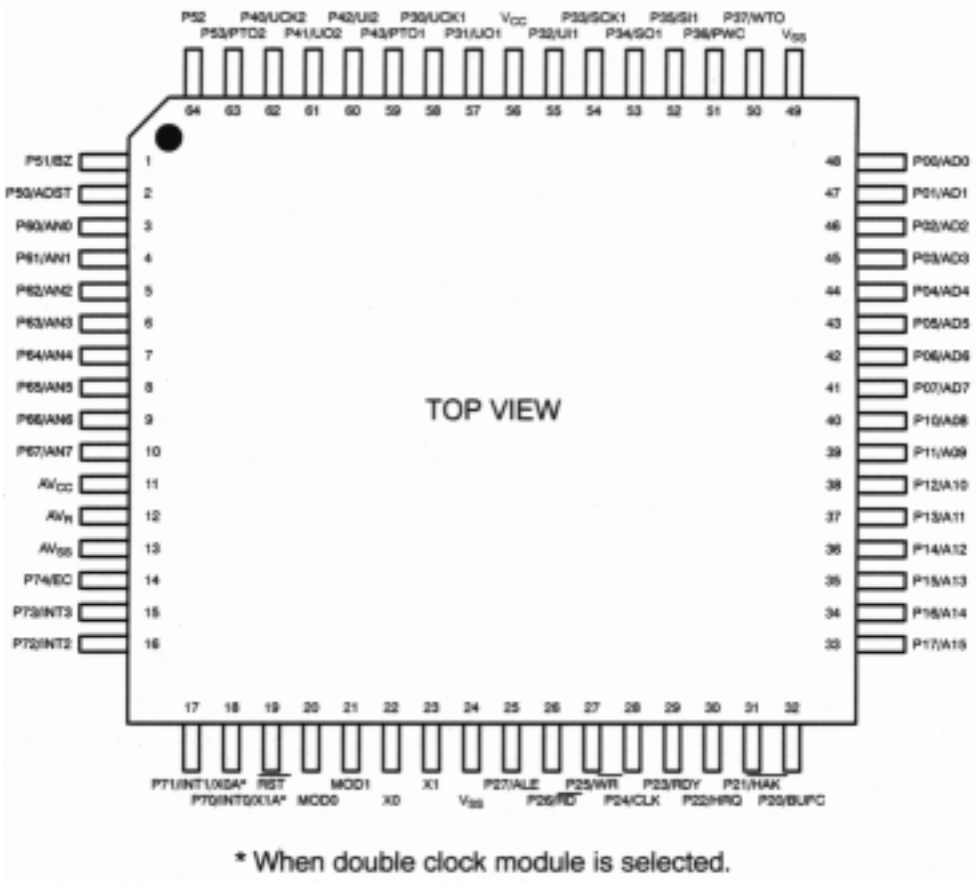
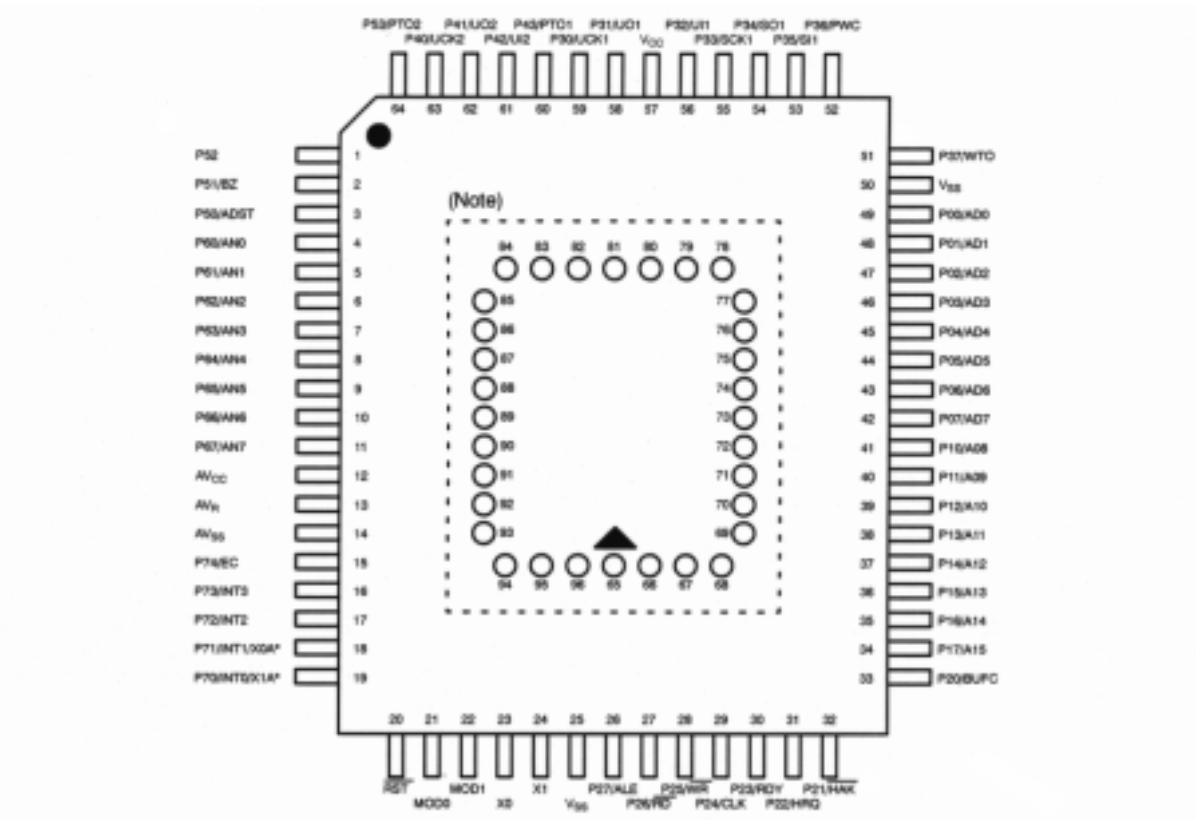


Fig. 1.3 Pin Assignment (FPT-64P-M09)



* When double clock module is selected.

Pin assignment on top of package (only for piggyback/evaluation type)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
65	N.C.	73	AD2	81	N.C.	89	$\overline{OE}$
66	V_{PP}	74	AD1	82	O4	90	N.C.
67	A12	75	AD0	83	O5	91	A11
68	AD7	76	N.C.	84	O6	92	A9
69	AD6	77	O1	85	O7	93	A8
70	AD5	78	O2	86	O8	94	A13
71	AD4	79	O3	87	$\overline{CE}$	95	A14
72	AD3	80	V_{SS}	88	A10	96	V_{CC}

Note: N.C.: Non-connection pin

Fig. 1.4 Pin Assignment (MQP-64C-P01 and FPT-64P-M06)

1.5 PACKAGE DIMENSIONS

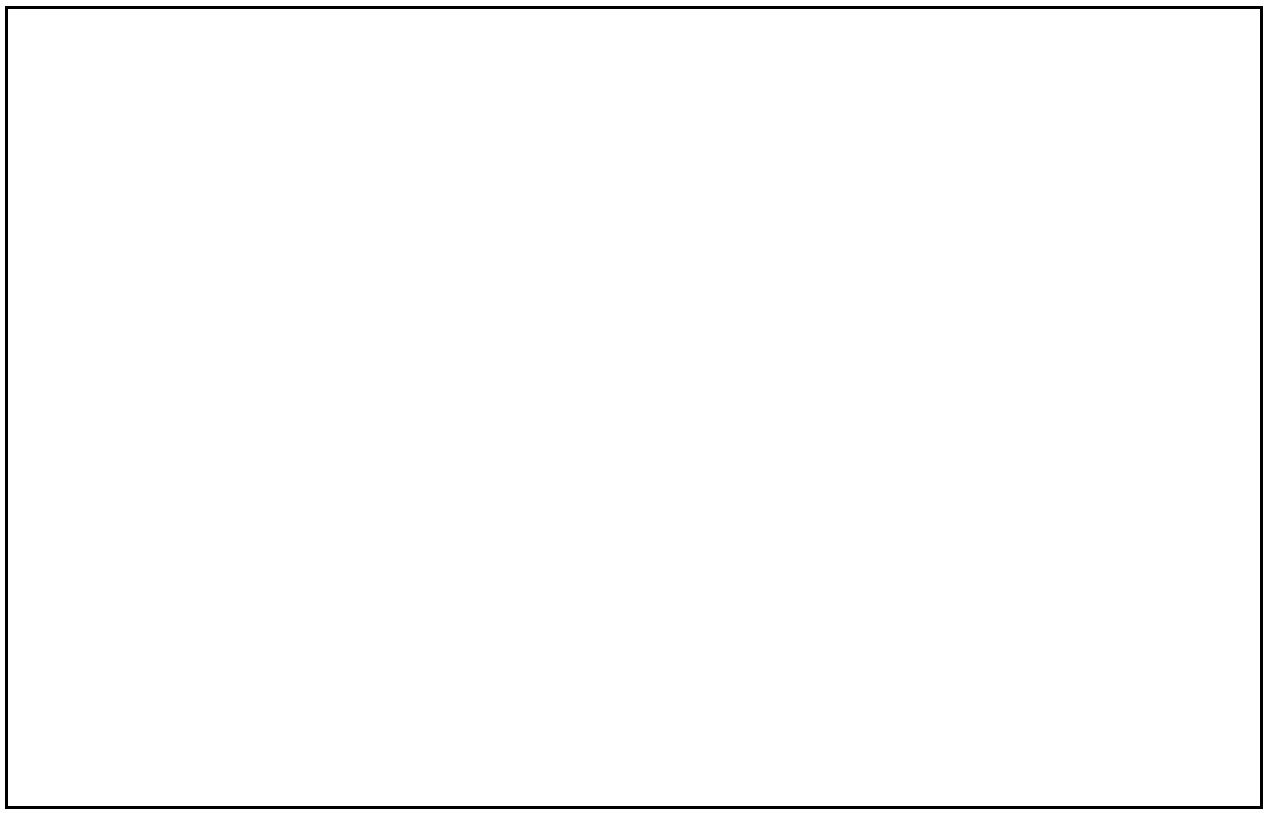


Fig. 1.5 Package dimension

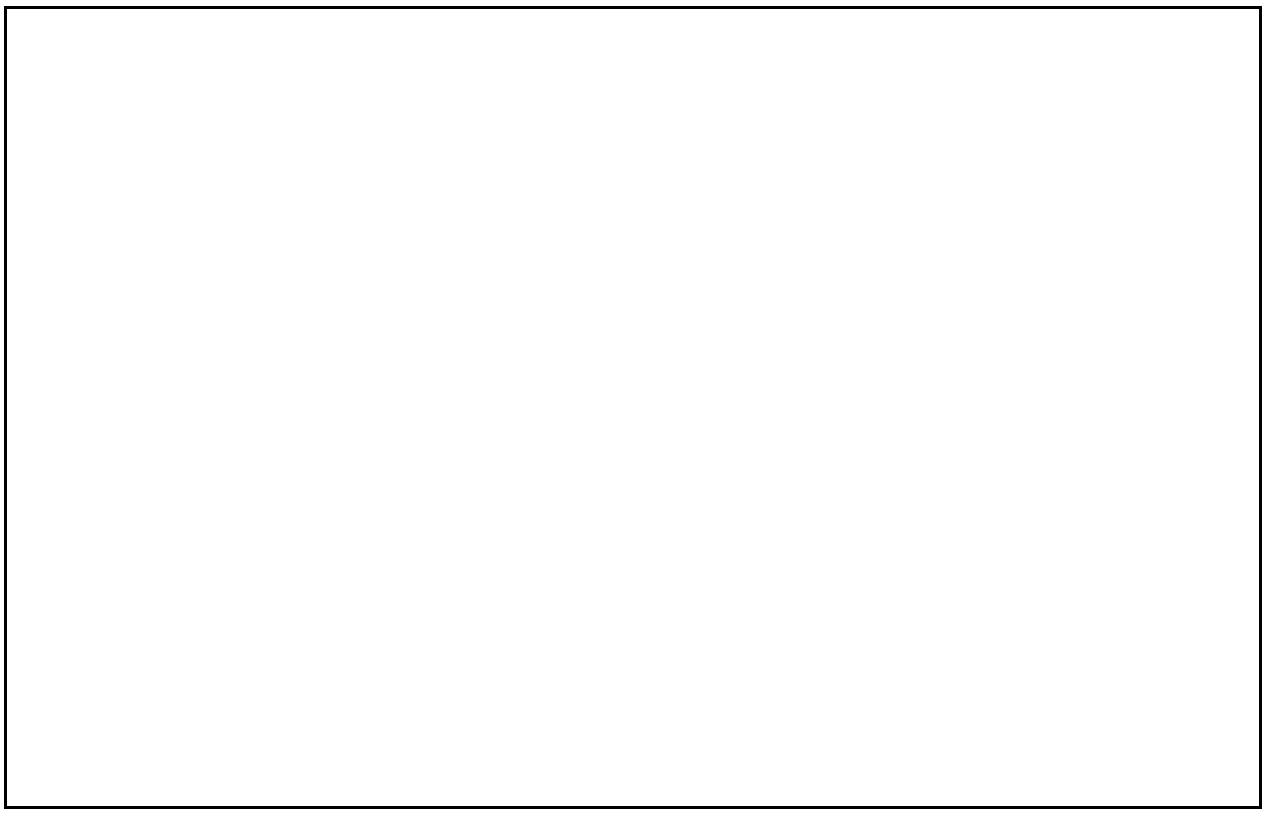
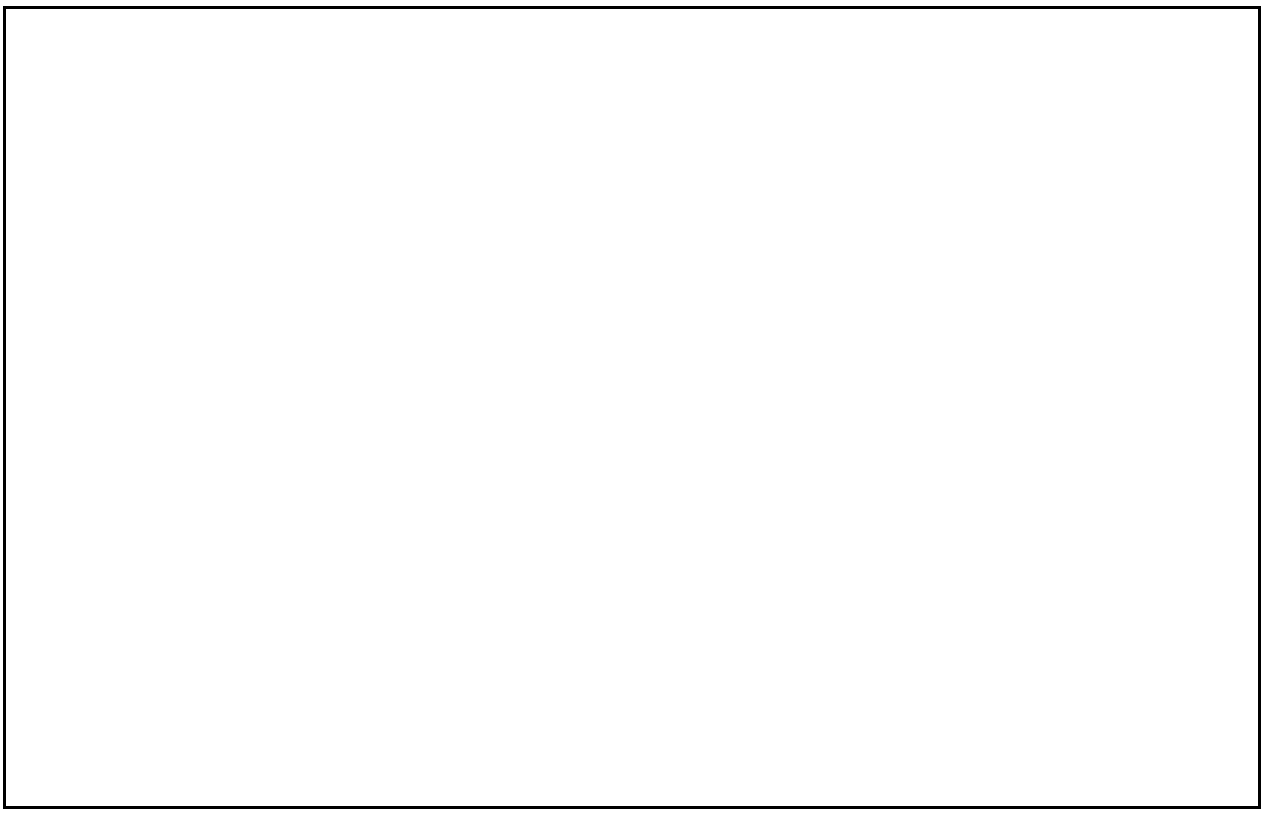


Fig. 1.6 Package dimension (QFP)



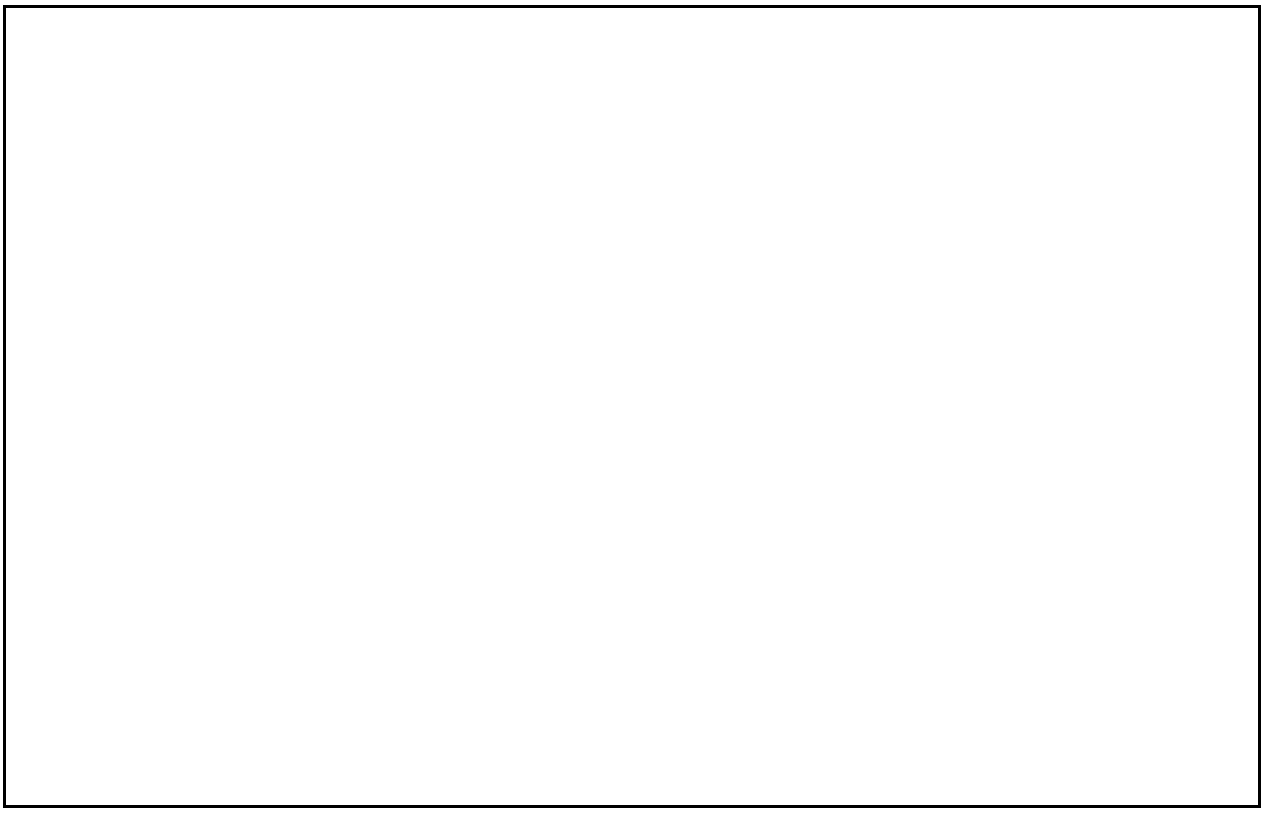


Fig. 1.7 Package dimension (MB89PV630)

1.6 PIN DESCRIPTION

Tables 1-2 and 1-3 list the pin functions and Table 1-4 shows the input/output circuits.

Table 1.2 Pin Description

Pin No.		Pin Name	Circuit type	Function
DIP-64P-M01	FPT-64P-M09			
30	22	X0	A	**Crystal oscillator pins**
31	23	X1		
28	20	MOD0	C	**Operation-mode select pins** These pins are connected directly to V_{CC} or V_{SS}.
29	21	MOD1		
27	19	$\overline{RST}$	B	**Reset I/O pin** This pin consists of an N-ch open-drain output with a pull-up resistor and hysteresis input. A Low level is output from this pin. The internal circuit is initialized at input of a Low level.
56 to 49	48 to 41	P00/AD0 to P07/AD7	E	**General-purpose I/O ports** When the external bus is used, these ports also serve as multiplex pins for output of lower addresses and data input/output.
48 to 41	40 to 33	P10/A08 to P17/A15	E	**General-purpose I/O ports** When the external bus is used, these ports also serve as pins for output of upper addresses.
40	32	P20/BUFC	G	**General-purpose output-only port** When the external bus is used, this port also serves as a buffer-control output pin by setting BCTR.
39	31	P21/$\overline{HAK}$	G	**General-purpose output-only port** When the external bus is used, this port also serves as a hold-acknowledge pin by setting BCTR.
38	30	P22/HRQ	E	**General-purpose output-only port** When the external bus is used, this port also serves as a hold-request input pin by setting BCTR.
37	29	P23/RDY	E	**General-purpose output-only port** When the external bus is used, this port also serves as a ready-input
36	28	P24/CLK	G	**General-purpose output-only port** When the external bus is used, this port also serves as a clock-output pin.
35	27	P25/$\overline{WR}$	G	**General-purpose output-only port** When the external bus is used, this port also serves as a write-signal output pin.
34	26	P26/$\overline{RD}$	G	**General-purpose output-only port** When the external bus is used, this port also serves as a read-signal output pin.
33	25	P27/ALE	G	**General-purpose output-only port** When the external bus is used, this port also serves as an address-latch signal-output pin.
2	58	P30/UCK1	F	**General-purpose I/O port** This port also serves as a clock I/O pin1 for the UART. Input is hysteresis type.
1	57	P31/UO1	E	**General-purpose I/O port** This port also serves as a data output pin1 for UART.

Table 1-2 Pin Description *(Continued)*

Pin No.		Pin Name	Circuit type	Function
DIP-64P-M01	FPT-64P-M09			
63	55	P32/UI1	F	**General-purpose I/O port** This port also serves as a data-input pin 1 for the UART. Input is hysteresis type.
62	54	P33/SCK1	F	**General-purpose I/O port** This port also serves as a data-input pin for serial I/O. Input is hysteresis type.
61	53	P34/SO1	E	**General-purpose I/O port** This port also serves as a data-output pin for serial I/O.
60	52	P35/SI1	F	**General-purpose I/O port** This port also serves as a data-input pin for serial I/O. Input is hysteresis type.
59	51	P36/PWC	F	**General-purpose I/O port** This port also serves as a measured-pulse input pin for the 8-bit pulse-width counter. Input is hysteresis type.
58	50	P37/WTO	E	**General-purpose I/O port** This port also serves as a toggle output pin for the 8-bit pulse-width counter.
6	62	P40/UCK2	F	**General-purpose I/O port** This port also serves as a clock I/O pin 2 for UART. Input is hysteresis type.
5	61	P41/UO2	E	**General-purpose I/O port** This port also serves as a data-output pin 2 for UART.
4	60	P42/UI2	F	**General-purpose I/O port** This port also serves as a data-input pin 2 for UART. Input is hysteresis type.
3	59	P43/PTO1	E	**General-purpose I/O port** This port also serves as a toggle output pin for the 8-bit PWM timer.
10	2	P50/ADST	J	**General-purpose I/O port** This port also serves as an external activation pin for the A/D converter. Input is hysteresis type.
9	1	P51/BZ	I	**General-purpose I/O port** This port also serves as a buzzer output pin.
8	64	P52	I	**General-purpose I/O port**
7	63	P53/PTO2	I	**General-purpose I/O port** This port also serves as a toggle output pin for the 8-bit PWM timer.
11 to 18	3 to 10	P60/AN0 to P67/AN7	H	**N-ch open-drain output-only ports** These ports also serve as analog input pins for the A/D converter.
26 to 25	18 to 17	P70/INT0/X1A to P71/INT1/X0A	A/D	**Input-only ports** Input is hysteresis type. These ports also serve as input pins for external interrupt (at single clock operation). Crystal oscillation pins (at double clock operation)
24 to 23	16 to 15	P72/INT2 to P73/INT3	D	**Input-only ports** These ports also serve as input pins for external interrupt. Input is hysteresis type.
22	14	P74/EC	D	**General-purpose input port** This port also serves as an external clock input pin for the 16-bit timer counter. Input is hysteresis type.
64	56	V_{CC}	—	**Power pin**
32, 57	24, 49	V_{SS}	—	**Power (GND) pins**
19	11	AV_{CC}	—	**Power pin for A/D converter**
20	12	AV_R	—	**Reference-voltage input pin for A/D converter**
21	13	AV_{SS}	—	**Power pin for A/D converter** It should be used at the same potential at V_{SS}.

Table 1.3 Pins for External ROM

Pin No.		Pin Name	Circuit type	Function
DIP-64C-P02	FPT-64C-P01			
65	66	V_{PP}	Output	**High-level output pin**
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	Output	**Address-output pins**
75 76 77	77 78 79	O1 O2 O3	Input	**Data-input pins**
78	80	V_{SS}	Output	**GND pin**
79 80 81 82 83	82 83 84 85 86	O4 O5 O6 O7 O8	Input	**Data-input pins**
84	87	$\overline{CE}$	Output	**Chip-enable pin for ROM** A High level is output in the standby mode.
85	88	A10	Output	**Address-output pin**
86	89	$\overline{OE}$	Output	**Output-enable pin for ROM** A Low level is always output.
87 88 89	91 92 93	A11 A9 A8	Output	**Address-output pins**
90	94	A13	Output	**Address-output pins**
91	95	A14	Output	**Address-output pins**
92	96	V_{CC}	Output	**Power pin for EPROM**
—	65 76 81 90	N.C.	—	**Non-connection pins which have internal-connection** These pins must be open when the device is used.

Table 1.4 Input/Output Circuit Configurations

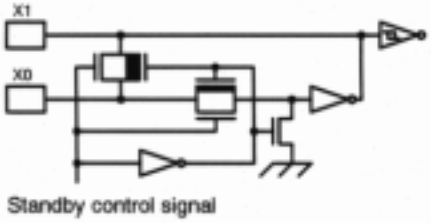
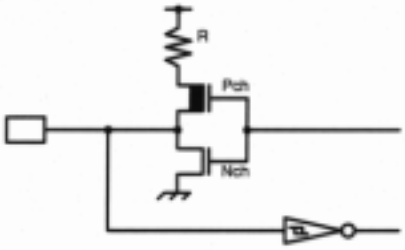
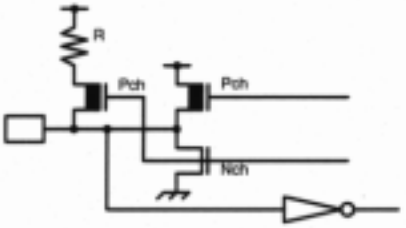
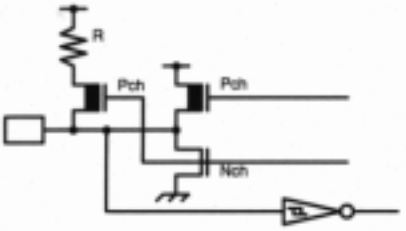
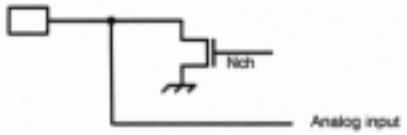
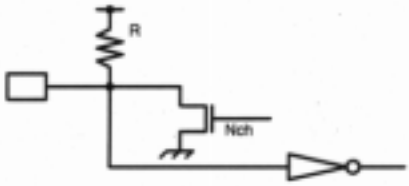
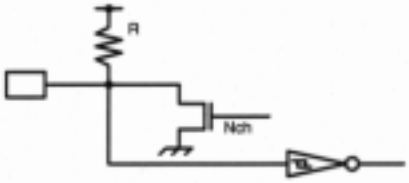
Classification	Circuit	Remarks
A		• Oscillation feedback resistor: About 2 MΩ (Main clock side)
B		• Output pull-up resistor (P-ch): About 50 kΩ (5 V) • Hysteresis input
C		• CMOS input
D		• Hysteresis input • The pull-up resistor is optional. (P70 and P71 are excluded)
E		• CMOS output • CMOS input • The pull-up resistor is optional. (P22 and P23 are excluded)
F		• CMOS output • Hysteresis input • The pull-up resistor is optional.
G		• CMOS output

Table 1-4 Input/Output Circuit Configurations *(Continued)*

Classification	Circuit	Remarks
H		• Analog input
I		• CMOS input • The pull-up resistor is optional.
J		• Hysteresis input • The pull-up resistor is optional.

1.7 HANDLING DEVICES

(1) Prevention of latch-up

In the CMOS IC, latch-up may occur when a voltage higher than V_{CC} or lower than V_{SS} is applied to other than the middle- or high-voltage resistant input or output pins, or when voltage exceeding the Absolute Maximum Ratings is applied between V_{CC} and V_{SS} pins.

When latch-up occurs, the supply current increases rapidly, sometimes resulting in overheating and destruc tion. Therefore, no voltage exceeding the Absolute Maximum Ratings should be used.

(2) Unused input pins

Leaving unused input pins open may cause a malfunction. Therefore, these pins should be pulled up or down with optional resistors in the Input/Output circuits. If the Input/Output circuit has no optional resistor, an exter nal resistor should be used.

(3) Non-Connected pins which have internal-connection (N.C.)

Non-Connected pins which have internal-connection (N.C.) must be open when the device is used.

(4) Variations in supply voltage

Some malfunction may be caused by an abrupt change of the power supply voltage even though the voltage is in the guaranteed range. For this reason, the power supply to the device should be stabilized. For the stabi lization, it is recommended to keep the power supply for the V_{CC} ripple voltage regulation (peak-to-peak) to less than 10% of the typical V_{CC} at the commercial frequency (50 to 60 Hz), and the coefficient of transitional variation should be less than 0.1 V/ms at a sudden supply voltage change (e.g. voltage switching).

(5) Precautions for external clock

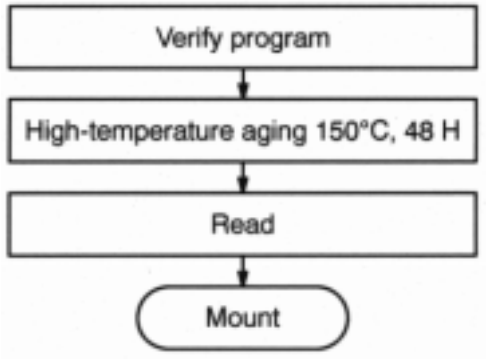
It may take a little time to stabilize the clock oscillation. The stabilization time should also be considered for an external clock during resets because all internal circuits in the device need to be initialized. So, an external clock should be input just after power-on reset (option selection) and cancellation of stop mode.

(6) Pin processing performed when A/D converter not used

When the A/D converter is not used, the pins should be connected to be $AV_{CC} = V_{CC}$, and $AV_{SS} = AV_R = AV_{SS}$.

(7) Recommended screening conditions

The OTPROM product should be screened by high-temperature aging before mounting.



Yield of preprogrammed product

The programming test cannot be performed for all bits of the preprogrammed OTPROM product due to its characteristics. Consequently, 100% yield of programming cannot be ensured.

2. HARDWARE CONFIGURATION

2.1 CPU 2-3
2.2 RESOURCE FUNCTIONS 2-27

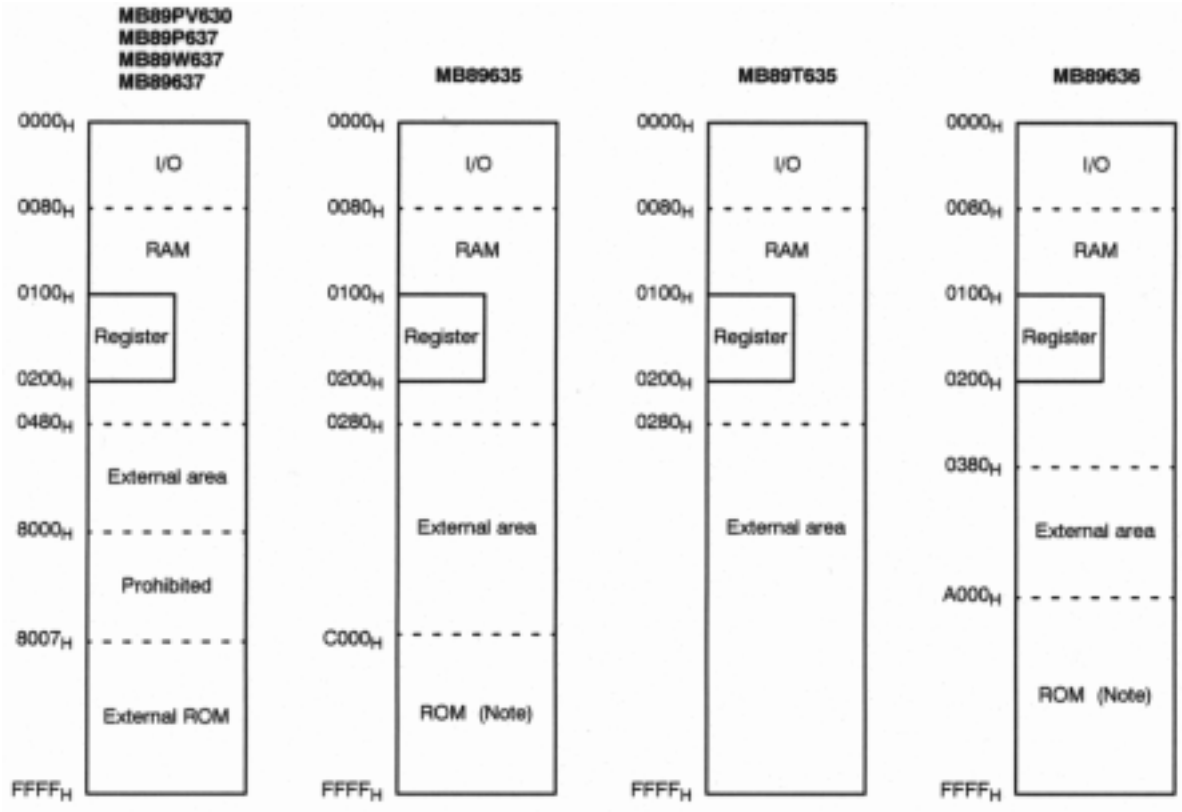
2.1 CPU

This section describes the CPU hardware composition. The CPU has the following six functions.

- Memory Space
- Arrangement of 16-bit Data in Memory
- Registers
- Operation Modes and External Bus Operation
- Clock Control Block
- Interrupt Controller

2.1.1 Memory Space

The MB89630 series of microcontrollers have a memory area of 64 Kbytes. All I/O, data, and program areas are located in this space. The I/O area is near the lowest address and the data area is immediately above it. The data area may be divided into register, stack, and direct-address areas according to the applications. The program area is located near the highest address and the tables of interrupt and reset vectors and vector-call instructions are at the highest address. Figure 2.1 shows the structure of the memory space for the MB89630 series of microcontrollers.



Note: This ROM space can be used for external data in mode operation. The ROMs of the MB89W637 and MB89P637 are internal OTPROMs. The ROM space is from **8007_H** to **$FFFF_H$**.

Fig. 2.1 Memory Space of MB89630 Series of Microcontrollers

(1) I/O area

This area is where various resources such as control and data registers are located. The memory map for the I/O area is given in Appendix 1.

(2) RAM area

This area is where the static RAM is located. Addresses from **0100_H** to **$01FF_H$** are also used as the general-purpose register area.

(3) External area

When data is read and written from and to this area with the external-bus function specified, the external de vice is accessed via ports 0, 1, and 2. Examples of expanding the external memory and peripheral resources by using the external-bus pins are described in 3.4 Memory Access Modes.

(4) ROM area

This area is where the internal ROM is located. Addresses from **$FFC0_H$** to **$FFFF_H$** are also used for the tables of interrupt and reset vectors and vector-call instructions. Table 2-1 shows the correspondence between each interrupt number or reset and the table addresses to be referenced for the MB89630 series of microcon trollers.

Table 2.1 Table of Reset and Interrupt Vectors

	Table address	
	Upper data	Lower data
CALLV #0	$FFC0_H$	$FFC1_H$
CALLV #1	$FFC2_H$	$FFC3_H$
CALLV #2	$FFC4_H$	$FFC5_H$
CALLV #3	$FFC6_H$	$FFC7_H$
CALLV #4	$FFC8_H$	$FFC9_H$
CALLV #5	$FFCA_H$	$FFCB_H$
CALLV #6	$FFCC_H$	$FFCD_H$
CALLV #7	$FFCE_H$	$FFCF_H$

	Table address	
	Upper data	Lower data
Interrupt #11	$FFE4_H$	$FFE5_H$
Interrupt #10	$FFE6_H$	$FFE7_H$
Interrupt #9	$FFE8_H$	$FFE9_H$
Interrupt #8	$FFEA_H$	$FFEB_H$
Interrupt #7	$FFEC_H$	$FFED_H$
Interrupt #6	$FFEE_H$	$FFEF_H$
Interrupt #5	$FFF0_H$	$FFF1_H$
Interrupt #4	$FFF2_H$	$FFF3_H$
Interrupt #3	$FFF4_H$	$FFF5_H$
Interrupt #2	$FFF6_H$	$FFF7_H$
Interrupt #1	$FFF8_H$	$FFF9_H$
Interrupt #0	$FFFA_H$	$FFFB_H$
Reset mode	. . . . .	$FFFD_H$
Reset vector	$FFFE_H$	$FFFF_H$

Note: $FFFC_H$ is already reserved.

2.1.2 Arrangement of 16-bit Data in Memory

When the MB89630 series of microcontrollers handle 16-bit data, the data written at the lower address is treated as the upper data and that written at the next address is treated as the lower data as shown in Figure 2.2.

Fig. 2.2 Arrangement of 16-bit Data in Memory

This is the same as when 16 bits are specified by the operand during execution of an instruction. Bits closer to the OP code are treated as the upper byte and those next to it are treated as the lower byte. This is also the same when the memory address or 16-bit immediate data is specified by the operand.

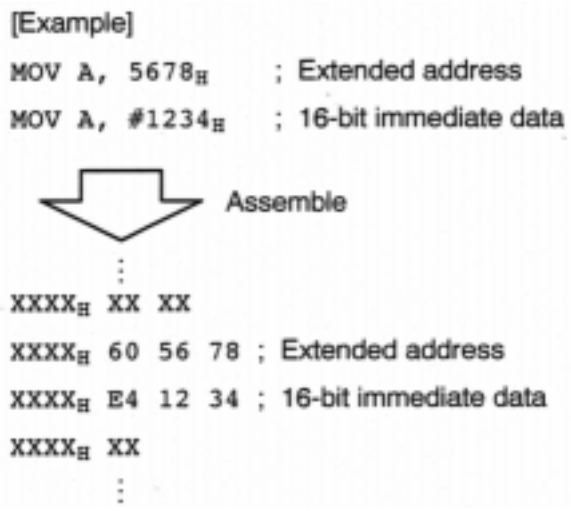


Fig. 2.3 Arrangement of 16-bit Data during Execution of Instruction

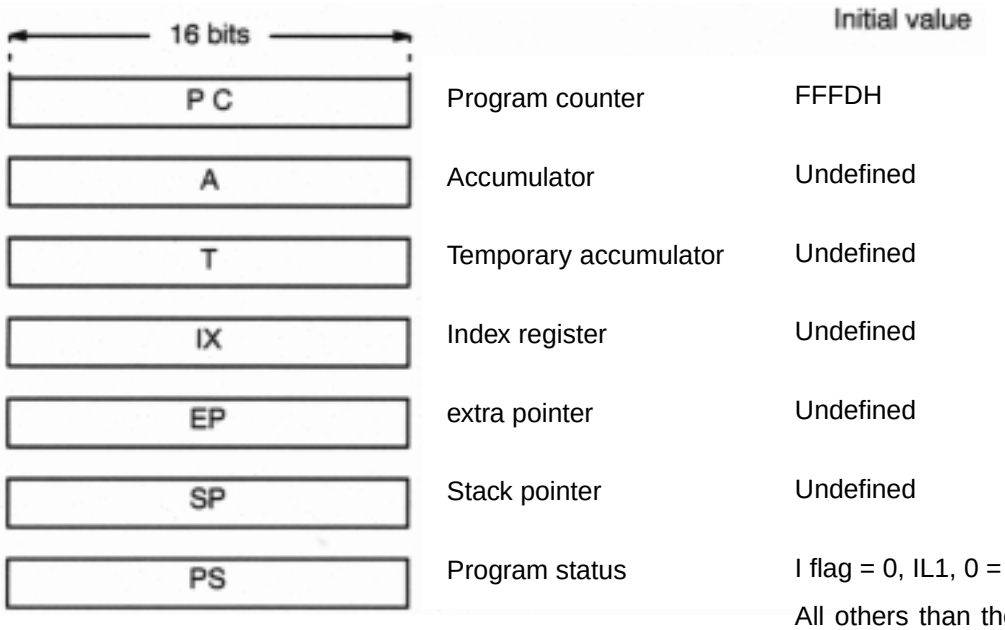
Data saved in the stack by an interrupt is also treated in the same manner.

2.1.3 Internal Registers in CPU

The MB89630 series of microcontrollers have dedicated registers in the CPU, and general-purpose registers in memory.

<Dedicated registers>

- Program counter (PC) ..... 16-bit long register indicating location where instructions stored
- Accumulator (A) ..... 16-bit long register where results of operations stored temporarily; the lower byte is used to execute 8-bit data processing instructions.
- Temporary accumulator (T) ... 16-bit long register; the operations are performed between this register and the accumulator. The lower one byte is used to execute 8-bit data processing instructions
- Stack pointer (SP) ..... 16-bit long register indicating stack area
- Processor status (PS) ..... 16-bit long register where register pointers and condition codes stored
- Index register (IX)..... 16-bit long register for index modification
- Extra pointer (EP)..... 16-bit long register for memory addressing



The 16 bits of the program status (PS) can be divided into 8 upper bits for a register bank pointer (RP) and 8 lower bits for a condition code register (CCR). (See Figure 2.4.)

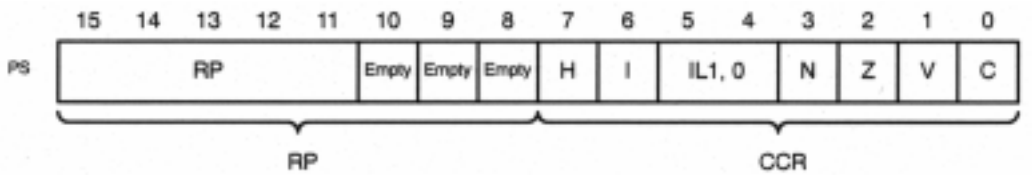


Fig. 2.4 Structure of Program Status

The RP indicates the address of the current register bank and the contents of the RP; the real addresses are translated as shown in Figure 2.5.

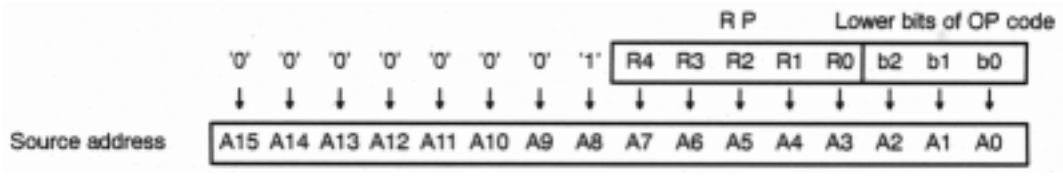


Fig. 2.5 Rule for Translating Real Addresses at General-purpose Register Area

The CCR has bits indicating the results of operations and transfer data contents, and bits controlling the CPU operation when an interrupt occurs.

- H-flag: .....H-flag is set when a carry or a borrow out of bit 3 into bit 4 is generated as a result of operations; it is cleared in other cases. This flag is used for decimal-correction instructions.
- I-flag:.....An interrupt is enabled when this flag is 1 and is disabled when it is 0. The I-flag is 0 at reset.
- IL1 and IL0:...These bits indicate the level of the currently-enabled interrupt. The CPU executes interrupt processing only when an interrupt with a value smaller than the value indicated by this bit is requested.

IL1	IL0	Interrupt level	High and low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = No interrupt

- N-flag: .....The N-flag is set when the most significant bit is 1 as a result of operations; it is cleared when the MSB is 0.
- Z-flag:.....Z-flag is set when the bit is 0 as a result of operations; it is cleared in other cases.
- V-flag:.....V-flag is set when a two's complement overflow occurs as a result of operations; it is reset when an overflow does not occur.
- C-flag: .....C-flag is set when a carry or a borrow out of bit 7 is generated as a result of operations; it is cleared in other cases. When the shift instruction is executed, the value of the C-flag is shifted out.

<General-purpose registers>

General-purpose registers are 8-bit long registers for storing data.

The 8-bit long general-purpose registers are in the register banks in memory. One bank has eight registers and up to 32 banks are available for the MB89630 series of microcontrollers. The register bank pointer (RP) indicates the currently-used bank.

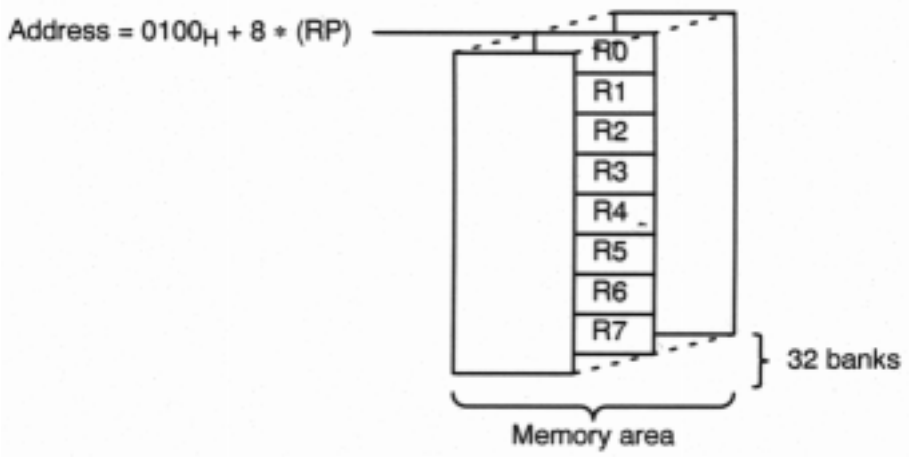


Fig. 2.6 Register Bank Configuration

2.1.4 Operation Modes and External Bus Operation

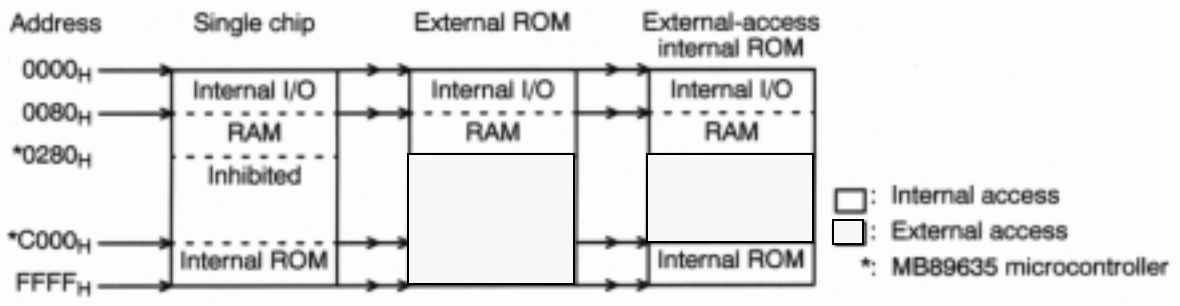
The MB89630 series of microcontrollers have the following three operation modes.

(1) Single-chip mode

(2) External-ROM mode

(3) External-access internal-ROM mode

The memory map for each mode is as follows:



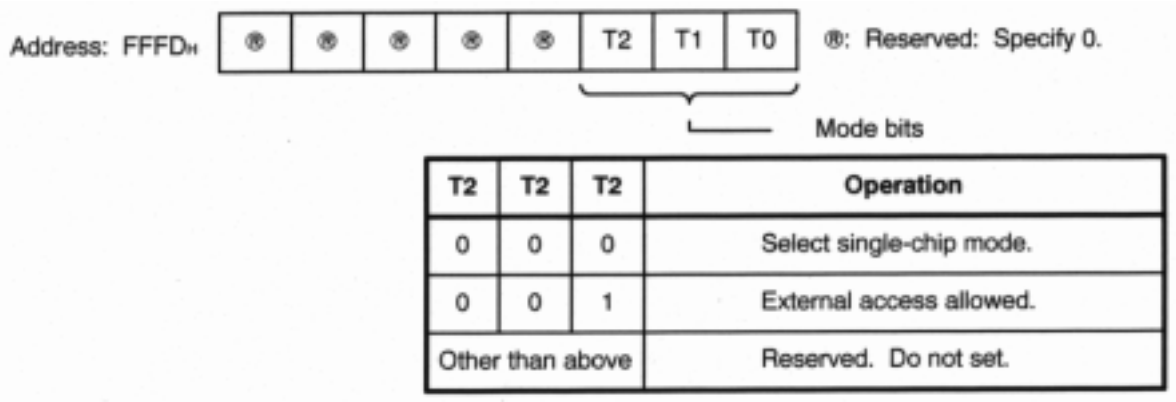
*: MB89635 Address values. For the addresses of each product in the MB89630 series, see ***2.1.1***.

Fig. 2.7 Memory Maps in Various Modes

The mode that the device enters depends on the states of the device-mode pins and the contents of the mode data fetched during the reset sequence. The relationship between the states and operations of the device-mode pins is shown below.

MOD1	MOD0	Description
0	0	Reset vectors are read from the internal ROM. The operation mode is determined according to the modde data contents.
0	1	Reset vectors are read from the external ROM. The external access functions.
1	0	Reserved for future expansion and testing.
1	1	Write mode for products containing EPROM.

The following functions are selected according to the mode-data setting conditions.



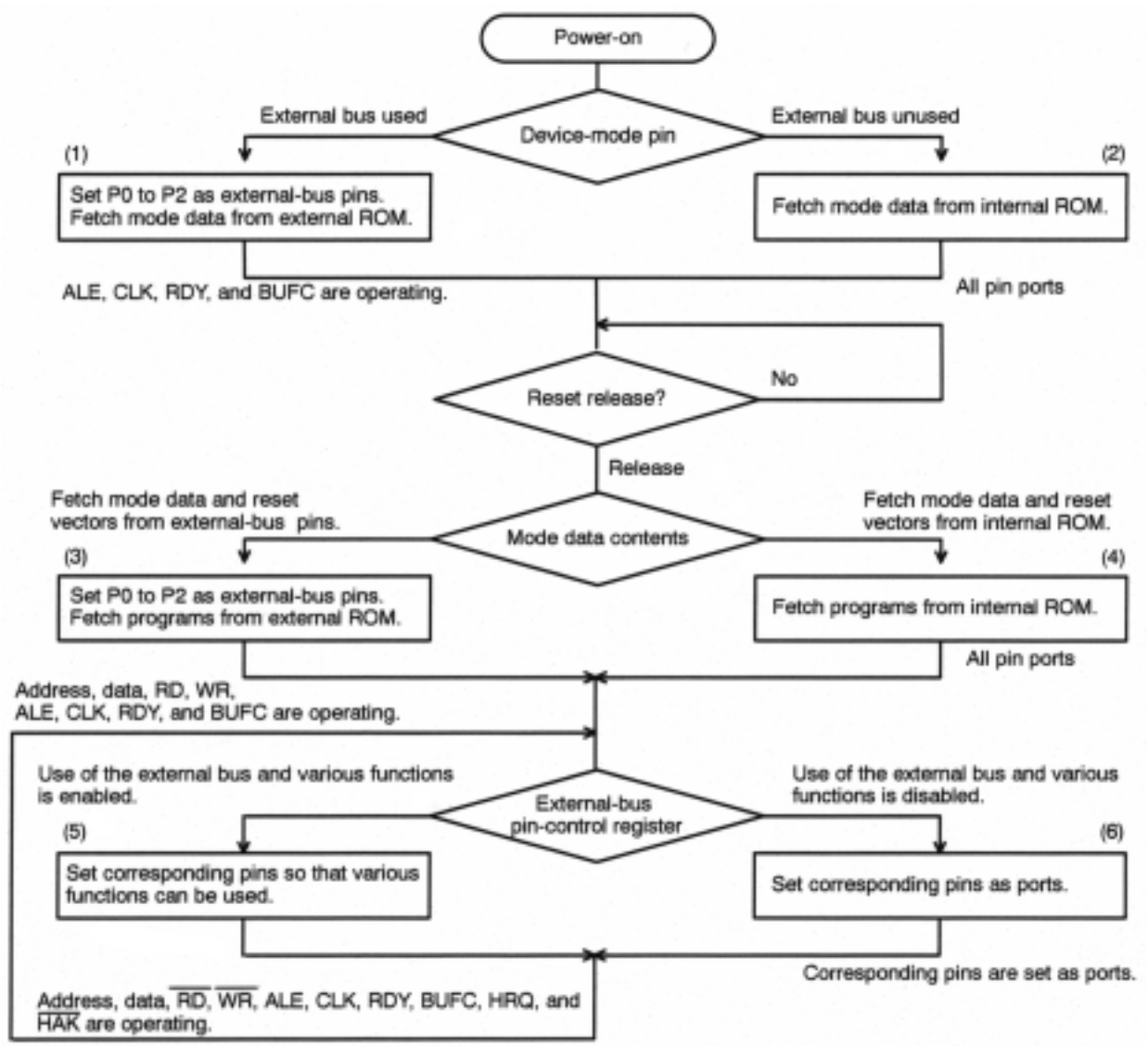
T2	T2	T2	Operation
0	0	0	Select single-chip mode.
0	0	1	External access allowed.
Other than above			Reserved. Do not set.

Note: Do not select the single-chip mode with the externally-fetched mode data.

As shown in the flowchart below, each mode is set according to the status of the device-mode pins and the contents of the mode data fetched during the reset sequence.

Setting procedure	Mode selected	Mode pin	Mode data
(2)→(4)→(6)	Single-chip mode	00	XXXXX000
(1)→(3)→ *(5) or (6)	External-ROM mode	01	XXXXX001
(2)→(4)→ *(5) or (6)	External-access internal-ROM mode	00	XXXXX001

* Depends on whether Ready or Hold function used



When the external-bus function is used, the following pins become active at default.

A, AD, $\overline{RD}$, $\overline{WR}$, ALE, CLK, RDY, and BUFC

The external-bus pin-control register (BCTR) is used to switch the function of the pin controlling the external bus for port 2 in the external-bus mode. When either of the bits is set to 0, the pin corresponding to the bit serves as the port. In the single-chip mode, the contents of both bits are ignored and all 8 bits of port 2 serve as parallel ports. Access to this register is not allowed in modes other than the external-bus mode. The structure of the BCTR is as follows:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0005_H	—	—	—	—	—	—	HLD	BUF	XXXX XX01$_B$
							(W)	(W)	

[Bit 1] HLD: Hold-enable bit. Bit 1 is used to enable the holding operation.

0	In external-bus mode, P21 and P22 serve as ports.
1	In external-bus mode, P21 used for $\overline{HAK}$ output and P22 used for HRQ input.

[Bit 0] BUF: BUFC-operation enable bit. Bit 0 is used to enable the operation of the BUFC pin.

0	In external-bus mode, P20 serves as port.
1	In external-bus mode, P20 used for BUFC output.

The states of the bus pins in each mode are as follows:

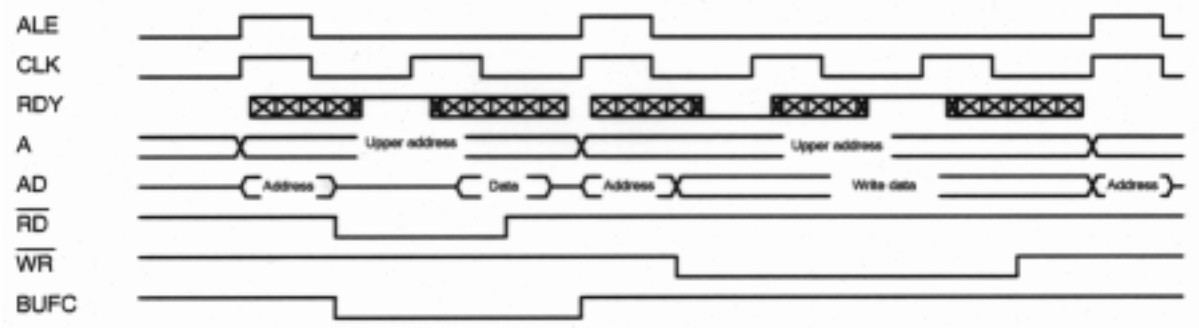
Pin name	Shingle chip	External Access
P00 to P07	P00 to P07	AD7 to AD0
P17	P17	A15
P16	P16	A14
P15	P15	A13
P14	P14	A12
P13	P13	A11
P12	P12	A10
P11	P11	A09
P10	P10	A08
P27	P27	ALE
P26	P26	$\overline{RD}$
P25	P25	$\overline{WR}$
P24	P24	CLK
P23	P23	RDY
P22	P22	HRQ
P21	P21	$\overline{HAK}$
P20	P20	$\overline{BUFC}$

Meaning of each signal

AD0 to AD7: Address/data multiplex bus
A08 to A15: Address bus
ALE: Address-latch enable
$\overline{RD}$: Read strobe (Active at L)
$\overline{WR}$: Write strobe (Active at L)
CLK: Clock output
RDY: Bus-ready input (Wait at L)
HRQ: Hold request
$\overline{HAK}$: Hold-acknowledge output (Active at L)
BUFC: Buffer control

Note: $\overline{RD}$, $\overline{WR}$, and $\overline{BUFC}$ are not output when the address indicates the internal area.

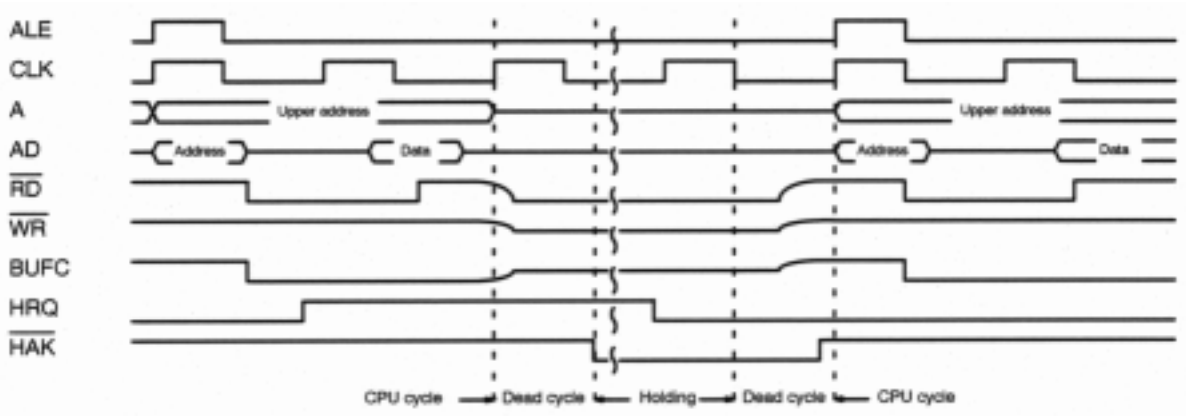
The timing concept for external access is shown below. Refer to the AC standard for details.



Note: The read cycle of the RDY signal is prolonged in the same manner as the write cycle.

RDY is an signal to execute the Ready function. When a Low level is input for RDY, the bus cycle is prolonged in CLK cycle. Fetching is carried out near the rising edge of the CLK signal. To prolong the bus cycle, set the RDY signal to Low before the rising edge of the CLK signal. When the ready function is not used in the external bus mode, the RDY pin should be pulled up.

The HRQ and $\overline{HAK}$ signals are used for the hold function. To obtain the external bus, set the HRQ signal to High. After that, the CPU recognizes the bus request between instructions to stop operation and sets the $\overline{HAK}$ signal to Low after waiting one half cycle. It signals the outside that the bus is open in this way. When another device terminates use of the bus, set the HRQ signal to Low to notify the CPU. When the CPU detects the Low level of the HRQ signal, it sets the $\overline{HAK}$ signal to High and starts using the external bus after waiting one half cycle. The hold function timing concept is diagram shown below.



2.1.5 Clock Control Block

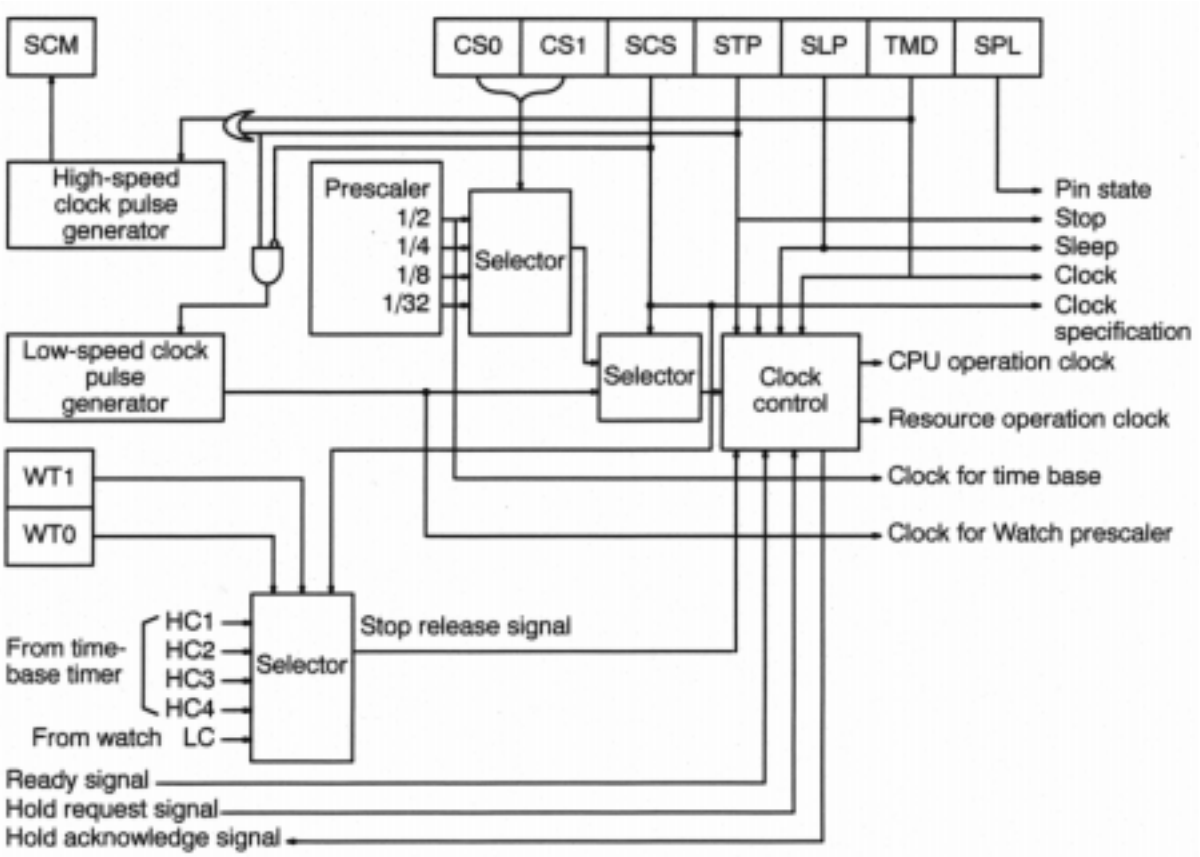
This block controls the standby operation, oscillation stabilization time, software reset, and clock switching.

(1) Register list

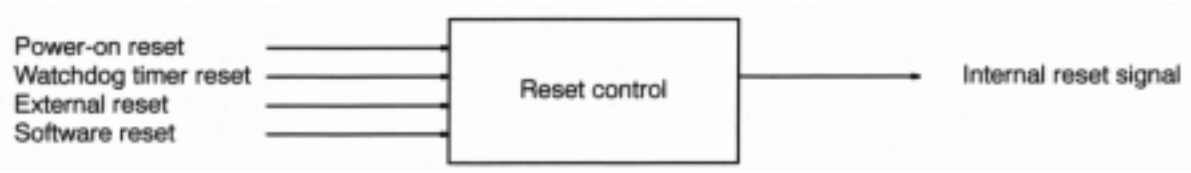
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Address: 0007_H	SCM	—	—	WT1	WT0	SCS	CS1	CS0	System clock control register (SYCC)
Address: 0008_H	STP	SLP	SPL	RST	TMD	—	—	—	Standby control register (STBC)

(2) Block diagram

(a) Machine clock control section



(b) Reset control section



(3) Description of registers

(a) STBC (Standby-conrol register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0008_H	STP	SLP	SPL	RST	TMD	—	—	—	$0001\ 0XXX_B$
	(W)	(W)	(R/W)	(W)	(W)				

[Bit 7] STP: Stop bit

Bit 7 specifies switching to the stop mode.

0	No operation
1	Stop mode

This bit is cleared at reset or stop cancellation.

0 is always read when this bit is read.

[Bit 6] SLP: Sleep bit

Bit 6 specifies switching to the sleep mode.

0	No operation
1	Sleep mode

This bit is cleared at reset or stop cancellation.

0 is always read when this bit is read.

[Bit 5] SPL: Pin state specifying bit

Bit 5 specifies the external pin state in the watch or stop mode.

When the pins for which "Pull-up resistor provided" is specified in the mask option enter the stop mode with SPL = 1, they are pulled up rather than having high impedance.

0	A 4-instruction-cycle reset signal is generated.
1	High impedance

This bit is cleared at resetting.

[Bit 4] RST: Software reset bit

Bit 4 resets the software.

0	Generate 4-cycle reset signal (6.4 μs at 10 MHz)
1	No operation

1 is always read when this bit is read.

If a software reset is performed during operation in a submode, one oscillation stabilization period is required to switch to the main mode. Therefore, a reset signal is output during the oscillation stabilization period.

[Bit 3] TMD: Watch bit

Bit 3 specifies switching to the watch mode.

0	No operation
1	Watch mode

Writing at this bit is possible only in the submode (SCS = 0). 0 is always read when this bit is read. This bit is cleared at an interrupt request or reset.

(b) System clock control register (SYCC)

Address: 0007_H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
SCM	—	—	WT1	WT0	SCS	CS1	CS0	X--M M100$_B$
(R)			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] SCM: System clock monitor bit

Bit 7 checks whether the current system clock is the main clock or subclock.

0	Subclock (Main clock is stopping or oscillation of main clock stable)
1	Main clock

[Bits 4 and 3] WT1 and WT0: Oscillation stabilization time select bits

Bits 4 and 3 select the oscillation stabilization wait time of the main clock.

WT1	WT0	Oscillation stabilization time	Oscillation stabilization time at original oscillation of 10 MHz
1	1	Approximate 2^{18}/fch	Approximate 26.2 (ms)
1	0	Approximate 2^{17}/fch	Approximate 13.1 (ms)
0	1	Approximate 2^{14}/fch	Approximate 1.6 (ms)
0	0	Approximate 2^4/fch	Approximate 0 (ms)

fch: Oscillation frequency of main clock

If the main mode is specified by the system clock select bit (SCS), the mode switches to main mode after the selected wait time has elapsed.

The initial value of this bit is determined by the mask option. Do not rewrite this bit during the oscillation stabilization period nor rewrite it concurrently with switching from low speed to high speed.

The oscillation stabilization time of the main clock is generated by dividing down the frequency of the main clock. Since the oscillation frequency is unstable immediately after oscillation starts, use the above table.

[Bit 2] SCS: System clock select bit

Bit 2 selects the system clock mode.

0	Selects subclock (32 kHz) mode
1	Selects main clock (10 MHz) mode

[Bits 1 and 0] CS1 and CS0: System clock select bits

If the main mode is specified by the system clock select bit (SCS), the system clock is as given in the table below.

CS1	CS0	Instruction cycle	Minimum instruction execution time at 10 MHz
0	0	64/fch	6.4 (μs)
0	1	16/fch	1.6 (μs)
1	0	8/fch	0.8 (μs)
1	1	4/fch	0.4 (μs)

fch: frequency of main clock

(4) Description of operation

(a) Low-power consumption mode

This chip has three operation modes. The sleep mode, and stop mode in the table below reduce the power consumption. In the main mode, four system clocks can be selected according to the system condition to minimize power consumption.

Table 2.2 Operating State of Low-power Consumption Modes

Main operation mode	(CS1, CS0)	Operation mode	Clock pulse generation		Each operating clock pulse (10 MHz main clock)				Wake-up source in each mode
			Main	Sub	CPU	Time-base timer	Each resource	Clock	
Main mode	(1, 1)	RUN SLEEP STOP	Oscillates Stops	Oscillates	5 MHz Stops	5 MHz Stops	5 MHz Stops	32 kHz	Various interrupt requests External interrupt
	(1, 0)	RUN SLEEP STOP	Oscillates Stops	Oscillates	2.5 MHz Stops	5 MHz Stops	2.5 MHz Stops	32 kHz	Various interrupt requests External interrupt
	(0, 1)	RUN SLEEP STOP	Oscillates Stops	Oscillates	1.25 MHz Stops	5 MHz Stops	1.25 MHz Stops	32 kHz	Various interrupt requests External interrupt
	(0 ,0)	RUN SLEEP STOP	Oscillates Stops	Oscillates	312.5 kHz Stops	5 MHz Stops	312.5 kHz Stops	32 kHz	Various interrupt requests External interrupt
Submode	—	RUN SLEEP STOP	Stops	Oscillates Stops	32 kHz Stops	Stops	32 kHz Stops	32 kHz Stops	Various interrupt requests External interrupt
CLOCK mode			Stops	Oscillates	Stops	Stops	Stops	32 kHz	Watch External interrupt

- The submode stops oscillation of the main clock.
- The SLEEP mode stops only the operating clock pulse of the CPU; other operations are continued.
- The WATCH mode stops the functions of all chips other than the special resources.
- The STOP mode stops the oscillation. Data can be held with the lowest power consumption in this mode.

[1] WATCH mode

- Switching to WATCH mode
  - Writing 1 at the TMD bit (bit 3) of the STBC register switches the mode to WATCH mode. Writing is invalid if 1 is set at the SCS bit (bit 2) of the SYCC register.
  - The WATCH mode stops all chip functions except the watch prescaler, external interrupt, and wake-up functions. Therefore, data can be held with the lowest power consumption.
  - The input/output pins and output pins during the WATCH mode can be controlled by the SPL bit of the STBC register so that they are held in the state immediately before entering the WATCH mode or so that they enter the high-impedance state.
  - If an interrupt is requested when 1 is written at the TMD bit , instruction execution continues without switching to the WATCH mode.
  - In the WATCH mode, the values of registers and RAM immediately before entering the WATCH mode are held.
- Canceling WATCH mode
  - The WATCH mode is canceled by inputting the reset signal and requesting an interrupt.
  - When the reset signal is input during the WATCH mode, the CPU is switched to the reset state and the WATCH mode is canceled.
  - When an interrupt higher than level 11 is requested from a resource during the WATCH mode, the WATCH mode is canceled.
  - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the WATCH mode.
  - If the WATCH mode is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization wait state. Therefore, the reset sequence is not executed unless the oscillation stabi lization time is elapsed. The oscillation stabilization time will be that of the main clock selected by the WT1 and WT0 bits. However, when Power-on Reset is not specified by the mask option, the CPU is not switched to the oscillation stabilization wait state, even if the WATCH mode is canceled by inputting the reset signal.

[2] SLEEP mode

- Switching to SLEEP mode
  - Writing 1 at the SLP bit (bit 6) of the STBC register switches the mode to SLEEP mode.
  - The SLEEP mode stops the CPU operating clock pulse; only the CPU stops and the resources continue to operate.
  - If an interrupt is requested when 1 is written at the SLP bit (bit 6), instruction execution continues without switching to the SLEEP mode. In the SLEEP mode,the values of registers and RAM im mediately before entering the SLEEP mode are held.
- Canceling SLEEP mode
  - The SLEEP mode is canceled by inputting the reset signal and requesting an interrupt.
  - When the reset signal is input during the SLEEP mode, the CPU is switched to the reset state and the SLEEP mode is canceled.
  - When an interrupt higher than level 11 is requested from a resource during the SLEEP mode, the SLEEP mode is canceled.
  - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the SLEEP mode.

[3] STOP mode

- Switching to STOP mode
  - Writing 1 at the STP bit (bit 7) of the STBC register switches the mode to STOP mode.
  - The STOP mode varies when the main clock is operating and when the subclock is operating.

    When the main clock is operating: The main clock stops but the subclock does not stop. All chip functions except the watch function stop.

    When subclock is operating: Both the main clock and subclock stop. All chip functions stop.
  - -The input/output pins and output pins during the STOP mode can be controlled by the SPL bit (bit 5) of the STBC register so that they are held in the state immediately before entering the STOP mode, or so that they enter in the high-impedance state.
  - If an interrupt is requested when 1 is written at the STP bit (bit 7), instruction execution continues without switching to the STOP mode.
  - In the STOP mode, the values of registers and RAM immediately before entering the STOP mode are held.

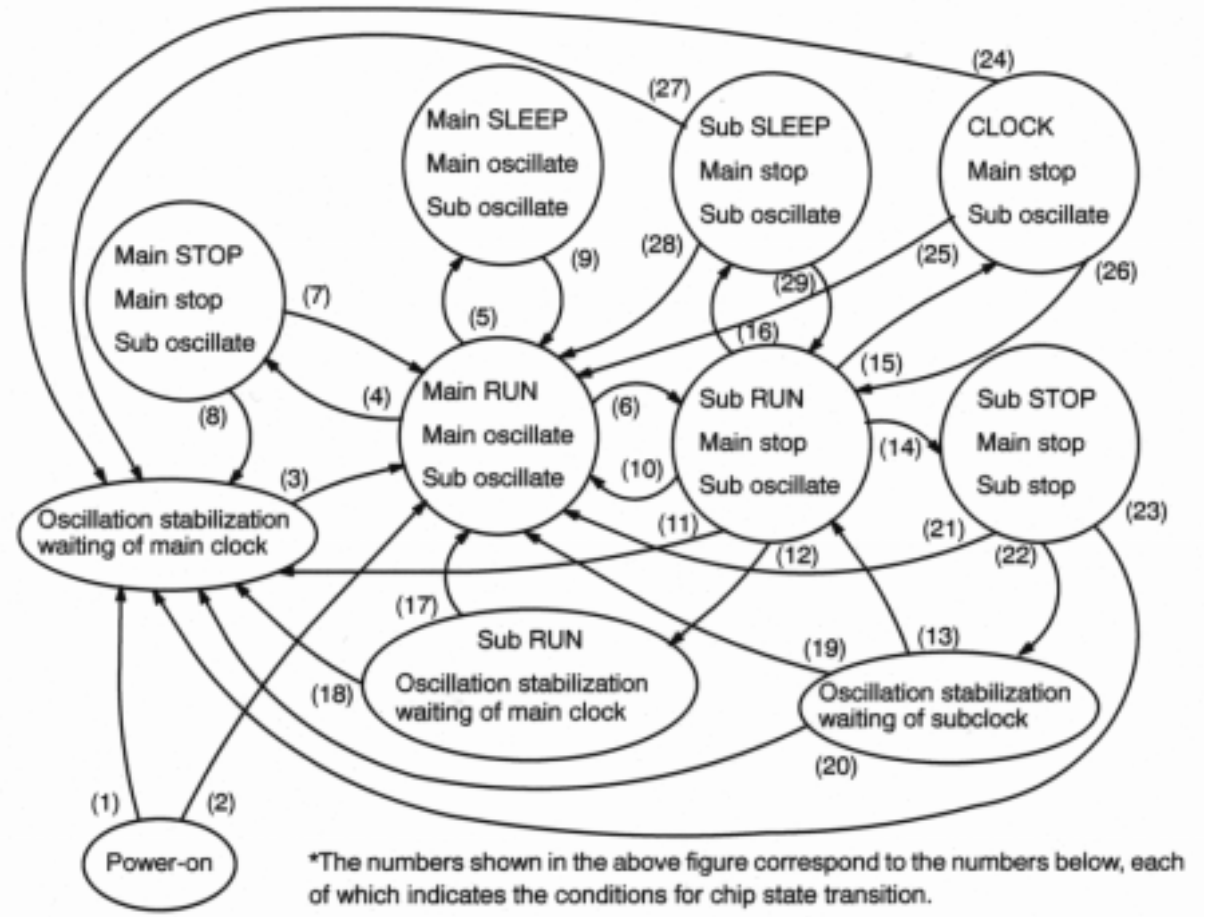
- Canceling STOP mode
  - The STOP mode is canceled either by inputting the reset signal or by requesting an interrupt.
  - When the reset signal is input during the STOP mode, the CPU is switched to the reset state and the STOP mode is canceled.
  - When an interrupt higher than level 11 is requested from the external interrupt circuit during the STOP mode, the STOP mode is canceled.
  - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the STOP mode.
  - Four oscillation stabilization times of the main clock can be selected by the WT1 and WT0 bits. The oscillation stabilization time of the subclock is fixed (at 2^{15}/fcl -- fcl: frequency of subclock).
  - If the STOP mode is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization wait state. Therefore, the reset sequence is not executed unless the oscillation stabi lization time is elapsed. The oscillation stabilization time corresponds to the oscillation stabiliza tion time of the main clock selected by the WT1 and WT0 bits. However, when Power-on Reset is not specified by the mask option, the CPU is not switched to the oscillation stabilization wait state even if the STOP mode is canceled by inputting the reset signal.

[4] Setting low power consumption mode

STBC Register			Mode
STP (Bit 7)	SLP (Bit 6)	TMD (Bit 3)	
0	0	0	Normal
0	0	1	WATCH
0	1	0	SLEEP
1	0	0	STOP
1	×	×	Disable

Note: When the mode is switched from the subclock mode to the main clock mode, do not set the stop, sleep, and watch modes. If the SCS bit of the SYCC register is rewritten from 0 to 1, set the above modes after the SCM bit of the SYCC register has been set to 1.

(b) State transition diagram



*The numbers shown in the above figure correspond to the numbers below, each of which indicates the conditions for chip state transition.

(1) When power-on reset option is selected
(2) When power-on reset option is not selected
(3) After oscillation stabilized
(4) Set STP bit to 1.
(5) Set SLP bit to 1.
(6) Set SCS bit to 0.
(7) External reset when power-on reset option not selected
(8) External reset or interrupt when power-on reset option selected
(9) External reset or interrupt
(10) External reset when power-on reset option not selected
(11) External reset or other reset when power-on reset option selected
(12) Set SCS bit to 1.
(13) After oscillation stabilized
(14) Set STP bit to 1.
(15) Set TMD bit to 1.
(16) Set SLP bit to 1.
(17) External reset after oscillation stabilized or when power-on reset option not selected
(18) External reset or other reset when power-on reset option selected
(19) External reset after oscillation is stabilized or when power-on reset option not selected
(20) External reset when power-on reset option selected
(21) External reset when power-on reset option not selected
(22) Interrupt
(23) External reset when power-on reset option selected
(24) External reset when power-on reset option selected
(25) External reset when power-on reset option not selected
(26) Interrupt
(27) External reset when power-on reset option selected
(28) External reset when power-on reset option not selected
(29) Interrupt

(d) Reset

There are four types of resets as shown in Table 2-3.

Table 2.3 Sources of Reset

Reset name	Description
External-pin reset	Sets external-reset pin to Low
Software reset	Writes 0 at RST (bit 4) of STBC
Watchdog reset	Overflows watchdog timer
Power-on reset*	Turns power on

*: "Power-on reset provided" is specified in the mask option.

When the power-on reset and reset during the stop mode are used, the oscillation stabilization time is needed after the oscillator operates. The time-base timer or watch prescaler controls this stabilization time. Consequently, the operation does not start immediately even after canceling the reset.

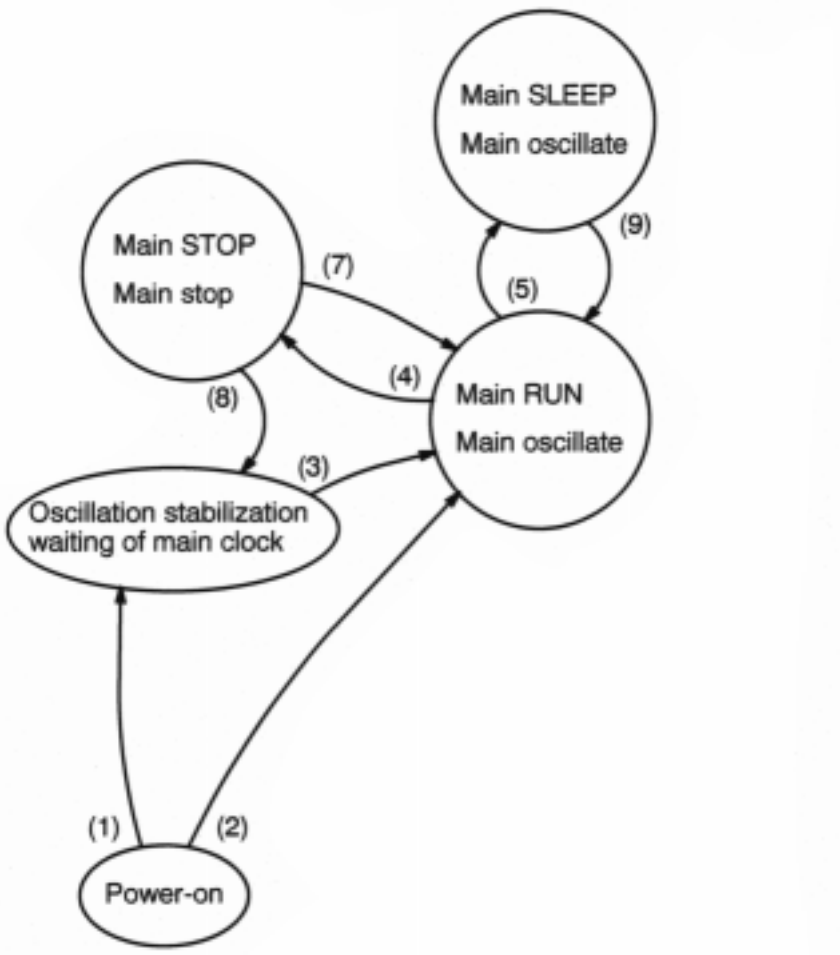
However, if Power-on Reset Disabled is selected by the mask option, no oscillation stabilization time is required in any state after external pins have been released from the reset.

Note: If Power-on Reset Disabled is selected, the RST pin must be kept Low until the oscillation stabilization time selected by the option has elapsed after power on.

(5) Single clock

The single clock module can be selected by the mask option. In the single clock operation, the functions are the same as those of the double clock module except that the subclock mode cannot be set. In the single clock operation, P72/X0A/INT2 and P73/X1A/INT3 serve as external interrupt pins.

(a) State transition diagram

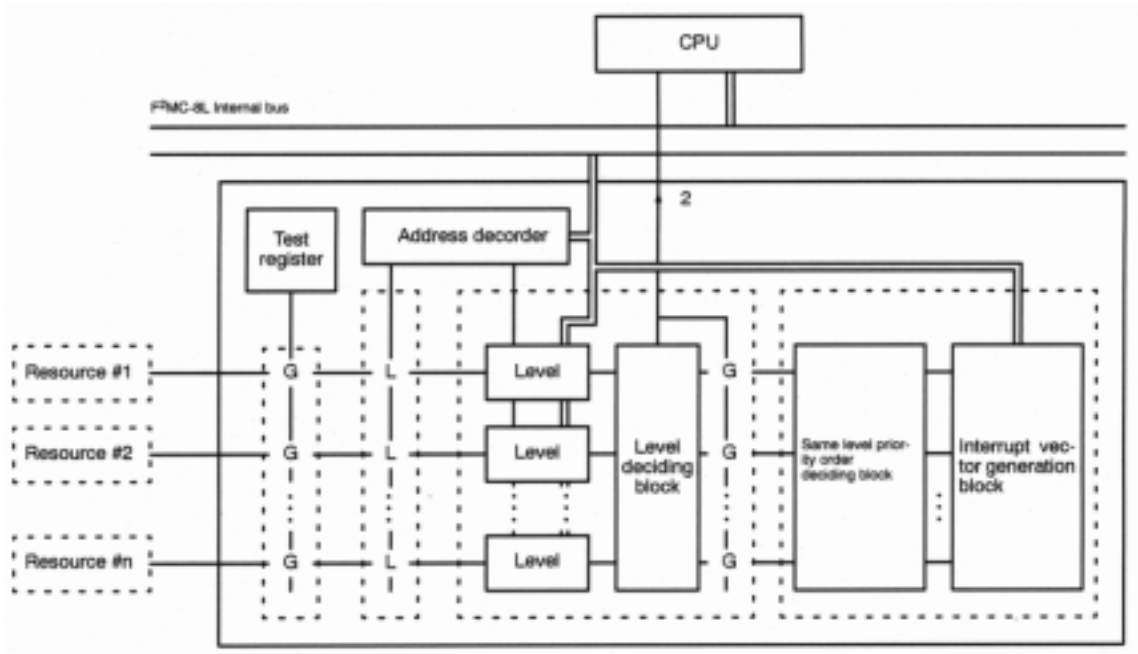


(1) When power-on reset option selected
(2) When power-on reset option not selected
(3) After oscillation stabilized
(4) Set STP bit to 1.
(5) Set SLP bit to 1.
(7) External reset when power-on reset option not selected
(8) External reset or interrupt when power-on reset option selected
(9) External reset or interrupt

2.1.6 Interrupt Controller

The interrupt controller for the F^{2}MC-8L is located between the CPU and each resource. This controller receives interrupt requests from the resources, assigns priority to them, and transfers the priority to the CPU; it also decides the priority of same-level interrupts.

(1) Block diagram



(a) Register list

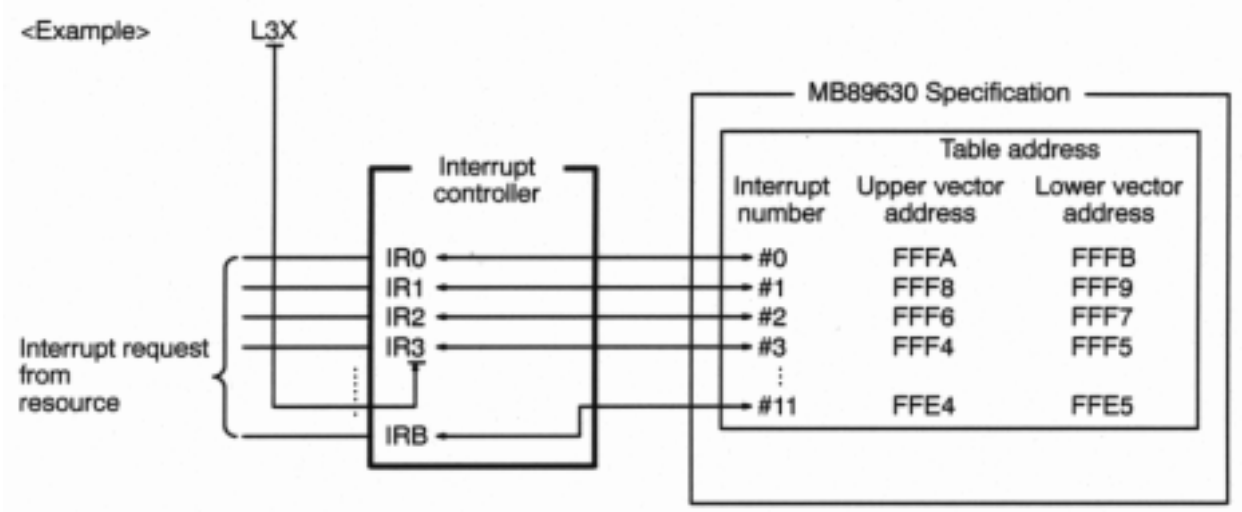
Address	7	6	5	4	3	2	1	0	Name	[Abbreviation]	(Initial value)
007C H	L31	L30	L21	L20	L11	L10	L01	L00	Interrupt-level register #1	[ILR1]	(1111 1111)
007D H	L71	L70	L61	L60	L51	L50	L41	L40	Interrupt-level register #2	[ILR2]	(1111 1111)
	LB1	LB0	LA1	LA0	L91	L90	L81	L80	Interrupt-level register #3	[ILR3]	(1111 1111)
007E H											

(2) Description of registers

- Interrupt level setting register (ILRX: Interrupt Level Register X)

	7	6	5	4	3	2	1	0		
1LR1	L31	L30	L21	L20	L11	L10	L01	L00	W	When reset (1111 1111)
1LR2	L71	L70	L61	L60	L51	L50	L41	L40	W	When reset (1111 1111)
1LR3	LB1	LB0	LA1	LA0	L91	L90	L81	L80	W	When reset (1111 1111)

The ILRX sets the interrupt level of each resource. The digits in the center of each bit correspond to the inter rupt numbers.



When an interrupt is requested from a resource, the interrupt controller transfers the interrupt level based on the value set at the 2 bits of the ILRX corresponding to the interrupt to the CPU. The relationship between the 2 bits of the ILRX and the required interrupt levels is as follows:

Lx1	Lx0	Required interrupt level
0	X	1
1	0	2
1	1	3 (None)

(3) Description of operation

- Interrupt functions

The MB89630 series of microcontrollers have 12 inputs for interrupt requests from each resource. The interrupt level is set by 2-bit registers corresponding to each input. When an interrupt is requested from a resource, the interrupt controller receives it and transfers the contents of the corresponding register to the CPU. The interrupt to the device is processed as follows:

1) An interrupt source is generated inside each resource.
2) If an interrupt is enabled, an interrupt request is output from each resource to the interrupt controller by referring to the interrupt-enable bit inside each resource.
3) After receiving this interrupt request, the interrupt controller determines the priority of simultaneously-requested interrupts and then transfers the interrupt level for the applicable interrupt to the CPU.
4) The CPU compares the interrupt level requested from the interrupt controller with the IL bit in the proc essor status register.
5) As a result of the comparison, if the priority of the interrupt level is higher than that of the current inter rupt processing level, the contents of the I-flag in the same processor status register are checked.
6) As a result of the check in step (5), if the I-flag is enabled for an interrupt, the contents of the IL bit are set to the required level. As soon as the currently-executing instruction is terminated, the CPU performs the interrupt processing and transfers control to the interrupt-processing routine.
7) When an interrupt source is cleared by software in the user's interrupt processing routine, the CPU terminates the interrupt processing.

Figure 2.8 outlines the interrupt operation for the MB89630 series of microcontrollers.

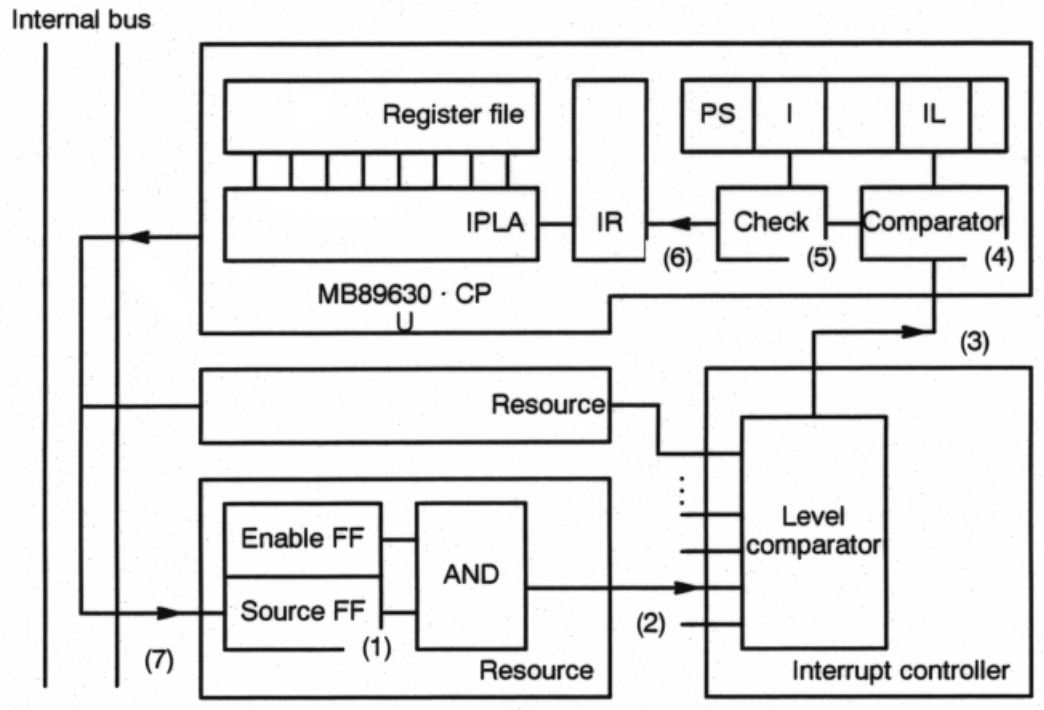


Fig. 2.8 Interrupt-processing Flowchart

2.2 RESOURCE FUNCTIONS

2.2.1 I/O Ports

- The MB89630 series of microcontrollers have eight parallel ports (53 ports). Ports 0, 1, and 3 serve as 8-bit I/O ports; ports 4 and 5 serve as 4-bit I/O ports; ports 2, and 6 serve as 8-bit output-only ports and port 7 serves as a 5-bit input-only port.
- Each port is also used as a resource (ports 3, 4, 5, and 7) and as external-bus pins (ports 0 to 2).

Table 2.4 List of Port Functions

Pin name	Input type	Output type	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P00 to P07	CMOS	CMOS push-pull	Parallel port 0	P07	P06	P05	P04	P03	P02	P01	P00
			External-address mode	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
P10 to P17	CMOS	CMOS push-pull	Parallel port 1	P17	P16	P15	P14	P13	P12	P11	P10
			External-address mode	A15	A14	A13	A12	A11	A10	A09	A08
P20 to P27	—	CMOS push-pull	Parallel port 2	P27	P26	P25	P24	P23	P22	P21	P20
			External-address mode	ALE	$\overline{RD}$	$\overline{WR}$	CLK	RDY	HRQ	$\overline{HAK}$	BUFC
P30 to P37	CMOS (Hysteresis)	CMOS push-pull /N-ch OD	Parallel port 3	P37	P36	P35	P34	P33	P32	P31	P30
			Resource	WTO	PWC	SI1	SO1	SCK1	UI1	UO1	UCK1
P40 to P43	CMOS (Hysteresis)	CMOS push-pull	Parallel port 4	—	—	—	—	P43	P42	P41	P40
			Resource	—	—	—	—	PTO1	UI2	UO2	UCK2
P50 to P53	—	N-ch open drain	Parallel port 5	—	—	—	—	P53	P52	P51	P50
			Resource	—	—	—	—	PTO2	—	BZ	ADST
P60 to P64	Analog comparator	N-ch open drain	Parallel port 6	P67	P66	P65	P64	P63	P62	P61	P60
			Resource	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
P70 to P74	CMOS (Hysteresis)	—	Parallel port 7	—	—	—	P74	P73	P72	P71	P70
			Resource	—	—	—	EC	INT3	INT2	INT1	INT0

Note: Output type of P33, P34, and P35 can be selected from the CMOS or N-ch open drain.
P70 and P71 serve as P70/INT0 and P71/INT1 at single clock operation and as X1A and X0A at double clock operation, respectively.

(1) Port registers

Table 2.5 Port Registers

Register name	Read/Write	Address	Initial value
Port-0 data register (PDR0)	R/W*1	0000_H	$XXXXXXXX_B$
Port-0 data direction register (DDR0)	W*1	0001_H	00000000_B
Port-1 data register (PDR1)	R/W*1	0002_H	$XXXXXXXX_B$
Port-1 data direction register (DDR1)	W*1	0003_H	00000000_B
Port-2 data register (PDR2)	R/W	0004_H	00000000_B
External-bus pin-control register (BCTR)	W*2	0005_H	$XXXXXX01_B$
Port-3 change register (CHG3)	R/W	$000C_H$	$XX000XXX_B$
Port-3 data register (PDR3)	R/W	$000D_H$	$XXXXXXXX_B$
Port-3 data direction register (DDR3)	W	$000E_H$	00000000_B
Port-4 data register (PDR4)	R/W	$000F_H$	$XXXXXXXX_B$
Port-4 data direction register (DDR 4)	W	0010_H	$XXXX0000_B$
Port-5 data register (PDR5)	R/W	0012_H	$XXXX1111_B$
Port-6 data register (PDR6)	R/W	0013_H	11111111_H
Port-7 data register (PDR7)	R	0014_H	$XXXXXXXX_H$

R/W : Read/write enabled
R : Read only
W : Write only
X : Undefined

*1 Data can be read and written only in the single-chip mode.

*2 Data can be written only when the external bus is extended.

*3 The bit manipulation instructions cannot be used for DDR0, DDR1, DDR3, and DDR4.

(2) Description of functions

P00 to P07 CMOS-type I/O ports (also used as external-address/data bus)

P10 to P17 CMOS-type I/O ports (also used as external-address bus)

- Operation when external bus extended

  See the description of the bus functions.

- Switching input and output

  These ports have a data-direction register (DDR) and port-data register (PDR) for each bit. Input and out put can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input. Note that the DDR is ineffective when the external bus is used.

- Operation for output port (DDR = 1)

  The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting con ditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

- Operation for input port (DDR = 0)

  When settings the input, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.

- State when reset

  In the single-chip mode (MOD0 = Low, MOD1 = Low), the DDR is initialized to 0 by resetting and the output impedance goes High at all bits. (Pins with activated pull-up resistors are in the pull-up state.) The PDR is not initialized by resetting. Therefore, set the value of the PDR before setting the DDR to output.

- State in stop mode

  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR. (Pins with activated pull-up resistors are in the pull-up state.)

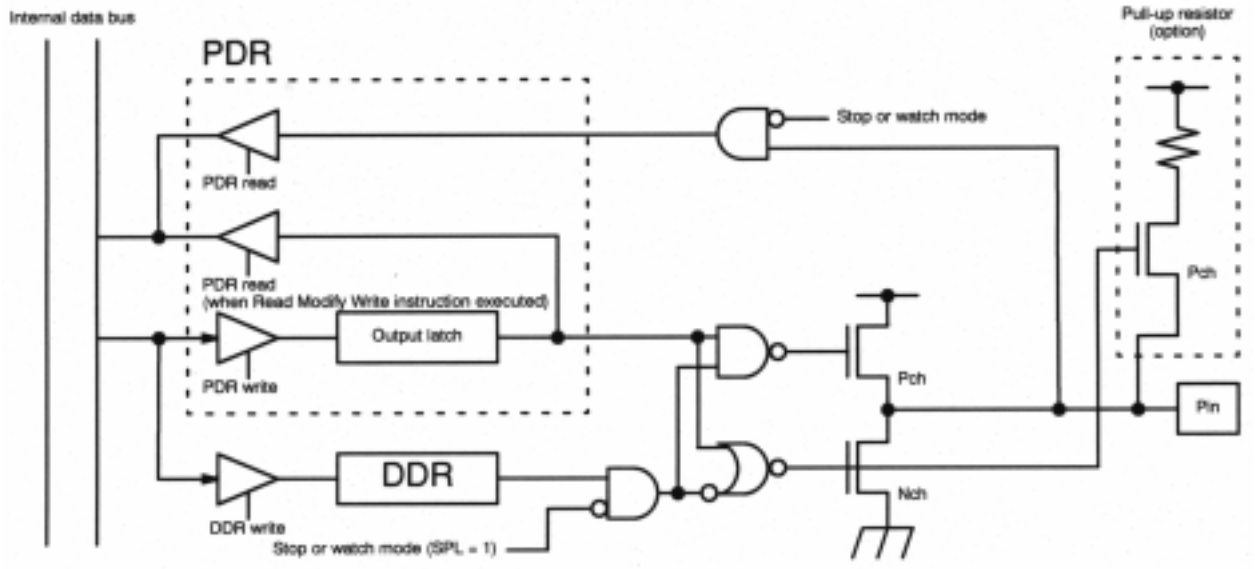


Fig. 2.9 Ports 0 and 1 (in Single-chip Mode)

P20 to P27 CMOS-type output-only ports (also used as external-bus control pin)

- Operation when external bus extended

  See the description of the bus functions.

- Operation for output port

  In the single-chip mode, the value written at the PDR is output to the pin. When the PDR is read, the con tents of the output latch are always read, so the bit- processing instruction is used even if the output level changes due to the load.

- State when reset

  In the single-chip mode, the pin impedance goes High at reset. As soon as a vector is fetched, output of the port is enabled and the port starts operation as the output port. Since the PDR is initialized to 0 by resetting, the Low level is output to the pin.

- State in stop mode

  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

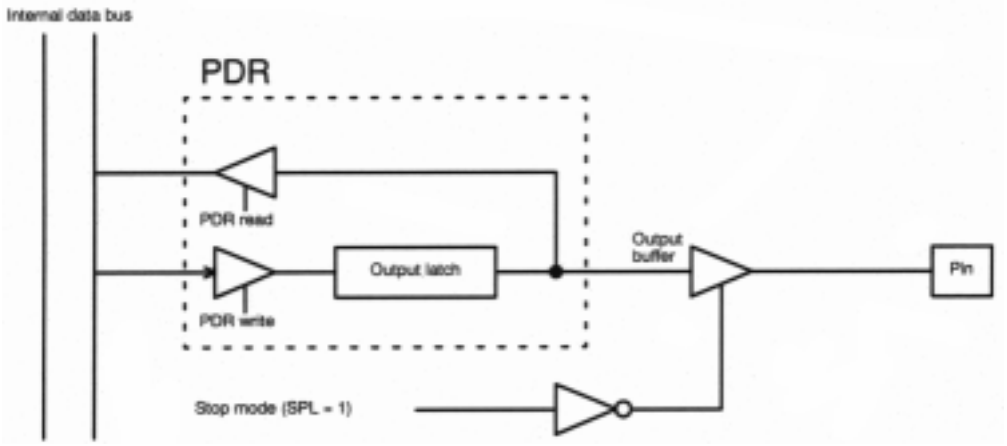


Fig. 2.10 Port 2 (in Single-chip Mode)

P30 to P37 CMOS-type I/O ports (also used as resource input/output)

- Switching input and output

  This port has a data-direction register (DDR) and a port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input. When the resource-output enable bit is enabled, the pin is set to output irre spective of the DDR setting conditions.

- Operation for output port (DDR = 1)

  The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting con ditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

  P33 to P35 can be selected from either CMOS (Bit X = 0) or N-ch open drain (Bit X = 1).

- Operation for input port (DDR = 0)

  When used as the input port, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.

- Operation for resource output

  When using as the resource output, setting is performed by the resource output- enable bit. (See the de scription of each resource.) If the output of each resource is enabled with the DDR set to 0, the port is set to output. Since the reading of the parallel port is effective even if the output of each resource is enabled, the output value of each resource can be read.

- Operation for resource input

  Input to the resource is irrelevant to the setting conditions of the DDR and resource. The value of the pin is always input to the port serving as the resource input. When using an external signal at the resource, set the DDR to input.

- State when reset

  When reset, the DDR and resource output-enable bit are initialized to 0 and the output impedance goes High at all bits. (Pins with activated pull-up resistors are in the pull-up state.) When reset, the PDR is unde fined. Therefore, set the value of the PDR before setting the DDR to output.

- State in stop mode

  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR. (Pins with activated pull-up resistors are in the pull-up state.)

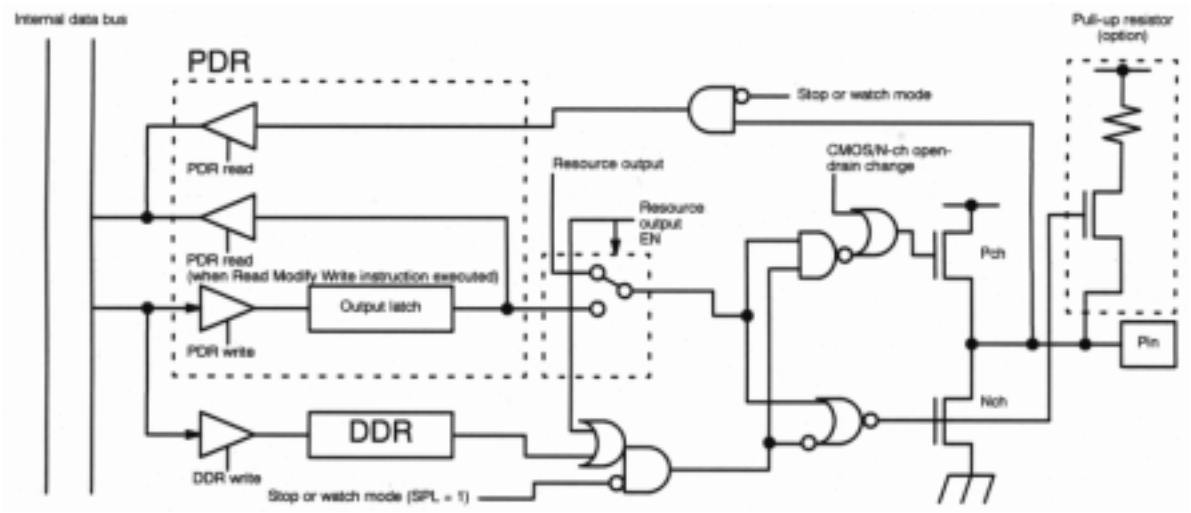


Fig. 2.11 Port 3

- CHG3: Port 3 change register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 000C$_H$	—	—	CG35 (R/W)	CG34 (R/W)	CG33 (R/W)	—	—	—	XX00 0XXX$_B$

CHG3 setting			Output type of port 3							
CG35	CG34	CG33	P37	P36	P35	P34	P33	P32	P31	P30
0	0	0	COMS		CMOS	CMOS	CMOS	COMS		
0	0	1			CMOS	CMOS	N-OD			
0	1	0			CMOS	N-OD	CMOS			
0	1	1			CMOS	N-OD	N-OD			
1	0	0			N-OD	CMOS	CMOS			
1	0	1			N-OD	CMOS	N-OD			
1	1	0			N-OD	N-OD	CMOS			
1	1	1			N-OD	N-OD	N-OD			

P40 to P43 CMOS-type I/O ports (also used as resource input/output)

- Switching input and output

  This port has a data-direction register (DDR) and a port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input. When the resource-output enable bit is enabled, the pin is set to output irre spective of the DDR setting conditions.

- Operation for output port (DDR = 1)

  The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting con ditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

- Operation for input port (DDR = 0)

  When used as the input port, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.

- Operation for resource output

  When using as the resource output, setting is performed by the resource output- enable bit. (See the de scription of each resource.) If the output of each resource is enabled with the DDR set to 0, the port is set to output. Since the reading of the parallel port is effective even if the output of each resource is enabled, the output value of each resource can be read.

- Operation for resource input

  Input to the resource is irrelevant to the setting conditions of the DDR and resource. The value of the pin is always input to the port serving as the resource input. When using an external signal at the resource, set the DDR to input.

- State when reset

  When reset, the DDR and resource output-enable bit are initialized to 0 and the output impedance goes High at all bits. (Pins with activated pull-up resistors are in the pull-up state.) When reset, the PDR is unde fined. Therefore, set the value of the PDR before setting the DDR to output.

- State in stop mode

  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR. (Pins with activated pull-up resistors are in the pull-up state.)

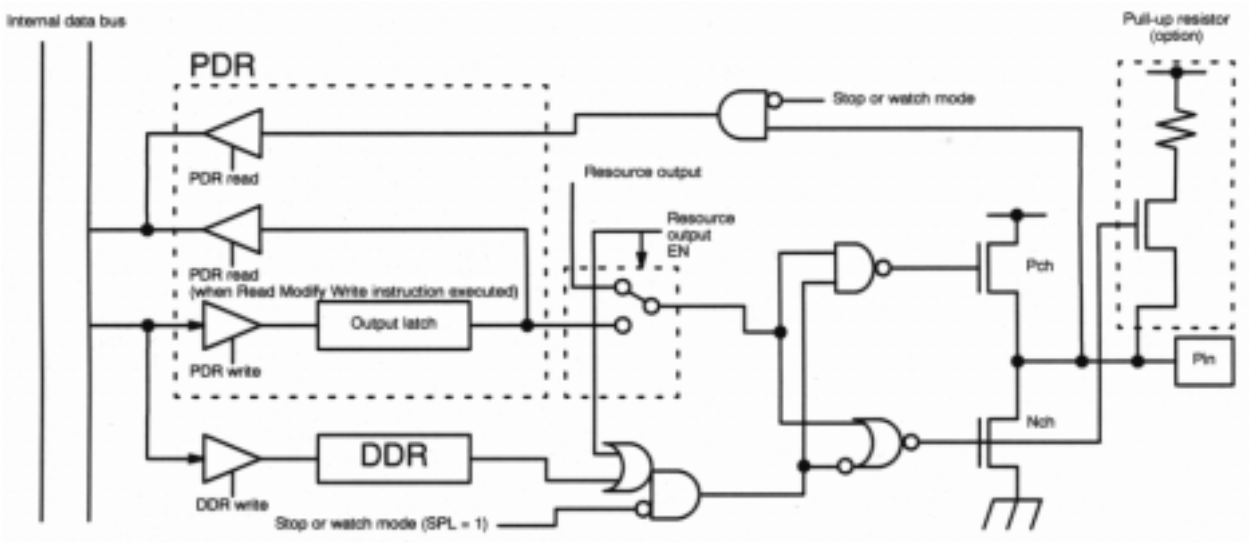


Fig. 2.12 Port 4

P50 to P53 N-ch open-drain-type I/O ports (also used as resource input/output)

- Switching input and output

  These ports have no register for specifying input or output. When using as an input port, set 1 at the Port Data Register (PDR).

- Operation for output port

  The value written at the PDR is output to the pin. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other.

- Operation for input port

  When using as the input port, set 1 at the PDR to turn off the output transistor. When the PDR is read under this condition, the value of the pin can always be read.

- Operation for resource output

  When using as a resource output, setting is performed by the resource output- enable bit (see description of each resource). Even if output of each resource is enabled, the port can be read other than when the Read Modify Write instruction is read. Therefore, the state of the pin can be checked.

- Operation for resource input

  The value of the pin is always input to the port serving also as the resource input irrespective of the setting of the resource. When using an external signal at the resource, set 1 at the PDR.

- State when reset

  The PDR is initialized to 1 at reset, so the output transistor is turned off at all bits.

- State in stop mode

  When the SPL bit of the standby-control register is set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR. (Pins with activated pull-up resistors are in the pull-up state.)

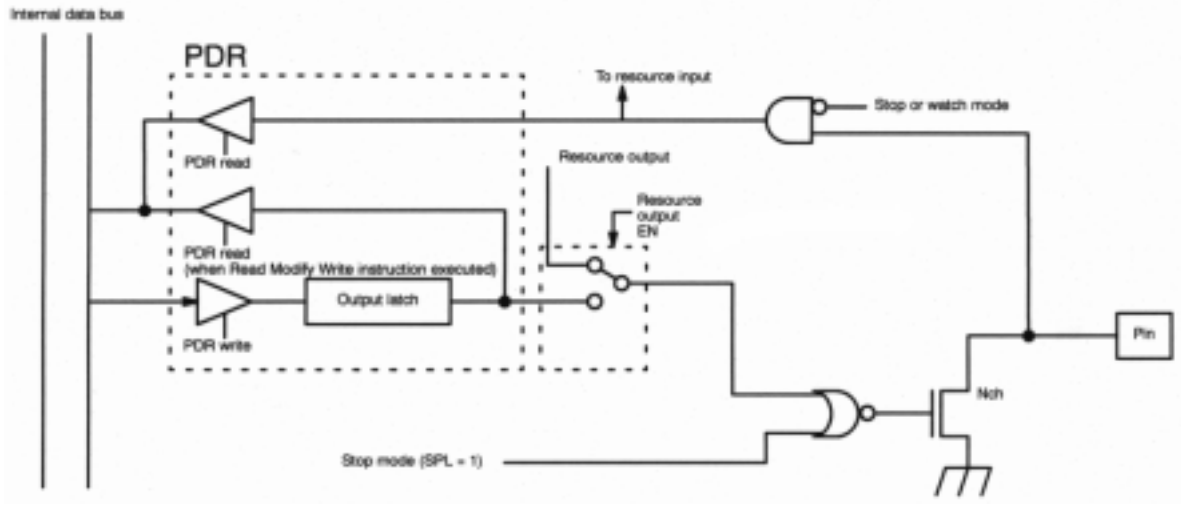


Fig. 2.13 Port 5

P60 to P67 N-ch open-drain-type output ports (also used as analog input)

- Operation for output port

  The value written at the PDR is output to the pin. When the PDR is read, the contents of the output latch are always read. Therefore, the state of the pin cannot be read.

- Operation for analog input

  When using as analog input, set 1 at the PDR to turn off the output transistor.

- State when reset

  When reset, the PDR is initialized to 1. Therefore, the output transistor is turned off at all bits.

- State in stop mode

  When the SPL bit of the standby-control register is set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

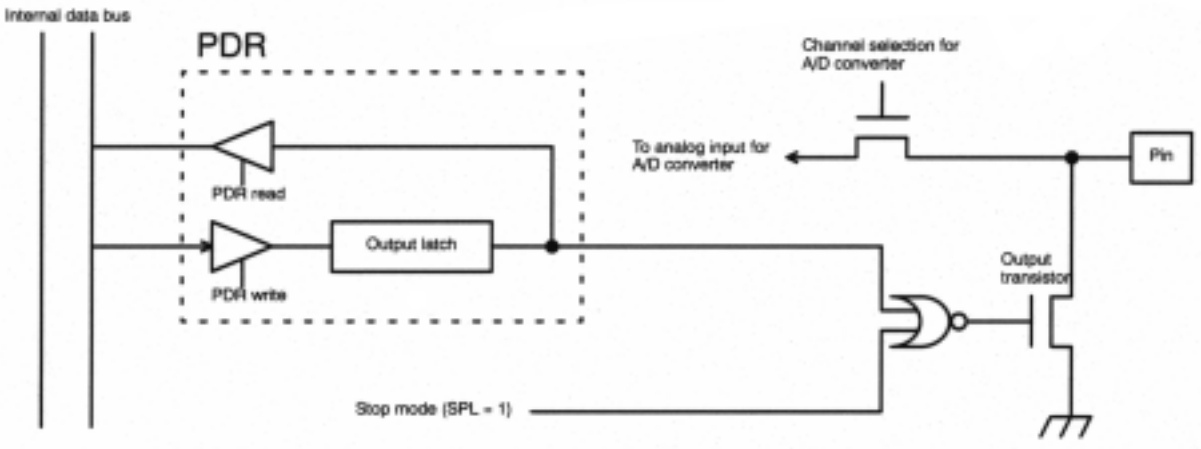


Fig. 2.14 Port 6

P70 to P74 Input-only ports (also used as external-interrupt input)

- Operation for external-interrupt input

  See the description of the external interrupts.

- Operation for input port

  The PDR can only be read and the value of the pin is always read. When using as an external-interrupt input, the value of the pin can also be read.

Note: P70 and P71 serve as oscillation circuit pins when the double clocks are operated and serve as input-only port which is also serve as external interrupt input, when single clock mode is operated.

- State at reset

  PDR is not initialized by raset.

- Operation at STOP mode

  These bits serve as the external interrupt input pins even at STOP mode.

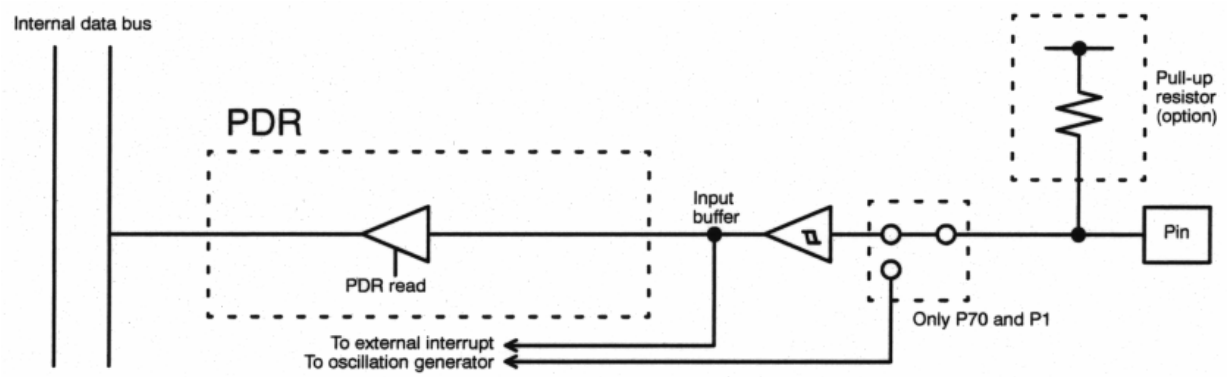
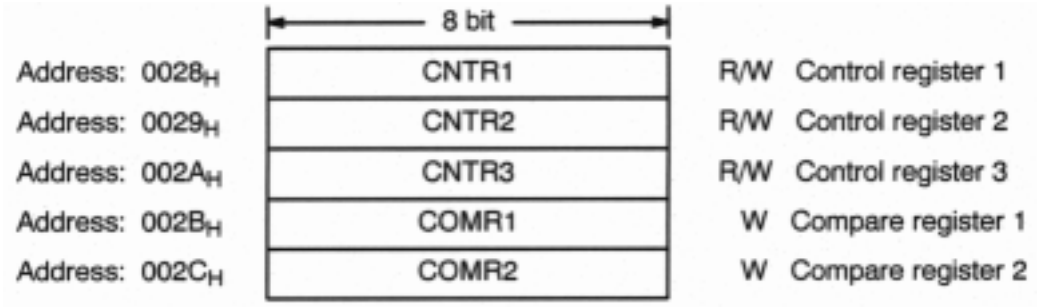


Fig. 2.15 Port 7

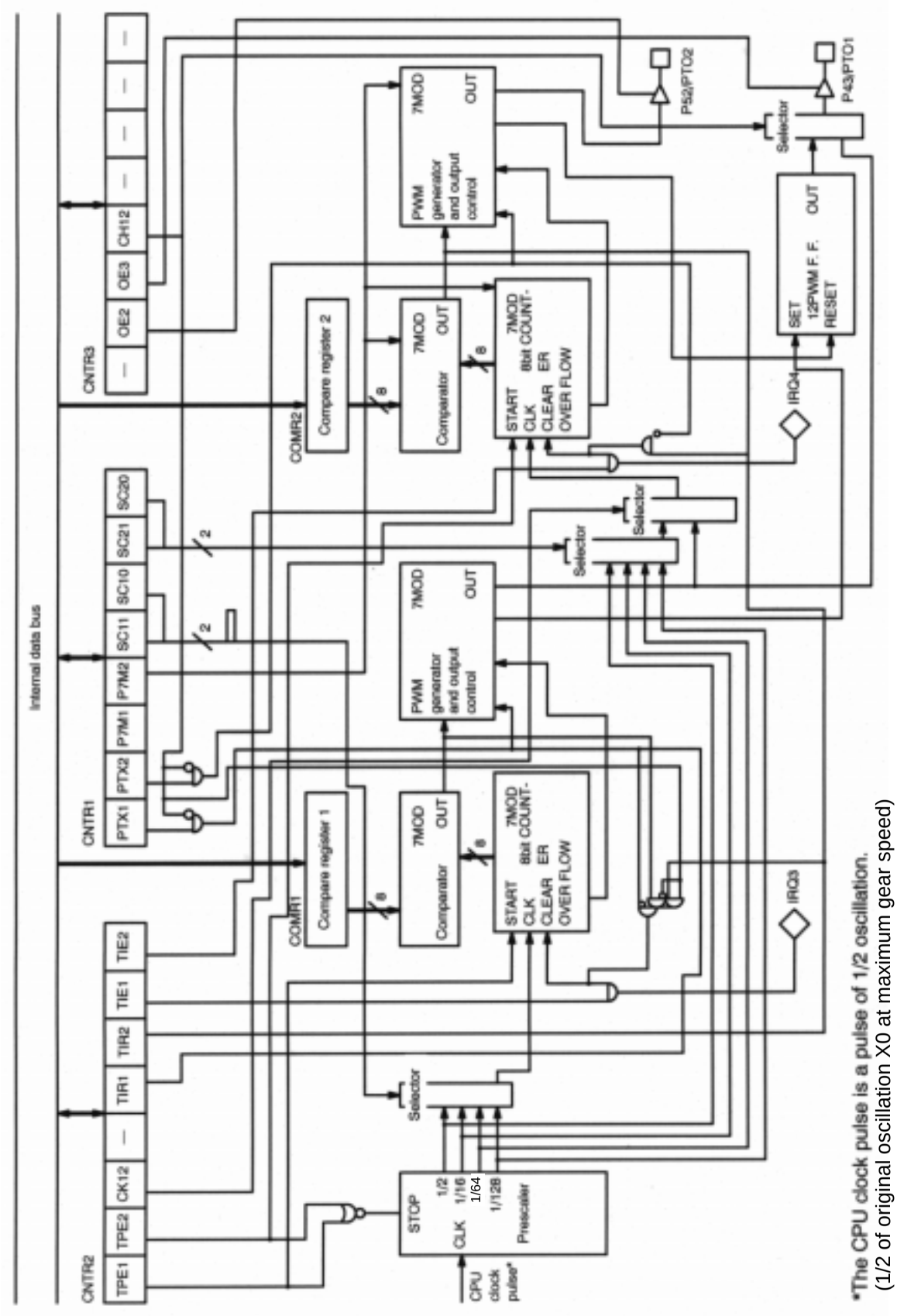
2.2.2 2-channel 8-bit PWM Timers (Timers 1 and 2)

- Four clock pulses can be selected.
- The input clock of CH2 has the CK12 mode to select CH1 output.
- This timer has the CH12PWM mode to output a PWM wave using CH1 and CH2.

(1) Registers



(2) Block diagram



(3) Description of registers

(a) Control register 1 (CNTR1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0028_H	PTX1	PTX2	P7M2	P7M2	SC11	SC10	SC21	SC20	$0000\ 0000_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] PTX1: CH1 timer/PWM operation mode switching bit

[Bit 6] PTX2: CH2 timer/PWM operation mode switching bit

The operation is performed as the timer when 0 is set at these bits, and as the PWM control circuit when 1 is written at these bits.

0	Timer
1	PWM-control circuit

The timer/PWM operation mode should be switched when the counter stops operation (TPE = 0), the inter rupt is enabled (TIE = 0), and the interrupt request flag is cleared (TIR = 0).

[Bit 5] P7M1: CH1 PWM operation mode switching bit

[Bit 4] P7M2: CH2 PWM operation mode switching bit

Writing 1 at P7W1 and P7W2 switches the mode from 8-bit PWM to 7-bit high-speed. This makes the PWM frequency two times larger than that in the 8-bit PWM mode.

0	8-bit PWM
1	7-bit PWM, high-speed mode

Do not write 1 at this bit in the timer mode.

[Bit 3 and 2] SC11, SC10: CH1 input-clock select bit

[Bit 1 and 0] SC21, SC20: CH2 input-clock select bit

Following clock cycles can be selected by these bits.

SC11	SC10	CH1 input-clock cycle (10 MHz with the highest speed gear)	
0	0	1 instruction cycle	(0.4 µs)
0	1	8 instruction cycle	(3.2 µs)
1	0	16 inctruction cycle	(6.4 µs)
1	1	64 instruction cycle	(25.6 µs)

SC21	SC20	CH2 input-clock cycle (10 MHz with the highest speed gear)	
0	0	1 instruction cycle	(0.4 µs)
0	1	8 instruction cycle	(3.2 µs)
1	0	16 inctruction cycle	(6.4 µs)
1	1	64 instruction cycle	(25.6 µs)

Note that these bits must not be rewritten when the counter is in operation (TPE = 1)

(b) Control register 2 (CNTR2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address:	TPE1	TPE2	CK12	—	TIR1	TIR2	TIE1	TIE2	000X 0000$_B$
0029$_H$	(R/W)	(R/W)	(R/W)		(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] TPE1: Counter-operation enable bit

[Bit 6] TPE2: Counter-operation enable bit

When this bit is set to 1, the timer or PWM-control circuit starts operation.

0	Counter operation stop (Timer cleared)
1	Counter operation start

[bit 4] CK12: CH2 input-clock switching bit

When 1 is written at this bit, CH1 toggle output is selected as the input clock of CH2 irrespective of the values of the SC21 and SC20 bits.

0	Clock selected by SC21 and SC20 bits
1	CH1 toggle output

Do not write 1 at this bit when the CH1-2PWM mode is set (CH1-2 bit = 1).

[Bit 3] TIR1: CH1 interrupt-request flag bit

[Bit 2] TIR2: CH2 interrupt-request flag bit

When an interrupt source occurs, these bits go to 1. To clear the generated interrupt source, write 0 at these bits. The meaning of each bit to be read is as follows:

0	Values of counter and COMR do not agree
1	Values of counter and COMR agree

Note that 1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

Note: In the PWM operation mode, neither the read nor write values of these bits have any meaning.

[Bit 1] TIE1: CH1 interrupt enable bit (timer mode)

[Bit 0] TIE1: CH2 interrupt enable bit (timer mode)

If these bits are set to 1, an interrupt occurs when the values of the counter and compare register agree.

0	Counter interrupt-output disabled
1	Counter interrupt-output enabled

However, in the PWM operation mode, interrupt occur irrespective of the values of these bits.

(c) Control register 3 (CNTR3)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $002A_H$	—	OE2	OE3	CH12	—	—	—	—	$0000\ XXXX_B$
	(R/W)	(R/W)	(R/W)	(R/W)					

[Bit 6] OE2: CH2 output-signal control bit

If this bit is 1, the port serves as the timer/PWM output. In the timer operation mode, usually a signal which is reversed each time the value of the counter and compare register agree, is output. In the PWM operation mode, a PWM signal is output.

0	General-purpose port (P53)
1	Counter/PWM output pin (PTO2)

If this bit is 1, the port functions as the counter/PWM output pin even after the PDR P53 are set to 1.

[Bit 5] OE3: CH 1-2 PWM mode output signal control bit

When this bit is 1, the port serves as the CH1-2 PWM output.

0	General-purpose port pin (P43)
1	CH1-2 PWM output pin/CH1 output (PTO1)

When the CH1-2 bit is 0, the port serves as the CH1 output.

[Bit 4] CH1-2: CH1-2 PWM mode set bit

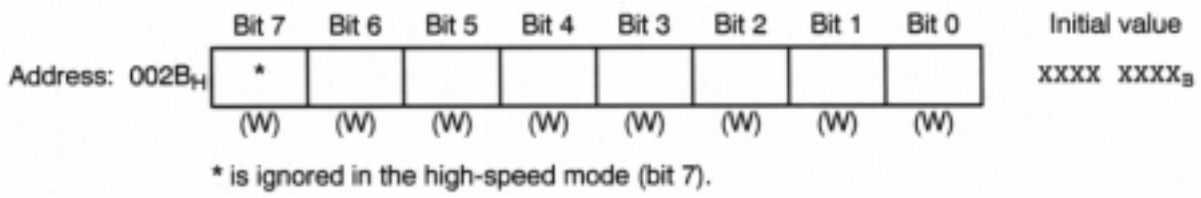
When this bit is 1, the CH1-2PWM mode is set. CH1 and CH2 enter the timer mode irrespective of the values of the PTX1 and PTX2 bits.

0	Ordinary mode
1	CH1-2 PWM mode

Do not rewrite this bit when CH1 or CH2 is in counter operation (TPE1 = 1 or TPE2 = 1).

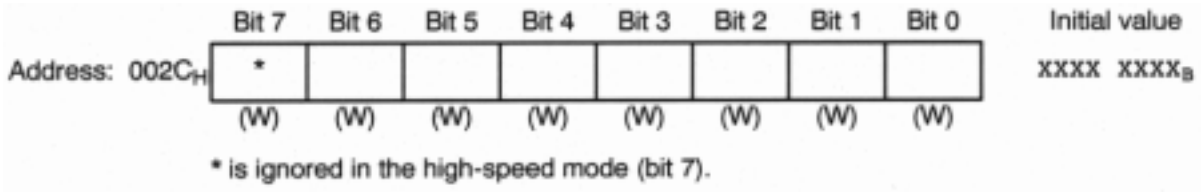
(d) Compare register 1 (COMR1)

This register is used to set the value to be compared with the value of the counter in the CH1 timer-opera tion mode. The counter is cleared in the timer-operation mode and when the values of the counter and this register agree. In the PWM operation mode, the High pulse width can be specified by the value of this register.



(e) Compare register 2 (COMR2)

This register is used to set the value to be compared with the value of the counter in the CH2 timer-opera tion mode. The counter is cleared in the timer-operation mode and when the value of the counter and this register agree. In the PWM operation mode, the High pulse width can be specified by the value of this register.



(4) Description of operation

(a) Timer operation

Setting the PTX bits 1 and 2 of the CNTR1 to 0 gives the timer-operation mode. When the TPE bits 1 and 2 of the CNTR2 are set to 1, the counter starts incrementing from 00H. When the value of the counter agrees with that of the COMR, the counter is cleared on the next count clock pulse and incrementing restarts. Therefore, the TIR bits 1 and 2 are set and the output pin is reversed (when the TPE bits 1 and 2 are 0, the output pin is fixed at Low level) in cycles of the count clock pulses when 00H is written at the COMR, or in cycles 256 times longer than those of the count clock pulses when FFH is written.

If the value of the COMR is rewritten in the timer-operation mode, it becomes effective from the next cycle (when the value of the counter is **00H**, the value of the COMR is transferred to the comparator latch).

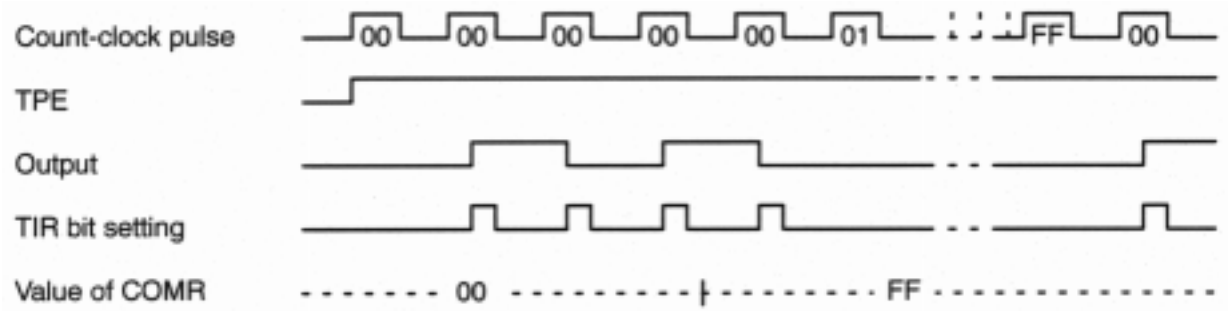


Fig. 2.16 Timer Operation

If the TIE bits 1 and 2 of the CNTR2 are set to 1, an interrupt occurs when the values of the counter and COMR agree. During interrupt processing, the TIR bits 1 and 2 are used as the interrupt flag. The TIR bits 1 and 2 are set to 1 irrespective of the value of the TIE bits 1 and 2.

Writing 0 at the TIR bits 1 and 2 permits clearing of the interrupt source or the TIR bits 1 and 2. When the Read Modify Write instruction is read, the TIR bits 1 and 2 is set so that 1 can always be read to prevent erroneous clearing.

The count clock pulse can be selected from four clock pulses from the prescaler by the clock pulse select bits SC11, SC10, SC21, and SC20 of the CNTR1 register. When 1 is written at the CK12 bit of the CNTR2 register, CH1 toggle output is selected as the input clock of CH2 irrespective of the values of the SC21 and SC20 bits.

Note: When the PWM operation mode is specified, do not put CH1 in the CK12 mode (do not write 1 at the CK12 bit).

(b) PWM operation

Setting the PTX bits 1 and 2 of the CNTR1 to 1 gives the PWM operation mode. The COMR1 and 2 specify the duty of the output pulse. Pulses can be output with 1/256 resolution and a duty of 0% to 99.6% . When 0 (**00H**) is written at the COMR1 and 2, the duty of the PWM output pulse is 0%; when 128 (**80H**) is written, the duty is 50%, and when 255 (**FFH**) is written, it is 99.6%.

The value of COMR is transferred to the comparator latch when the value of the counter is 00H. If the value of the COMR is rewritten in the PWM operation mode, it becomes effective from the next cycle.

- When COMR is 00H

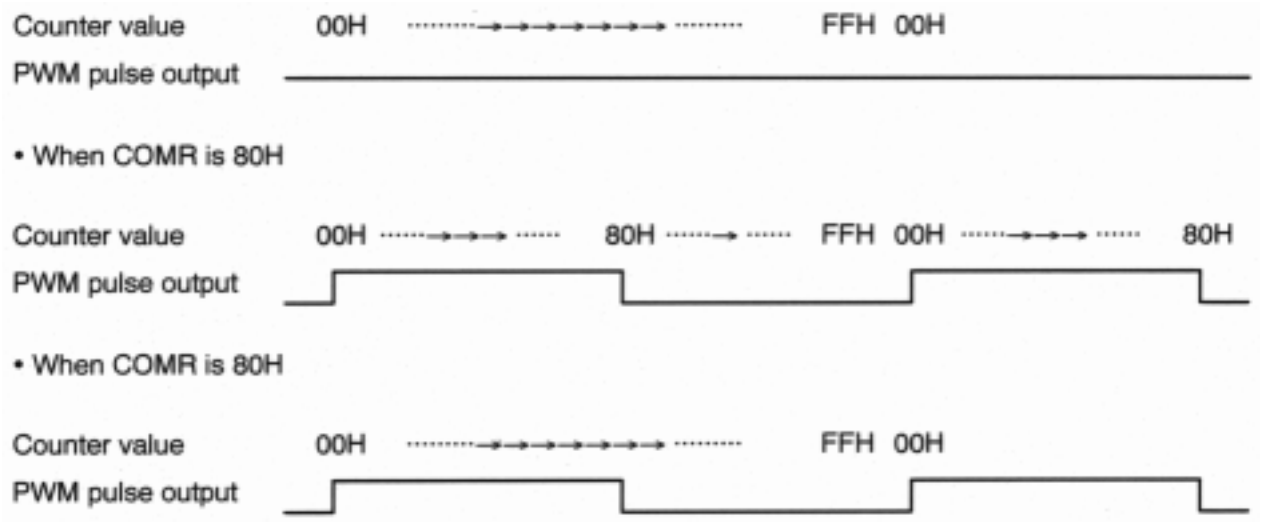


Fig. 2.17 PWM Pulse Output

The TIR bits 1 and 2 of the CNTR2 have no relation with the PWM operation. No interruption occurs irre spective of the TIE bits 1 and 2.

The cycle and frequency of the PWM pulse can be changed by switching the count clock pulse. The count clock pulse can be selected from four clock pulses from the prescaler by clock-pulse select bits SC11, SC10, SC21, and SC20 of the CNTR1. When 1 is written at the CK12 bit of the CNTR2 register, CH1 toggle output is selected as the input clock of CH2 irrespective of the values of the SC21 and SC20 bits.

Note: When the PWM operation mode is specified, do not put CH1 in the CK12 mode (do not write 1 at the CK12 bit).

(c) High-speed PWM operation (7-bit PWM)

In the PWM operation mode, there are the normal mode with 8-bit 256 resolution and the high-speed mode with 7-bit 128 resolution.

Writing 1 at the P7M1 and P7M2 bits of the CNTR1 register gives this mode.

Table 2.6 PWM Cycle and Resolution
(Clock = 10 MHz with the Highest Speed Gear (Instruction Cycle = 400 ns))

Selected clock	Ordinary mode			High speed mode		
	Resolution	PWM cycle	PWM frequency	Resolution	PWM cycle	PWM frequency
1 instruction cycle	400 ns	102.4 μs	9.8 kHz	400 ns	51.2 μs	19.5 kHz
1/8 instruction cycle	3.2 μs	819.2 μs	1.2 kHz	3.2 μs	408.6 μs	2.4 kHz
1/16 instruction cycle	6.4 μs	1.6 ms	625 Hz	6.4 μs	819.2 μs	1.2 kHz
1/64 instruction cycle	25.6 μs	6.5 ms	153.8 Hz	25.6 μs	3.3 ms	303 Hz
Channel-1 toggle output	0.8 μs	204.8 μs	4.9/n Hz	0.8 μs	102.4 μs	4.9/n Hz

n = 1, 2, 3, ..., 255, 256 (CH1 timer compare register value + 1)

(d) CH1-2 PWM mode

This mode causes the 2-channel PWM timer to be a timer and generates width L with the CH1 timer and the cycle with the CH2 timer to output a PWM wave.

Writing 1 at the CH1-2 bit of the CNTR3 register gives this mode. The timer mode is set irrespective of the values of the PTX1 and PTX2 bits of the CNTR1 register. A PWM wave is output from the P43 pin con trolled by OE3 to the compare registers 1 and 2.

To start the operation, write 1 simultaneously at the TPE1 and PTE2 bits of the CNTR2 register. Writing 1 separately at the TPE1 and TPE2 bits changes the duty or cycle. However, when the count value of CH2 agrees with the value of the compare register, both the CH1 and CH2 are simultaneously counter-cleared. Therefore, the duty or cycle is based on the value of the compare register from the second cycle.

When not in the CH1-2PWM mode, the P43 pin provides the CH1 toggle output or outputs a PWM wave. The default value of the PWM output is Low level.

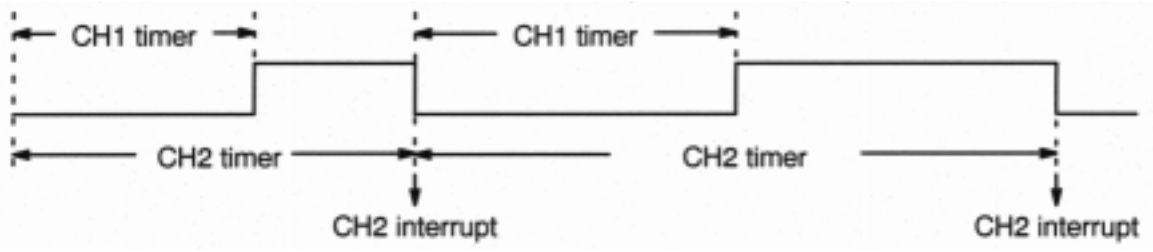
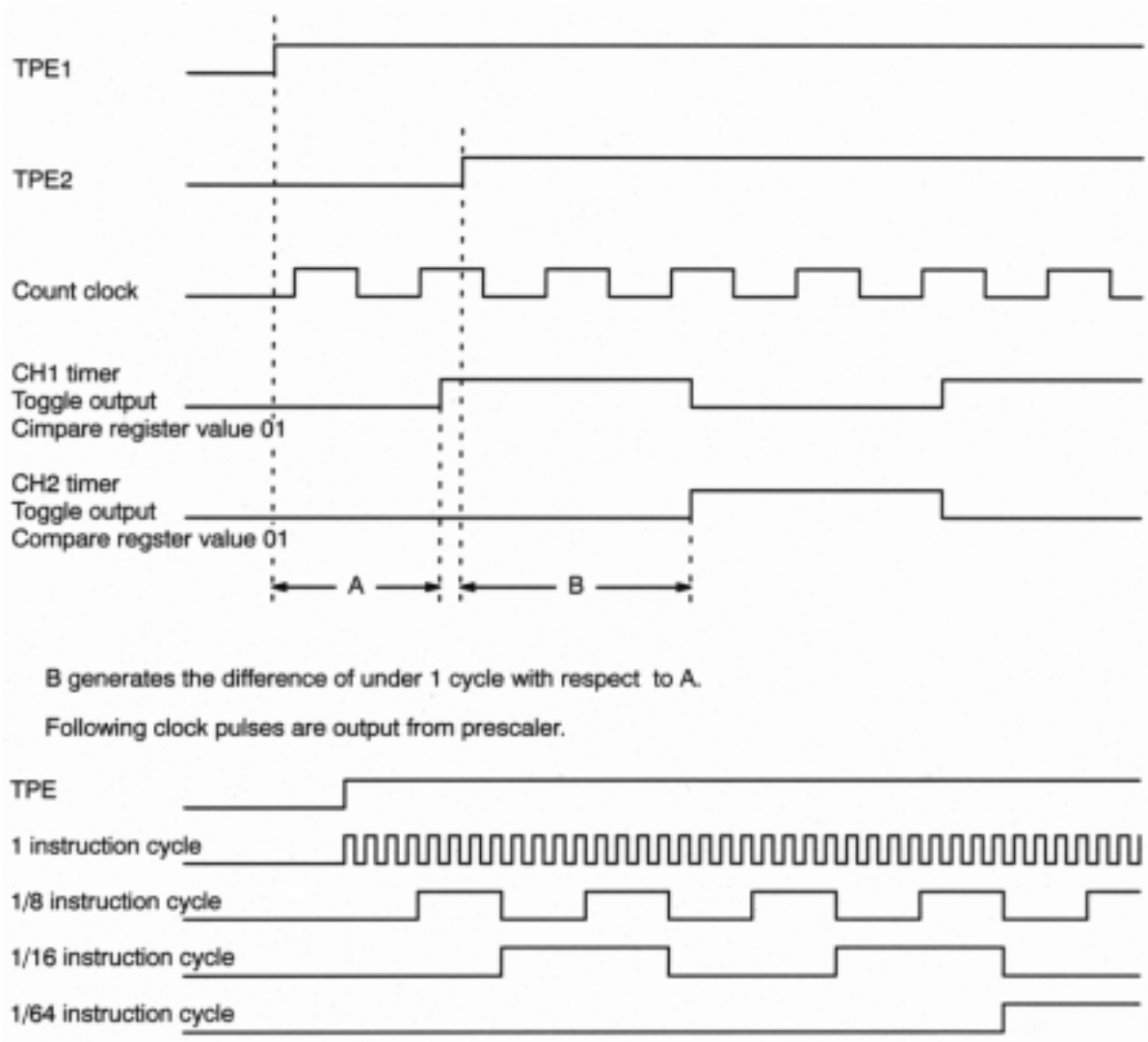


Fig. 2.18 PWM Wave Output at CH1-2 PWM Mode

If the cycle of the CH1 timer becomes larger than that of the CH2 timer, a PWM wave is not output. The CH1 timer should be disabled for an interrupt. The CH2 timer can be used in the same manner as the nor-mal timer.

(e) Prescaler

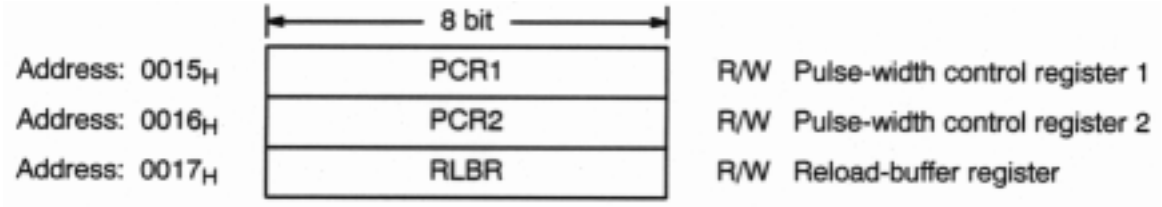
The prescaler can operate when either of the TPE1 or TPE2 bit is 1. Therefore, when 1 is written simulta neously at the TPE1 and TPE2 bits, both CH1 and CH2 perform the same operation from the first cycle. However, if either of the TPE1 or TPE2 bit is already 1 and the timer or PWM starts operation after the prescaler has been enabled, a difference of not more than one cycle occurs in the input clock pulse of the counter.



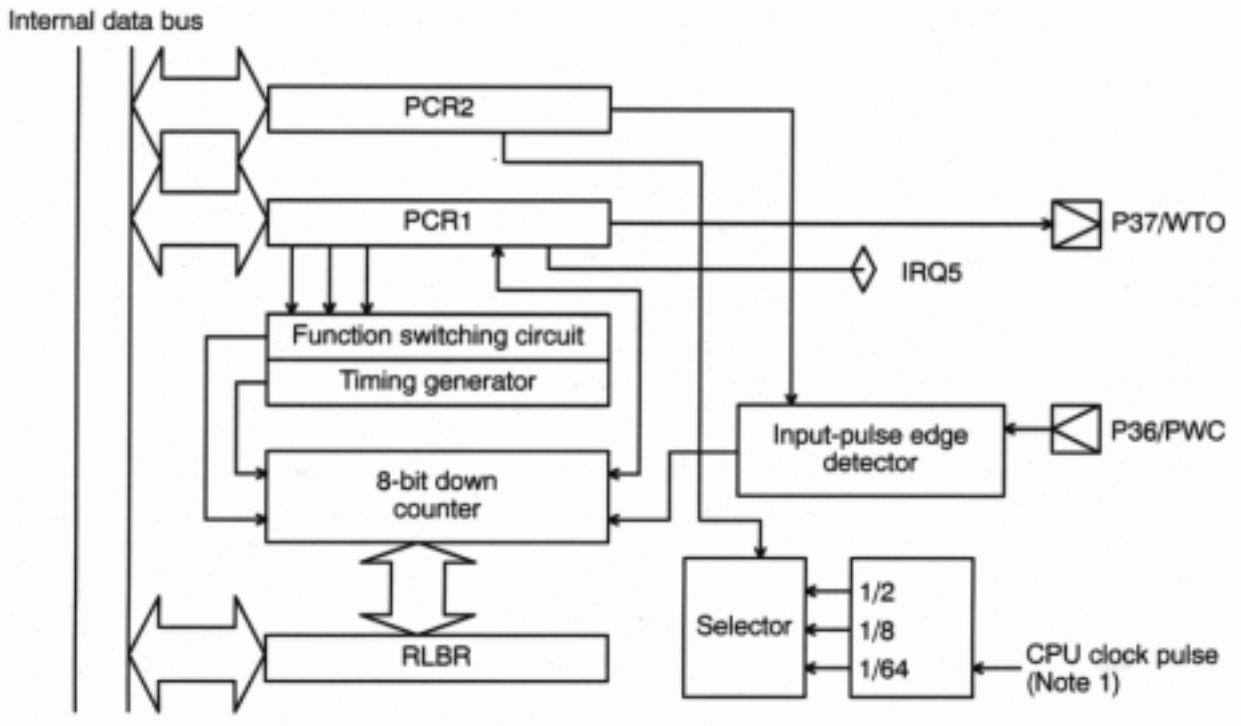
2.2.3 Pulse-width Count Timer (Timer 3)

- This timer has timer and pulse-width measurement functions.
- The timer function has two modes: reload timer and one-shot timer modes.
- In the reload-timer mode, the set values are decremented repeatedly.
- In the one-shot-timer mode, decrementing is started from the set value and stops at the first underflow.
- The pulse-width measurement function allows measurement of High, Low, or one-cycle widths of pulses input from pins.

(1) Registers



(2) Block diagram



Note: The CPU clock pulse is the pulse with 1/2 oscillation (gear max. at gear maximum speed).

(3) Description of registers

(a) Pulse-width control register 1 (PCR1)

This PCR1 is used to enable and disable each function and to display the state of the timer.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0015_H	EN	TOE	IE	—	—	UF	IR	BF	$000X\ X000_B$
	(R/W)	(R/W)	(R/W)			(R/W)	(R/W)	(R)	

[Bit 7] EN: Counter-operation enable bit

At the timer function, when 1 is written at this bit, the value of the data register is loaded to start the decre menting. At the pulse-width measurement function, when 1 is written at this bit, the measurement-enable state is set. Under this condition, decrementing starts when the edge of the measured pulse is detected. When 0 is written at this bit during measurement, the operation stops but the value of the counter is not transferred to the buffer (RLBR).

	Timer function	Pulse-width measurement function
0	Count-operation disable	Pulse-width measurement function stop/disable
1	Count-operation enable/start	Pulse-width measurement function enable/start

[Bit 6] TOE: TO bit output-enable bit

When Bit 6 is set to 1, the contents of the TO bit are output to port P37.

0	General-purpose port (P37) (default)
1	TO bit output (WTO)

If this bit is set to 1 even after the DDR of P37 is set to input, the port functions as the TO bit output port.

[Bit 5] IE: Interrupt-enable bit

When Bit 5 is 1, an interrupt request is output if the interrupt-request flags (UF, IR, and BF) are set.

0	Interrupt disabled (default)
1	Interrupt enabled

[Bit 2] UF: Underflow interrupt-request bit

Bit 2 indicates the presence or absence of timer overflow. The meaning of each bit to be read is as follows:

0	Underflow does not occur.
1	Underflow occurs.

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 1] IR: Bit for interrupt request at measurement termination

When the IE bit (bit 5) of the PCR1 is 1, an interrupt occurs at termination of pulse measurement. The meaning of each bit to be read is as follows:

0	Pulse-width measurement not terminated
1	Pulse-width measurement terminated

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 0] BF: Buffer-full flag

When the IE bit (bit 5) of the PCR1 is 1, an interrupt occurs if any measured value is found in the RLBR. This bit is set when the pulse-width measurement is terminated, and is cleared when data in the buffer is read. The meaning of each bit to be read is as follows:

0	Pulse-width measured value not found
1	Pulse-width measured value found

(b) Pulse-width control register 2 (PCR2)

The PCR2 is used to select the timer operation modes.

Rewriting is possible only when bit 7 (EN) of the PCR1 is 0.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0016_H	FC	RM	TO	—	C1	C0	W1	W0	$000X\ 0000_B$
	(R/W)	(R/W)	(R/W)		(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] FC: Function-select bit

Bit 7 is used to select the timer and pulse-width measurement functions.

0	Timer function
1	Pulse-width measurement function

[Bit 6] RM: Timer mode-select bit

At the timer function, this bit is used to select the modes below.

0	Reload-timer mode
1	One-shot timer mode

[Bit 5] TO: Timer-output bit

The value of Bit 5 is reversed each time the counter underflows. When the TOE bit (bit 6 of CSR1) is 1, the contents of this bit are output from the WTO pin.

[Bits 3 and 2] C1 and C0: Counter clock-pulse select bits

Setting is made as shown below by a combination of these bits. These bits are not related to the value of the FC bit.

C1	C0	Count clock pulse
0	0	Internal clock pulse 1 instruction cycle
0	1	Internal clock pulse 1/4 instruction cycle
1	0	Internal clock pulse 1/32 instsruction cycle
1	1	Do not set.

[Bits 1 and 0] W1 and W0: Measured pulse-select bit

Setting is made as shown below by a combination of these bits. These bits are not relevant in the timer-op eration mode (at FC = 0).

W1	W0	Measured pulse width
0	0	High level
0	1	Low level
1	0	Rising edge to rising edge
1	1	Falling edge to falling edge

(c) Reload buffer register (RLBR)

At the timer function, this register can be read and written. At the pulse-width measurement function, it functions as the read-only data buffer register used for holding the measured value. In this case, writing is impossible. Data is read to clear the BF flag (bit 0) of the PCR1.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0017_H									xxxx xxxx$_B$
At timer function ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
At pulse-width measurement function ⇒	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

(4) Description of operation

(a) Timer function

This timer has the following two modes: reload timer and one-shot timer.

(1) Reload timer mode

Each time the counter underflows, the value written at the RLBR is reloaded to continue the decrement ing. When the counter underflows, the interrupt flag UF (bit 2) is set. If the IE bit (bit 5) is set to 1, an interrupt request is output. If the TOE bit (bit 6) is set to 1, the value of the TO bit is reversed each time the timer underflows.

(2) One-shot timer mode

When an underflow occurs, the timer stops operation. When the counter underflows, the interrupt request flag UF (bit 2) is set. The EN bit (bit 7) is automatically set to 0 to stop counting.

In both modes, counting starts when 1 is written at the EN bit (bit 7), and it stops when 0 is written.

(b) Pulse-width measurement function

(1) Measurement start

Writing 1 at the FC bit (bit 7) and EN bit (bit 7) causes the counter to enter the operation-enable state. Counting starts when the edge of the measured pulse input is detected under this condition. At the pulse-width measurement function, decrementing is started from FF_H.

(2) Measurement end and measured value

When measurement is terminated, the counter transfers the measured value to the buffer, sets the measurement-end flag IR (bit 1) and buffer-full flag BF (bit 0), and then enters the operation-enable state again. At this time, an interrupt request is output if the IE bit (bit 5) is set to 1. However, if the previous measured value cannot be read after continuous pulse-width measurement, continue to set the BF flag to hold the previous measured value. The new measured value is discarded.

(3) Long pulse

If the counter undeflows during measurement, set the UF bit (bit 2) to continue counting. In this case, an interrupt request is also output if the IE bit (bit 5) is set to 1.

(4) Operation stop

Measurement stops when 0 is written at the EN bit (bit 7).

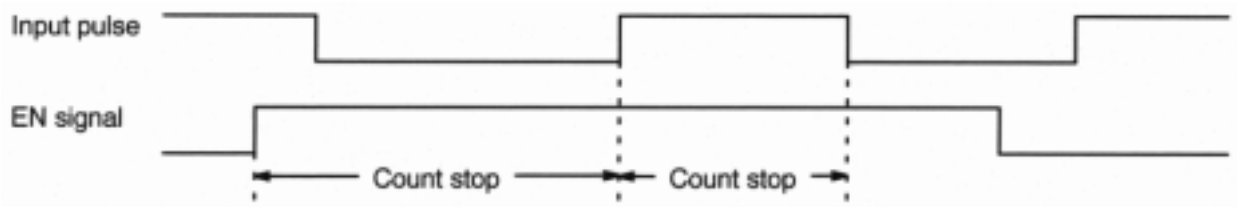
(5) Calculation of pulse width

The measured value to be transferred to the buffer is the same as that of the counter when measurement is terminated. Therefore, the pulse width should be calculated as follows:

Pulse width = [(256 - counter value) + (Number of TO reversed ψ 256)] ψ 1 cycle width of count clock pulse

(6) Others

The counter is in the operation-enable state even after the end of measurement, so continuous pulse-width measurement is enabled. The High width measurement is started from the changing edge of the input pulse. If the input pulse is already High, enable the EN bit (0 %1) to perform counting after the next rising edge occurs.



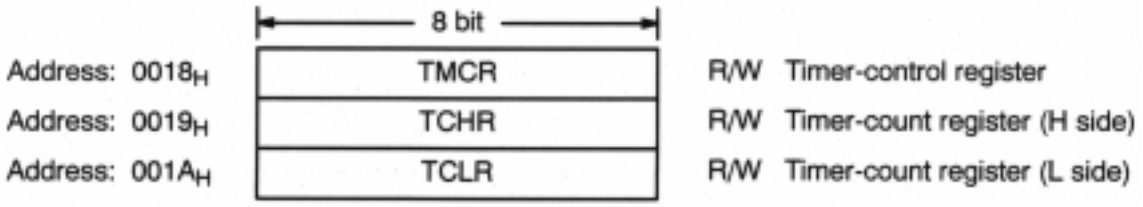
(5) Precautions for use

(a) When the EN bit is 1 (during timer operation or pulse-width measurement), do not rewrite the con tents of the PCR2.
(b) When the mode is switched (the FC bit is rewritten), the state of each flag does not change. There fore, clear each flag immediately after switching the mode.
(c) Read the measured value before the next underflow occurs. If the value is read after an underflow occurs, the TO bit is reversed, sometimes disabling calculation of the correct measured value.
(d) If the previous measured value cannot be read after continuous pulse-width measurement, hold the previous measured value without transferring the new one to the buffer.

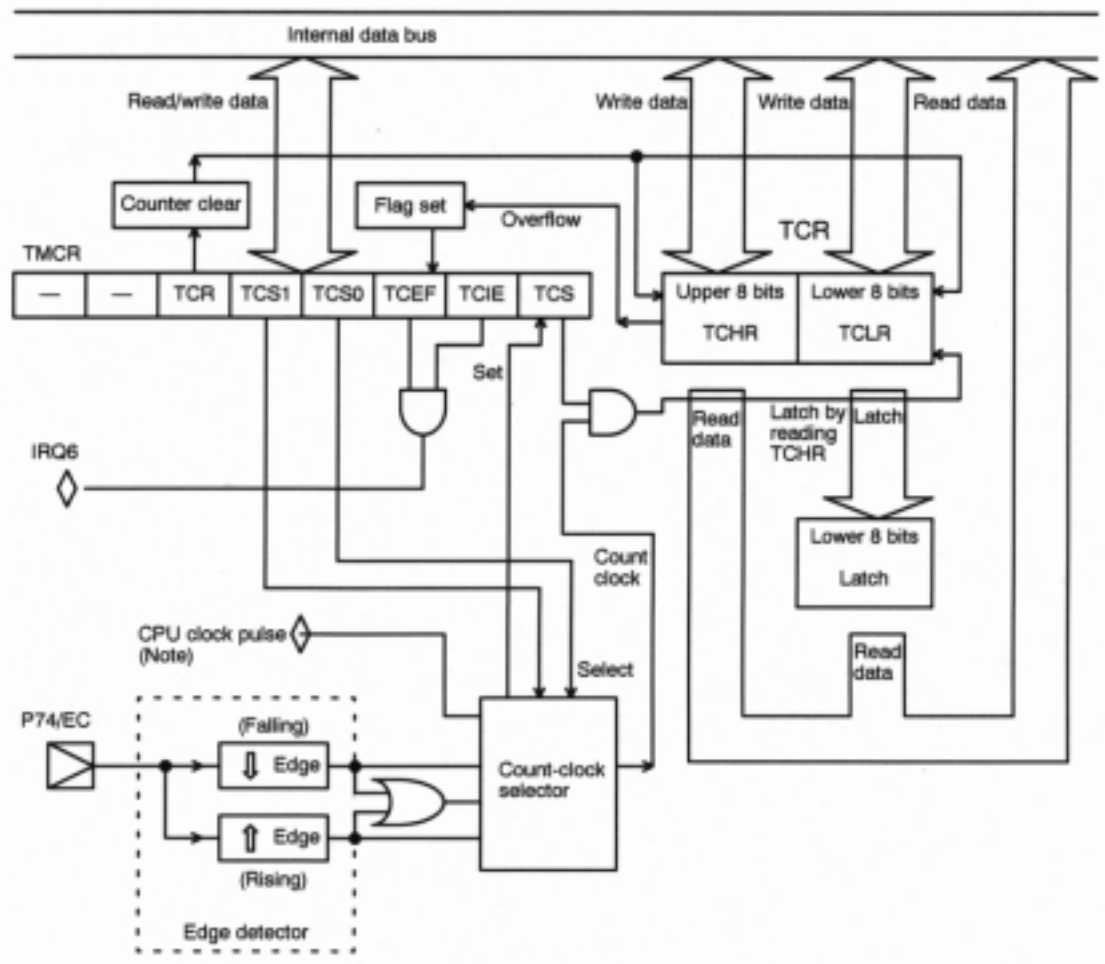
2.2.4 16-bit Timer/Counter (Timer 3)

- 16-bit binary timer/counter
- It is possible to select the timer function for count-clocking internal clock sources and the counter function for counting by detecting an arbitrary edge of the external pin input.
- An arbitrary byte value can be written from the data bus to the counter.
- An interrupt request can be output to the CPU by detecting counter overflow.

(1) Registers



(2) Block diagram



Note: The CPU clock pulse is the pulse with 1/4 oscillation.

(3) Description of registers

(a) Timer-control register (TMCR)

This 6-bit register selects and controls various operations of the counter, and controls interrupts.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0018_H	—	—	TCR	TCS1	TCF0	TCEF	TCIE	TCS	XX00 0000_B
			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 5] TCR: Counter-clear bit

Bit 5 is used to clear the counter. The meaning of each bit to be written is as follows:

0	Counter cleared - The contents of the 16-bit counter are set to 0000_H.
1	Other counters not affected

The read value of this bit is always 1.

[Bits 4 and 3] TCS1 and TCS0: Timer/counter operation-mode select bits

These bits are used to select the timer/counter operation mode and to determine the detection edge of the external-count clock pulse to be detected in the counter- operation mode. The counter-operation mode and the detection edge of the external-count clock pulse are selected as shown below.

Table 2.7 Selection of Timer/Counter Operation Mode

TCS1	TCS0	Operation mode	
0	0	Timer mode (Internal clock source operation)	
0	1	Counter mode	Detect falling edge of external input.
1	0		Detect rising edge of external input.
1	1		Detect both edges of external input.

[Bit 2] TCEF: Interrupt-request flag

Bit 2 is a flag for interrupt request due to counter overflow. The meaning of each bit to be read is as follows:

0	Counter does not overflow.
1	Counter overflows (counter value $FFFF_H \Rightarrow 0000_H$).

Note: 1 is always read when the Read Modify Write instruction is read. When interrupt-output is enabled (TCIE = 1), an interrupt request is output to the CPU if this bit is 1.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 1] TCIE: Interrupt-request output-enable bit

Bit 1 is used to enable and disable interrupt output to the CPU. When the bit is 1, an interrupt request is output if the interrupt flag TCEF (bit 2) is set to 1. When the bit is 0, interrupt-request output is disabled.

0	Interrupt-request output disabled
1	Interrupt-request output enabled

[Bit 0] TCS: Count start bit (counter-enable bit)

Bit 0 is used to start and stop the counter. When 1 is written at this bit, the TCR is enabled for counting and the value of the counter is incremented by the count clock. When 0 is written, the TCR stops counting to hold the value of the counter.

0	Count disabled
1	Count enabled

(b) Timer-count register (TCR)

The TCR is a 16-bit binary up counter. TCHR is used for upper bytes; the TCLR is used for lower bytes. Writing to the counter should be performed when counting stops (TCS bit (bit 0) of TMCR = 0). To read the counter, always use the word transfer instructions (MOVW A, dir, etc.).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0019_H									$0000\ 0000_B$ TCHR
Address: $001A_H$									$0000\ 0000_B$ TCLR
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(4) Description of functions

(a) Operation modes

The operation modes of the 16-bit timer/counter can be selected from the timer and counter modes by a combination of bit 3 (TCS0) and bit 4 (TCS1) of the TMCR.

(1) Timer mode

Setting values other than $\mathbf{00_B}$ at bit 3 (TCS0) and bit 4 (TCS1) of the TMCR gives the timer mode. The TCR increments according to the internal clock source (1/4 oscillation or instruction cycle); external-count input is disabled at this time. Detecting an overflow enables generation of time intervals up to 2^{16} times the clock source (65536 instruction cycles). The maximum time intervals are 32.8 ms at 8 MHz oscillation.

(2) Counter mode

Setting values other than $\mathbf{00_B}$ at bit 3 (TCS0) and bit 4 (TCS1) of the TMCR gives the counter mode. The edge polarities given in Table 2-1 can be selected according to the value to be set. The counter mode is divided into three according to the setting of the edge detection for the external-count input. In the counter mode, the TCR increments each time the arbitrary edge of the EC input for the external-count clock pin is detected. (The internal clock source is disabled at this time.) This enables counting with the number of external-count input events (arbitrary edges). The pulse width of the external-count clock input can be input from 8 to a minimum width of two instruction cycles (This corresponds to DC to 1/2 instruction cycle).

(b) Count start/stop

The TCR starts counting when 1 is written at bit 0 (TCS) of the TMCR, and stops counting when 0 is written.

(c) Counting and interrupt occurrence

In the timer mode, the TCR is incremented every one instruction cycle of the clock source; in the counter mode, it is incremented each time the effective edge of the external-count input is detected. When the counter value changes from $\mathbf{FFFF_H}$ to $\mathbf{0000_H}$ (overflows), an overflow-interrupt request is output to the CPU if the interrupt flag TCEF (bit 2) of the TMCR is set to 1 and the interrupt-request output-enable bit TCIE (bit 1) is 1.

Any byte value can be set at the TCR. (This setting should be done when the counter stops (TCS = 0).) The value of the TCR can be read even during operation. To read, always use the word-transfer instructions (MOVW A, dir, etc.).

(d) Counter clear

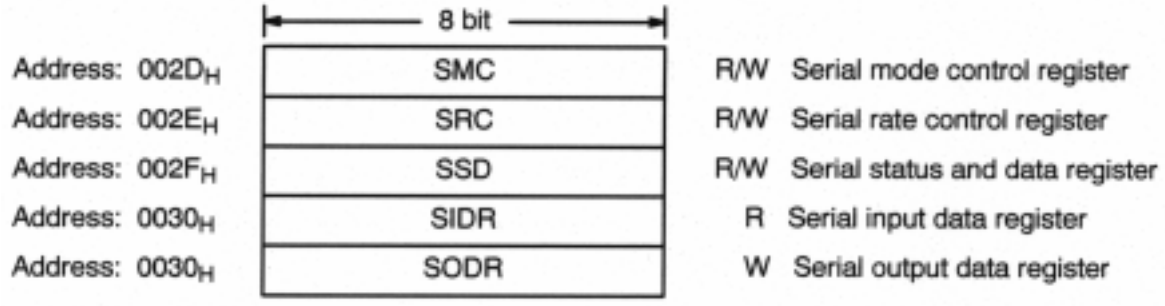
The TCR is cleared to $\mathbf{0000_H}$ when 0 is written at bit 5 (TCR) of the TMCR. If clearing is performed concurrently with overflow, the interrupt flag is not set.

2.2.5 UART

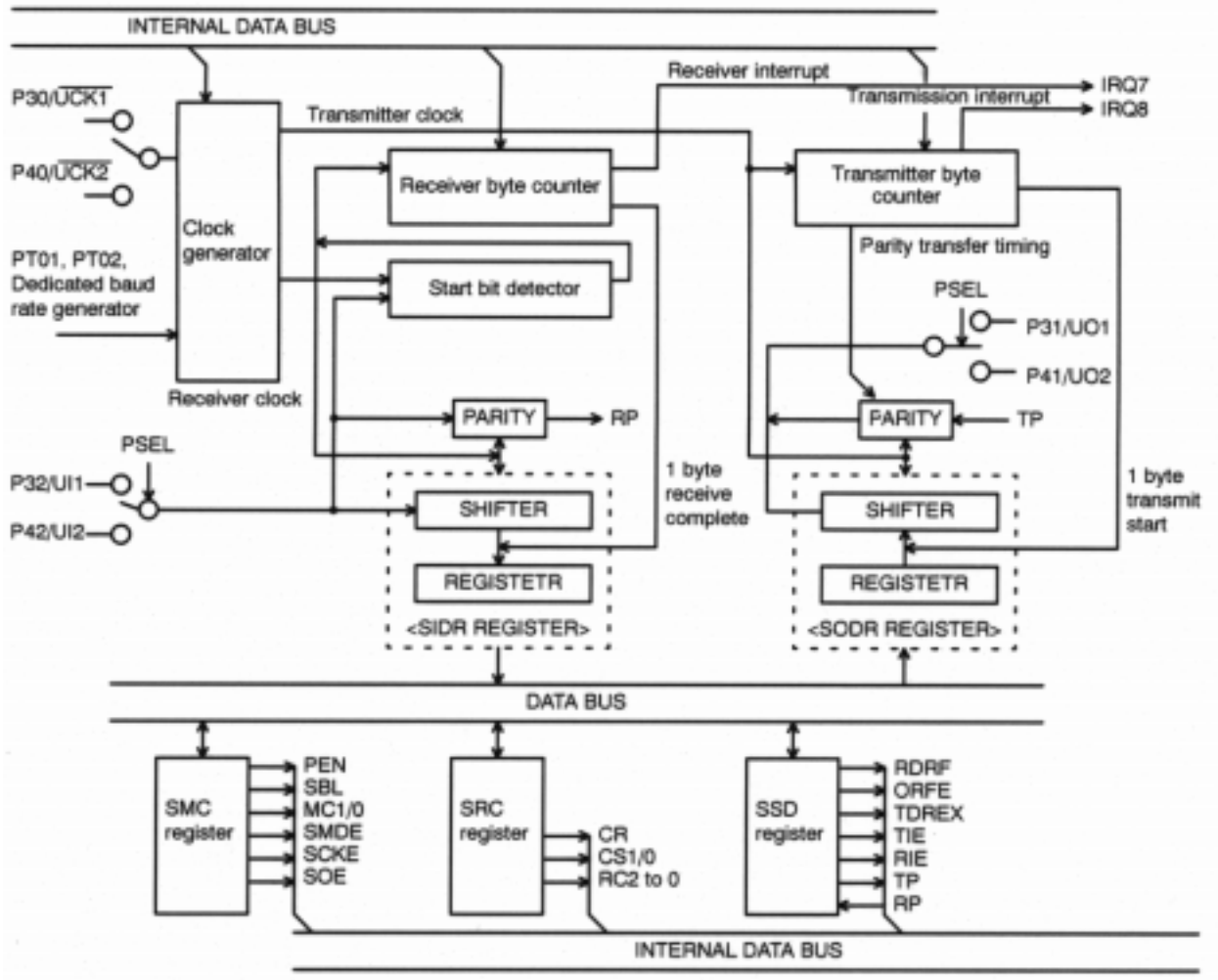
Outline

- Full-duplex double buffers
- CLK synchronous and asynchronous data transfer
- 14 baud rates (for internal clock)
  The baud rate can also be freely selected by external clock input or input from the internal timer.
- Variable data length
- NRZ transfer format

(1) Registers



(2) Block diagram



(3) Description of registers

(a) Serial mode control register (SMC)

This register is used to select the UART operation mode.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $002D_H$	PEN	SBL	MC1	MC0	SMDE	—	UCKE	UOE	$0000\ 0\text{-}00_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)		(R/W)	(R/W)	

[Bit 7] PEN: Parity enable

Bit 7 is used to determine whether to append a parity bit (when transmitting) or to detect it (when receiving) for serial data input/output.

0	No parity (default)
1	Parity (Odd or even parity is set by TD8/TP of the SSD register.)

[Bit 6] SBL: Stop bit length

Bit 6 is used to determine the stop bit length of transmit data. At the receiving end, only the first bit of the stop bit is recognized; second and later bits are ignored (default: 0).

0	2-bit length (default)
1	1-bit length

[Bits 5 and 4] MC1 and MC0: Mode control

Bits 5 and 4 are used to select the transfer mode (data length).

MC1	MC0	Mode	Data length
0	0	0	7 (6)
0	0	0	8 (7)
1	1	can not be used	can not be used
1	1	1	9 (8)

(Initial value)
Values in parentheses indicate the data length with parity.

[Bit 3] SMDE:

0	Synchronous transfer (default)
1	Asynchronous transfer

[Bit 1] UCKE: UART clock enable

When 1 is written at bit 1, the UART serial clock output pin is switched to the port to output an external synchronous clock pulse.

If the mode in which a synchronous clock pulse is input from the outside is set by the CS1 and CS0 bits of the SRC register, the value can also be read from the port as the input pin.

0	Port functions as general-purpose input/output port that does not output serial clock pulse. (default) When the port is set to input (DDR = 0), it also functions as a serial clock input pin.
1	Port functions as UART serial clock output pin.

In the external clock input mode, set this bit to 0.

[Bit 0] UOE: UART output enable

When 1 is written at bit 0, the port is switched to the UART serial data output pin to enable serial data output.

0	No parity (default)
1	Parity (Odd or even parity is set by TD8/TP of the SSD register.)

(b) Serial rate control register (SRC)

This register is used to control the data transfer speed (baud rate) of the UART.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $002E_H$	—	—	CR	SCS1	SCS0	RC2	RC1	RC0	$--01\ 1000_B$
			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 5] CR: Clock rate

Bit 5 is used to select the asynchronous transfer clock rate. However, when the CS1 and CS0 bits are $\mathbf{11_B}$, the 1/8 clock rate is selected irrespective of the value of the CR bit.

0	1/16 of clock input (default)
1	1/64 of clock input

Note: The synchronous transfer clock rate is as follows irrespective of the value of the CR bit:

Clock source — Internal clock 1/2.....1/2
Clock source — External clock, dedicated baud rate generator 1/1

[Bits 4 and 3] SCS1 and SCS0: Clock select

Bits 4 and 3 are used to select the clock input of the UART port. If the external or internal clock is selected as clock input, the baud rate is a 1/16 or 1/64 clock frequency according to the value of the CR bit (default: $\mathbf{11_B}$). For details, see 4.4.

[Bits 2 to 0] RC2 to RC0:

Bits 2 to 0 are needed only when generating a serial clock pulse with the dedicated baud rate generator. Fourteen baud rates can be selected by these bits (default: $\mathbf{000_B}$). For the baud rate setting, see 4.4.

(c) Serial status and data register (SSD)

This register is used to indicate the current status of the UART. When the data communication length is 9 bits, the most significant data (bit 8) is included.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $002F_H$	RDRF	ORFE	TDRE	TIE	RIE	PSEL	TD8/TP	RD8/RP	$0010\ 001X_B$
	(R)	(R)	(R)	(R/W)	(R/W)	(R/W)	(R/W)	(R)	

[Bit 7] RDRF:

The RDRF flag is used to indicate the data status of the serial input data register (SIDR).

0	Empty (default)
1	Contains data

When the SIDR register is read after reading the SSD register with the RDRF flag set to 1, the RDRF flag is cleared. When this flag is set to 1, the receiver interrupt request is output.

[Bit 6] ORFE:

The ORFE flag is used to indicate that an overrun or framing error has occurred. This flag is initialized to 0 at reset.

0	Normal
1	Error

If this flag is set, data is not transferred from the receive shift register to the SIDR register.

When the SIDR register is read after reading the SSD register with the ORFE flag set to 1, the ORFE flag is cleared. When this flag is set to 1, the receiver interrupt request is output.

The status of input data is specified by the RDRF and ORFE flags as follows:

RDRF	ORFE	SIDR data status
0	0	Empty
0	1	Framing error (If new data is input under this condition, RDRF is not set.)
1	0	Normal data
1	1	Overrun (previous data remains)

[Bit 5] TDRE:

The TDRE flag is used to indicate the status of the serial output data register (SODR).

0	Contains data
1	Empty (default)

When data is written to the SODR register after reading the SSD register with the TDRE flag set to 1, serial data is output from the SOUT pin.

When the TDRE flag is set to 1, a transmitter interrupt request is output.

[Bit 4] TIE: Transmitter interrupt request enable bit

Bit 4 is used to enable the transmitter interrupt request.

0	Interrupt disabled (default)
1	Interrupt enabled

[Bit 3] RIE: Receiver interrupt request enable bit

Bit 3 is used to enable the receiver interrupt request.

0	Interrupt disabled (default)
1	Interrupt enabled

[Bit 2] PSEL: Port select bit

Bit 2 is used to select the UART ports.

0	P30 to P32 selected (default)
1	P40 to P42 selected

[Bit 1] TD8/TP

When parity is not provided, bit 1 is treated as bit 8 of the SODR register. When parity is provided, this bit is used to determine whether the parity of serial output data is even or odd.

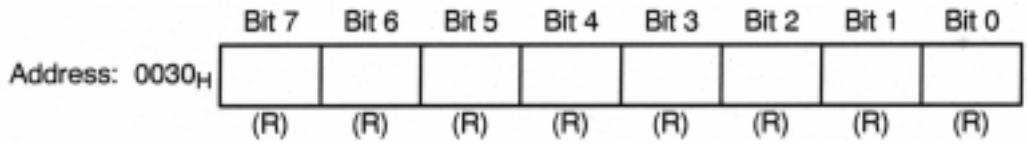
0	Odd parity
1	Even parity

[Bit 0] RD8/RP:

When parity is not provided, bit 0 is treated as bit 8 of the SIDR register. When parity is provided, this bit is used to determine whether the parity of serial input data is even or odd (default: undefined).

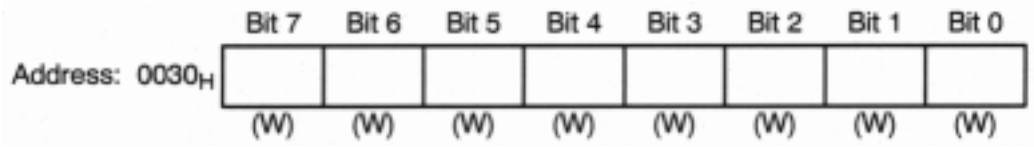
0	Odd parity
1	Even parity

(d) Serial input data register (SIDR)



The SIDR register is used for input of serial data (default: undefined).

(e) Serial output data register (SODR)



The SODR register is used for output of serial data (default: undefined).

(4) Description of operation

(a) Operation modes

The UART has the operation modes listed in Table 2-2; they can be switched by setting the value at the serial mode control register (SMC).

Table 2.8 Operation Modes of UART

Mode	Parity	Data length	Clock mode	Stop bit length
0	Provided	6	Asynchronous/synchronous	1 bit or 2 bits
	Not provided	7	Asynchronous/synchronous	1 bit or 2 bits
1	Provided	7	Asynchronous/synchronous	1 bit or 2 bits
	Not provided	8	Asynchronous/synchronous	1 bit or 2 bits
2	Can not be used			
3	Provided	8	Asynchronous/synchronous	1 bit or 2 bits
	Not provided	9	Asynchronous/synchronous	1 bit or 2 bits

However, the stop bit length can be specified only for the transmitter channel. The 1-bit length is always specified for the receiver channel.

(b) Interrupt occurrence and flag setting conditions

The UART has three flags and two interrupt sources.

The three flags are ORFE, RDRF, and TDRE. The ORFE flag is an overrun/framing error flag which is set when an error occurs at receiving. The RDRF flag indicates that the receive data is ready at the SIDR register. The TDRE flag indicates that writing to the transmit data register (SODR) is enabled.

The two interrupt sources are one for receiving, and one for transmitting. At receiving, an interrupt is requested by the RDRF or ORFE flag. At transmitting, an interrupt is requested by the TDRE flag.

- Receiving in modes 0, 1, and 3

Both the RDRF (receive data register full) and ORFE (overrun/framing error) flags are set when receiving and transfer are completed and the last stop bit is detected. An interrupt request is then output to the CPU. When the RDRF flag is active, the received data is transferred to the serial data input register (SIDR).

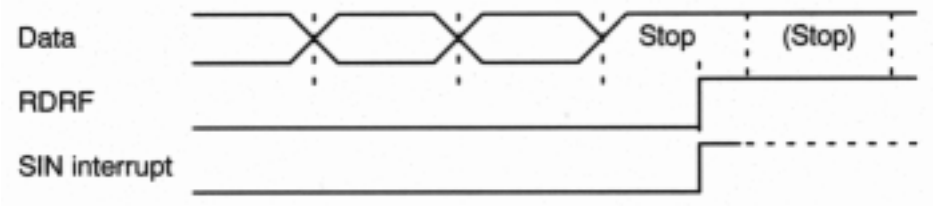


Fig. 2.9 RDRF Flag Set Timing

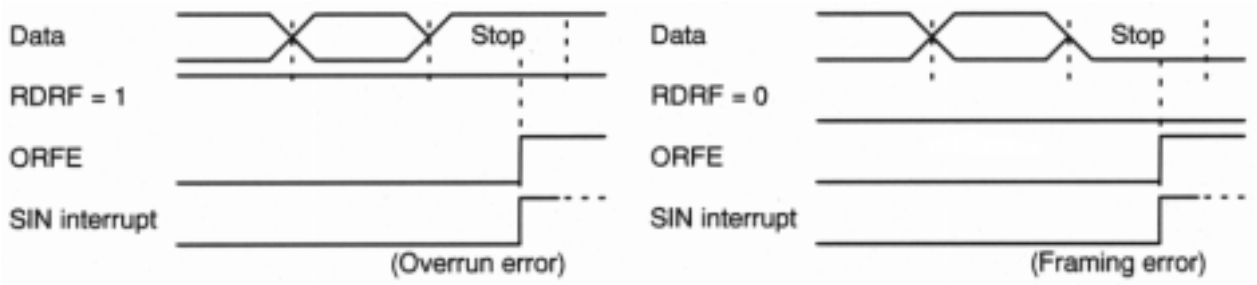


Fig. 2.10 ORFE Flag Set Timing

• Transmission

When the next data is ready to write after data written to the serial output data register (SODR) is trans ferred to the interrupt shift register, the TDRE (transmit data register empty) flag is set and an interrupt request is output to the CPU.

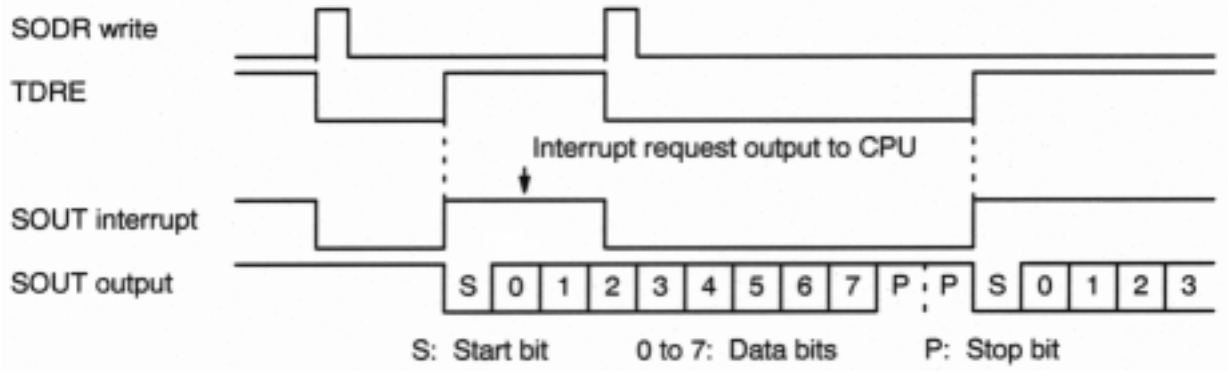


Fig. 2.11 TDRE Flag Set Timing (Mode 0)

(c) Transfer data format

The UART can handle only NRZ (non-return-to-zero)-type data. The relationship between transmitter/re ceiver clocks and data is shown in the figure below.

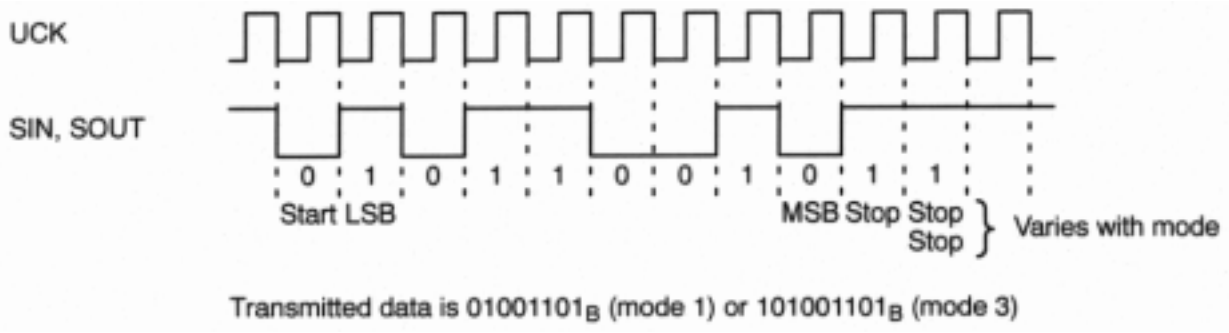


Fig. 2.4 Transfer Data Format

As shown in the figure, data transfer starts from the start bit (Low-level data), the data bit length specified by the LSB first is transferred, and transfer ends at the stop bit (High-level data).

In asynchronous transfer, the relationship between UCK and SIN is not as shown in the above figure. In addition, at asynchronous transfer, the relationship is not as shown in the above diagram even when UCK is set to input.

(d) Transfer clock selection

The transfer clock can be selected from the external clock (UCK pin), two internal clocks (PTO1 and PTO2), and the dedicated baud rate generator. This selection is done by the SCS0, SCS1, and CR bits of the serial rate control register (SRC). The division ratios are listed in Table 2-3.

Table 2.9 Clock Division Ratio

SCS1	SCS0	Clock input	CR	Asynchronous	Synchronous
0	0	External clock	0	1/16	1/1
			1	1/64	
0	1	PWM timer 1	0	1/16	1/2
			1	1/64	
1	0	PWM timer 2	0	1/16	1/2
			1	1/64	
1	1	Dedicated baud rate	—	1/8	1/1

The transfer clocks when using the dedicated baud rate generator are listed in Table 2-4.

Table 2.10 Baud Rate Selection

RC2	RC1	RC0	CLK asynchronous (μs/baud)	CLK synchronous (μs/baud)
0	0	0	104/9615	1 /1 M
0	0	1	208/4808	2/500 K
0	1	0	416/2404	4/250 K
0	1	1	832/1202	8/125 K
1	0	0	1664/601	16/62.5 K
1	0	1	3228/300	32/31.25 K
1	1	0	16/62500	2/500 K
1	1	1	128/7813	16/62.5 K

(At 10-MHz oscillation)

Note: After canceling register initialization by a reset, initialization of the internal control section requires an initialization time of 11 shift clocks.

(e) Expression for Calculating Dedicated Baud Rate (UART)

The dedicated baud rate is determined by the settings of the clock gear, clock division ratio registers (SCS1 and SCS0), and baud rate select registers (RC2, RC1 and RC0). The baud rate is calculated as follows:

fch: Frequency of original oscillation

$$\frac{1}{\text{Baud rate}} = \boxed{\begin{matrix}\text{Clock gear selection}\\ 64/f\,ch\\ 16/f\,ch\\ 8/f\,ch\\ 4/f\,ch\end{matrix}} \times 10/4 \times \boxed{\begin{matrix}\text{Clock division ratio}\\ (SCS1, SCS0)\end{matrix}} \times \boxed{\begin{matrix}\text{Baud rate selection}\\ (RC2, RC1, RC0)\end{matrix}}$$

[ex]

$$\frac{1}{9615\ \text{baud}} = 0.4\ \mu s\ (4/f\,ch) \times 10/4 \times 8\ (\text{asynchronous mode}) \times 13\ (RC2 = RC1 = TC0 = 0)$$

(fch = 10 MHz)

• Clock division ratio (SCS1, SCS0)

When using a dedicated baud rate, set the clock division ratio register SCS1 to 1 and SCS0 to 0. The clock division ratio results in 1/8 in the asynchronous mode.

SCS1	SCS0	Clock input	Asynchronous mode
1	1	Dedicated baud rate	1/8

• Baud rate selection (RC2, RC1, RC0)

The baud rates can be selected depending on the settings of RC2, RC1, and RC0. For example, the baud rates at an original oscillation of 10 MHz are listed in the following table.

RC2	RC1	RC0	Division ratio selected as baud rate	CLK in asynchronous mode (µs/baud)
0	0	0	13	104/9615
0	0	1	26	208/4808
0	1	0	52	416/2404
0	1	1	104	832/1202
1	0	0	208	1664/601
1	0	1	416	3328/300
1	1	0	2	16/62500
1	1	1	16	128/7813

(Original oscillation: 10 MHz)

(f) Expression for Calculating Baud Rate (UART)

The baud rate is determined by the clock input selected by the clock division ratio registers (SCS1 and SCS0). The clock inputs of the external clock and the PWM timer 1/PWM timer 2 are selectable. Each expression for calculating baud rate is given below.

- External clock selected

fch: Frequency of original oscillation

$$\frac{1}{\text{Baud rate}} = \text{External clock input (min: 8/fch X 2)} \times CR \left(\begin{array}{l} CR = 0 \ldots\ldots 16 \\ CR = 1 \ldots\ldots 64 \end{array} \right)$$

[ex]

$$\frac{1}{\text{36 K baud}} = 1.6\ \mu s \text{ (min. value)} \times 16\ (CR = 1)$$

(fch = 10 MHz)

- PWM timer 1/PWM timer 2 selected

Clock gear selection: 64/f ch, 16/f ch, 8/f ch, 4/f ch

Input clock select bit (PWM timer) (SC11 = SC21/SC10 = SC20): 1 (SC11 = 0, SC10 = 0), 8 (SC11 = 0, SC10 = 1), 16 (SC11 = 1, SC10 = 0), 64 (SC11 = 1, SC10 = 1)

Compare register (COMR1/COMR2): Compare register value + 1

fch: Frequency of original oscillation

$$\frac{1}{\text{Baud rate}} = \text{Clock gear selection} \times \text{Input clock select bit} \times \text{Compare register value} + 1 \times 2 \times CR \left(\begin{array}{l} CR = 0 \ldots 16 \\ CR = 1 \ldots 64 \end{array} \right) \text{ (Cycle)}$$

[ex 1]

$$\frac{1}{\text{75 K baud}} = 0.4\ \mu s\ (4/f\ ch) \times 1(SC11 = 0, SC10 = 0) \times 1\ (COMR1 = 0) \times 2 \times 16\ (CR = 0)$$

(fch = 10 MHz)

[ex 2]

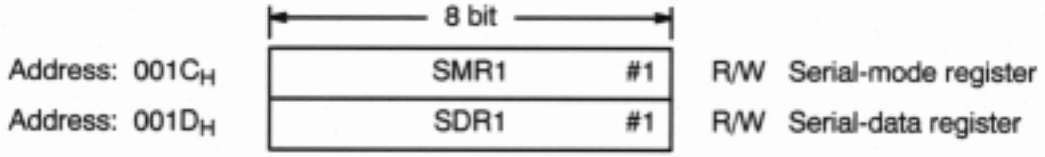
$$\frac{1}{\text{19531 baud}} = 0.4\ \mu s\ (4/f\ ch) \times 1(SC11 = 0, SC10 = 0) \times 4\ (COMR1 = 3) \times 2 \times 16\ (CR = 0)$$

(fch = 10 MHz)

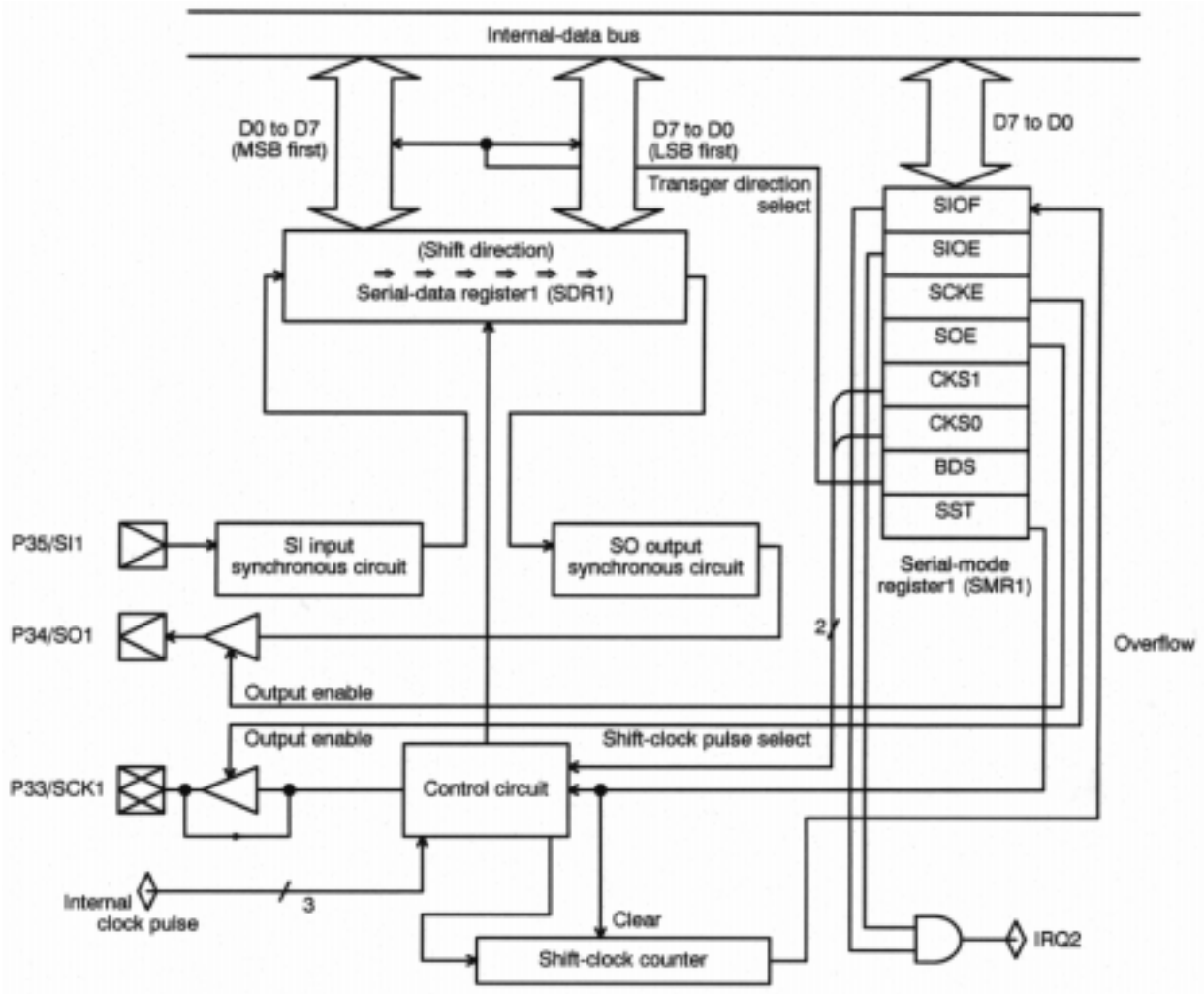
2.2.6 8-bit Serial I/O 1

- 8-bit serial data transfer is possible by the clock synchronous method.
- LSB first or MSB first can be selected for data transfer.
- Four shift-clock modes (three internal and one external) can be selected.

(1) Registers



(2) Block diagram



(3) Description of registers

(a) Serial-mode register 1 (SMR1)

The SMR1 is used to control serial I/O.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $001C_H$	SIOF	SIOE	SCKE	SOE	CKS1	CKS0	BDS	SST	$0000\ 0000_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] SIOF: Serial I/O interrupt-request flag

Bit 7 indicates the serial I/O transfer state.

The meaning of each bit to be read is as follows:

0	Serial data transfer not terminated
1	Serial data transfer terminated

Note that 1 is always read when the Read Modify Write instruction is read. If this bit is set when an interrupt is enabled (SIOE = 1), an interrupt request is output to the CPU.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

The end-of-transfer decision may be made by either the SST bit (bit 0) of the SMR or by this bit.

[Bit 6] SIOE: Serial I/O interrupt-enable bit

Bit 6 is used to enable a serial I/O interrupt request.

0	Serial I/O interrupt-output disable
1	Serial I/O interrupt-output enable

[Bit 5] SCKE: Shift-clock output-enable bit

Bit 5 is used to control the shift-clock I/O pins.

0	General-purpose port pins (P33) or SCK1 input pin
1	SCK1 (shift clock) output pin

When using the P33/SCK1 and P55/SCK2 pins as external clocks, always set the DDR to input (bit 3 of DDR3 = 0).

[Bit 4] SOE: Serial-data output-enable bit

Bit 4 is used to control the output pins for serial I/O.

0	General-purpose port pins (P34)
1	SO (serial data) output pin

When using P35/SI1 and P57/SI2 pins as the SI pin, always set the DDR to input (bit 3 of DDR3 = 0).

[Bits 3 and 2] CKS1 and CKS0: Shift-clock select bits

Bits 3 and 2 are used to select the serial shift-clock modes.

CKS1	CKS0	Mode	(Clock rate)	SCK
0	0	Internal shift-clock mode	(1/2 instruction cycle)	Output
0	1	Internal shift-clock mode	(1/8 instruction cycle)	Output
1	0	Internal shift-clock mode	(1/32 instruction cycle)	Output
1	1	External shift-clock mode	(SCK1)	Input

[Bit 1] BDS: Transfer direction select bit

At serial data transfer, Bit 1 is used to select whether data transfer is performed from the least significant bit first (LSB first) or from the most significant bit first (MSB first).

0	LSB first
1	MSB first

Note that when this bit is rewritten after writing data to the SDR, the data become invalid.

[Bit 0] SST: Serial I/O transfer-start bit

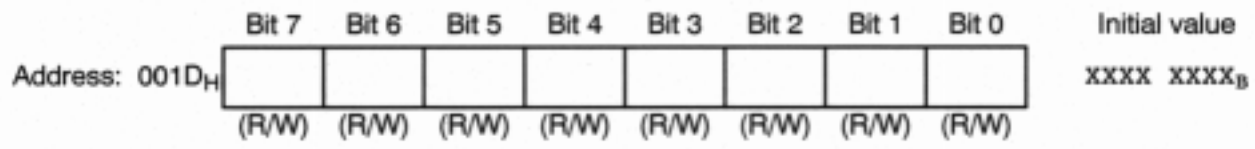
Bit 0 is used to start serial I/O transfer. The bit is automatically cleared to 0 when transfer is terminated.

0	Serial I/O transfer stop
1	Serial I/O transfer start

Before starting transfer, ensure that transfer is stopped (SST = 0).

(b) Serial-data register 1 (SDR1)

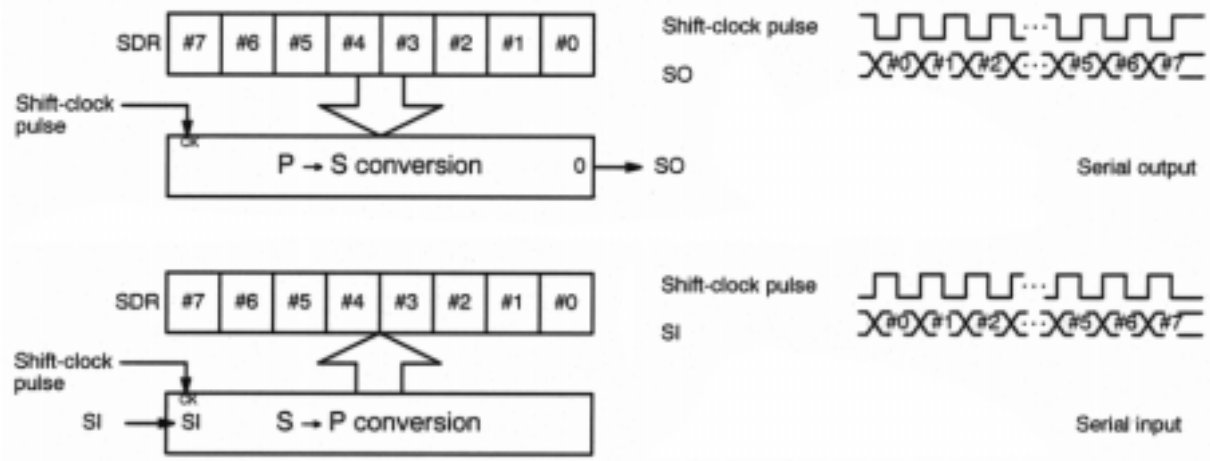
This 8-bit register is used to hold serial I/O transfer data. Do not write data to this register during the serial I/O operation.



(4) Description of operation

(a) Outline

This module consists of the serial-mode register (SMR) and serial-data register (SDR). At serial output, data in the SDR is output in bit serial to the serial output pin (SO) in synchronization with the falling edge of a serial shift-clock pulse generated from the internal or external clock. At serial input, data is input in bit serial from the serial input pin (SI) to the SDR at the rising edge of a serial shift-clock pulse.



(b) Operation modes

The serial I/O has three internal shift-clock modes and one external shift-clock mode, which are specified by the SMR. Mode switching or clock selection should be made with serial I/O stopped (SST bit (bit 0) of SMR = 0).

(1) Internal shift-clock mode

Operation is performed by the internal clock. A shift-clock pulse with a duty of 50% is output from the $\overline{SCK}$ pin as a synchronous timing output. Data is transferred bit-by-bit at every clock pulse.

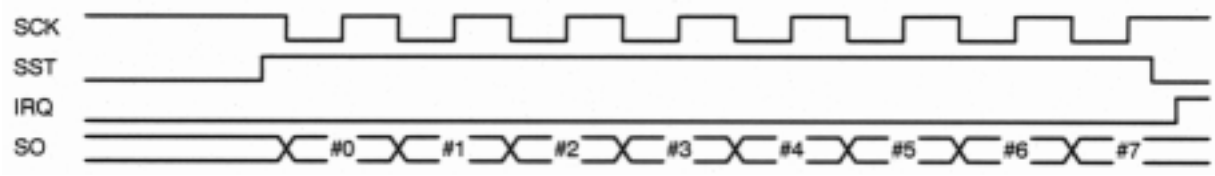
(2) External shift-clock mode

Data is transferred bit-by-bit at every clock pulse in synchronization with the external shift-clock pulse input from the $\overline{SCK}$ pin. If an external clock is input when the SST bit is set to 0, no shift operation occurs and data of the SDR register (or the value of bit 7 when MSB first used) is output to the SO pin. However, the pin value is also rewritten when the SDR register data is rewritten. The transfer speed can be from DC to 1/2 oscillation (two instruction cycles). When one instruction cycle is 0.4µs (at 10 MHz oscilla tion), the transfer speed can be up to 1.25 MHz.

Do not write data to the SMR and SDR during the serial I/O operation in either mode.

(c) Interrupt functions

This module can output an interrupt request to the CPU. To output an interrupt request, set the SIOE bit (bit 6) of the SMR to 1 to enable an interrupt and then set the interrupt flag SIOF (bit 7) of SMR after 8-bit data transfer is terminated.

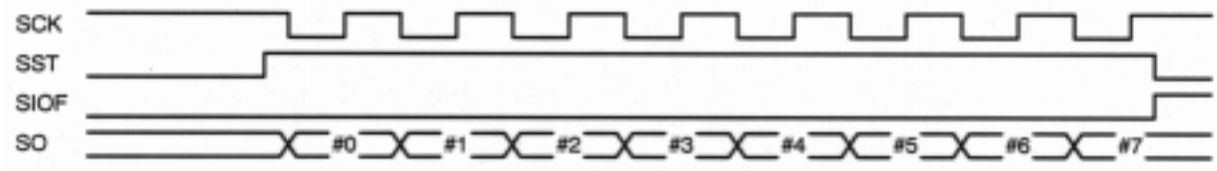


(d) Shift start/stop timing

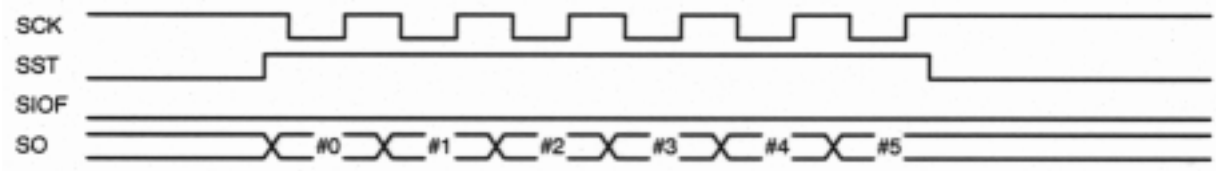
Data transfer starts when 1 is written at the SST bit (bit 0) of the SMR, and stops when 0 is written. When data transfer is terminated, the SST bit is automatically cleared to 0, which stops the operation.

(1) Internal shift-clock mode (LSB first)

[When transfer terminated]

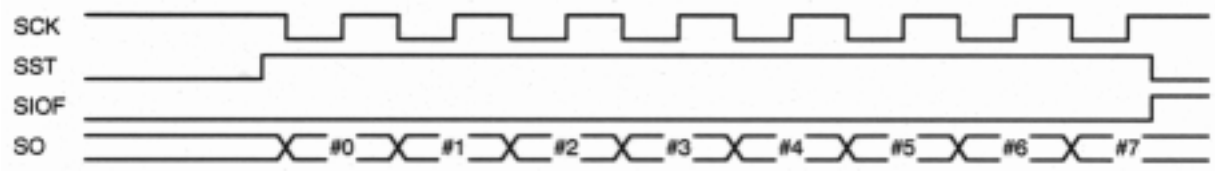


[When transfer suspended]

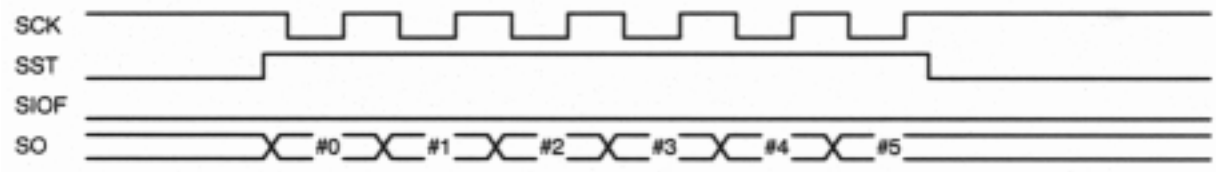


(2) External shift-clock mode (LSB first)

[When transfer terminated]



[When transfer suspended]



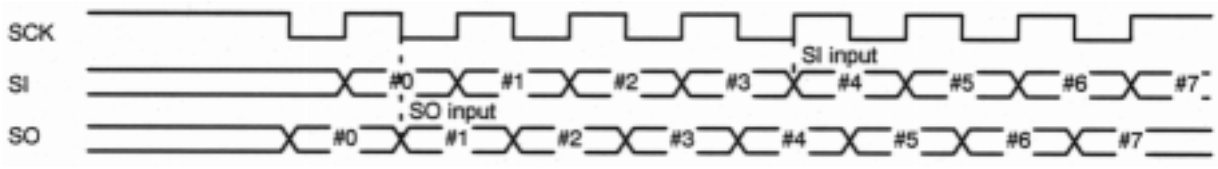
Note: When data is written at the SDR, the output data changes at the falling edge of the external-clock pulse.

Fig. 2.12 Shift Start/Stop Timing

(e) Input/output shift timing

Data is output from the serial output pin (SO) at the falling edge of the shift-clock pulse, and is input from the serial input pin (SI) to the SDR at the rising edge of the shift-clock pulse.

(1) LSB first (BDS = 0)



(2) MSB first (BDS = 1)

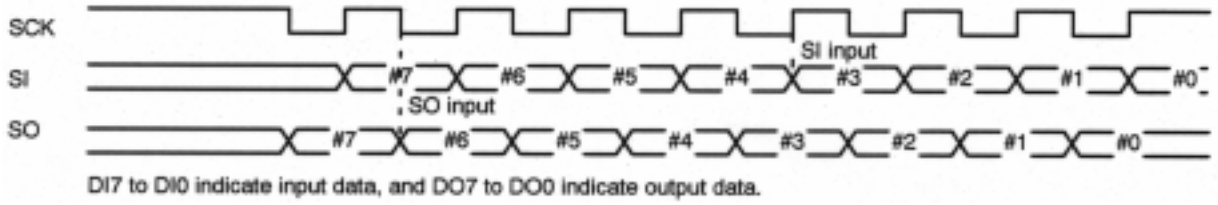


Fig. 2.13 Input/Output Shift Timing

2.2.7 10-bit A/D Converter

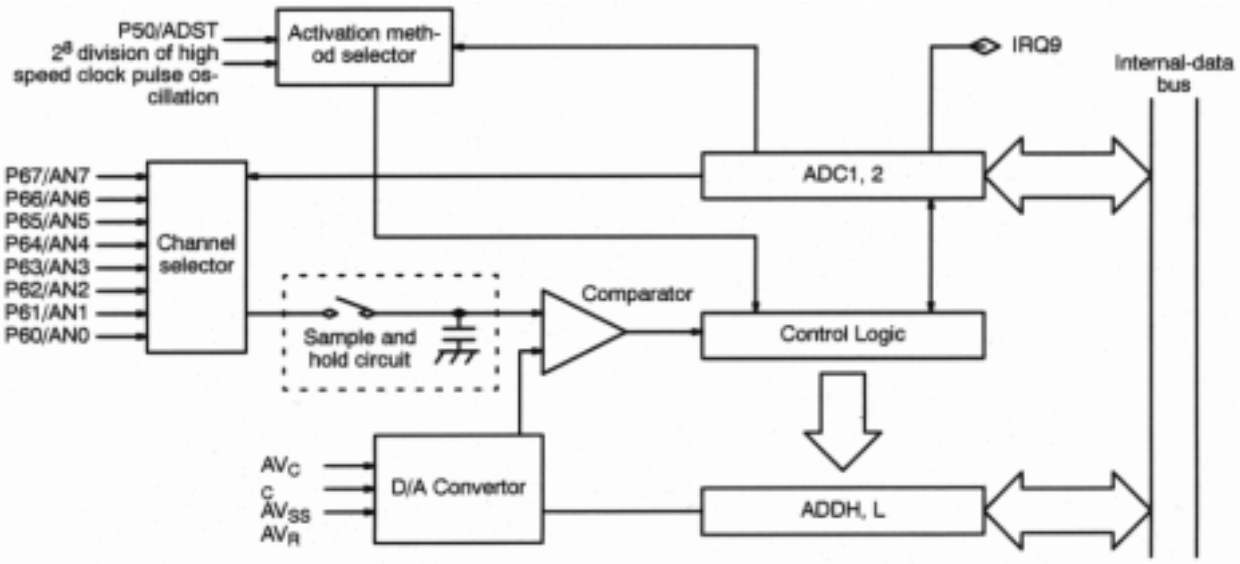
This is an 10-bit sequential-comparison A/D converter. This register has the following features:

- A/D conversion time: 33 instruction cycles 13.2 µs (at 10 MHz oscillation)
- Sense function: Compare time 18 instruction cycles 7.2 µs at 10 MHz.
  - The sense function compares the preset value in the data register with the analog input value.
- Start by program or continuous start external input clock selectable
- End detection enabled by interrupt or software polling

(1) Registers

	8 bit	
Address: 0020_H	ADC1	R/W A/D control-status register 1
Address: 0021_H	ADC2	R/W A/D control-status register 2
Address: 0022_H	ADDH	R/W A/D data register H (Upper 2 bits)
Address: 0023_H	ADDL	R/W A/D data register L (Lower 2 bits)

(2) Block diagram



(3) Description of registers

(a) A/D converter control register 1 (ADC1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0020_H	ANS3	ANS2	ANS1	ANS0	ADI	ADMV	SIFM	AD	$0000\ 0000_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	(R/W)	

[Bits 7 to 4] AN3 to AN0: Analog-input channel select bits

These four bits are used to select analog-input channel.

ANS3	ANS2	ANS1	ANS0	Select channel	ANS3	ANS2	ANS1	ANS0	Select channel
0	0	0	0	AN0	0	0	0	0	—
0	0	0	1	AN1	0	0	0	1	—
0	0	1	0	AN2	0	0	1	0	—
0	0	1	1	AN3	0	0	1	1	—
0	1	0	0	AN4	0	1	0	0	—
0	1	0	1	AN5	0	1	0	1	—
0	1	1	0	AN6	0	1	1	0	—
0	1	1	1	AN7	0	1	1	1	—

[Bit 3] ADI: Interrupt-flag bit

The meaning of each bit to be read in the A/D mode is as follows:

0	Conversion not terminated.
1	Conversion terminated.

The meaning of each bit to be read in the sense mode is as follows:

0	Conditions specified by SIFM bit not met
1	Conditions specified by SIFM bit met

In both the A/D and sense modes, an interrupt request is output if these bits are set when the ADIE bit (bit 4) of the ADC2 is 1.

The meaning of each bit to be written in both the A/D and sense modes is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

1 is always read when the Read Modify Write instruction is read.

[Bit 2] ADMV: Conversion-on/comparison-on flag

This flag indicates that A/D conversion/comparison is in progress.

0	Conversion/comparison not in progress
1	Conversion/comparison in progress

[Bit 1] SIFM: Interrupt-source setting bit

Bit 1 is used to set the conditions for setting the interrupt source in the sense mode.

0	Set interrupt source when analog input value lower than the value set by the data register.
1	Set interrupt source when analog input value higher than the value set by the data register.

[Bit 0] AD: A/D conversion start bit

When the EXT bit (bit 1) of the ADC2 is 0, writing 1 at this bit starts the A/D conversion in both the A/D and sense modes. Writing 0 at this bit does not make sense. 0 is always read.

The meaning of each bit to be written is as follows:

0	No A/D conversion
1	A/D conversion start (when EXT (bit 1) of ADC2 is 0)

(b) A/D converter control and status display register 2 (ADC2)

The ADC2 is used to control the A/D converter and display its status.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0021_H	—	TIM1	TIM0	ADCK	ADIE	ADMD	EXT	TEST	$X000\ 0001_B$
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bits 6 and 5] TIM1 and 0: Reserved bits

Always set 00 at these bits.

TIM1	TIM0	Conversion time at 10 MHz	Compara time at 10 MHz
0	0	33 instruction cycles (13.2 μs)	18 instruction cycles (7.2 μs)

[Bit 4] ADCK: External input-clock pulse-select bit

Bit 4 is used to select the external input clock pulse for starting A/D conversion.

0	2^8 division of high speed clock oscillation
1	Input to P50/ADST

When using the external-clock input, set the DDR of P30 to input.

[Bit 3] ADIE: Interrupt-enable specifying bit

Bit 3 is used to specify interrupt enable/disable.

0	Interrupt disabled
1	Interrupt enabled

[Bit 2] ADMD: Function select bit

Bit 2 is used to select the A/D mode and sense mode.

0	A/D mode
1	Sense mode

[Bit 1] EXT: Conversion select bit

Bit 1 is used to select starting method of A/D conversion.

0	Start by AD (bit 0) of ADC1
1	Start at rising edge of clock pulse selected by ADCK (bit 4) of ADC2

[Bit 0] TEST: Testing bit

Bit 0 is used only for testing. Always write 1 at this bit. 1 is always read.

(c) A/D data registers H and L (ADDH, ADDL)

These registers store the results of A/D conversion in A/D mode. They write the setting value for the com parison in it in sense mode. Upper 2 bits and Lower 8 bits assigned to ADDH and ADDL, respectivery.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0022_H									XXXX XXXX$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0023_H	7	6	5	4	3	2	1	0	XXXX XXXX$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- A/D mode

  In the A/D mode, the results are stored as soon as the A/D conversion is terminated. After the conversion, the contents of the register are held until next conversion is started. Once started, the value becomes undefined. Therefore, always read the data after the end of conversion.

- Sense mode

  In the sense mode, the vale to be compared with the converted value is written in these registers in ad vance. The contents set in the register are held without changing by the comparison operation.

Do not write data during conversion in either the A/D or sense mode.

(4) Description of operation

(a) A/D mode

(1) Start or restart by program

Writing 0 at the ADMD bit (bit 2) of the ADC2 gives the A/D mode. Writing 1 at the AD bit (bit 0) of the ADC1 starts the A/D conversion. If 1 is written at the AD bit (bit 0) of ADC1 during A/D conversion, the conversion operation is canceled and restarted.

(2) Start/restart by external clock

Writing 1 at EXT (bit 1) of ADC2 sets the AD mode to wait for starting by the external clock. A/D conver sion is started after detecting the rising edge of the clock pulse selected by the ADCK bit (bit 4) of ADC2. If the rising clock pulse occurs during the operation, the conversion operation is canceled and restarted. When the external clock is used for starting or restarting by setting EXT (bit 1) to 1, A/D conversion cannot be started or restarted by the program.

(3) End

When A/D conversion is terminated, the result of the operation is stored in the data register and AD1 (bit 3) of ADC1 is set. At that time, an interrupt request is output when ADIE (bit 2) of ADC2 is 1.

The conversion result is stored in the data register until next conversion starts. Therefore, read the conversion result before starting the next conversion. The result stored in the register is lost when the operation is restarted.

(4) Continuous start of AD conversion by external clock

The A/D conversion can be started continuously by providing an external clock based on the conver sion time and operation result reading time.

(b) Sense Mode

(1) Comparison/recomparison by program

Preprogram a specified comparison value in the data register.

Writing 1 at ADMD (bit 2) of ADC2 gives the sense mode. Writing 1 at AD (bit 0) of ADC1 starts compari son. If 1 is written at AD (bit 0) of ADC1 during comparison, the operation is canceled and restarted.

(2) Comparison/recomparison by external clock

Preprogram a specified comparison value in the data register.

Writing 1 at EXT (bit 1) of ADC2 sets the sense mode to wait for starting by the external clock. Compari son is started at after detecting rising edge of the clock pulse selected by the ADCK bit (bit 4) of ADC2. If the rising clock pulse occurs during the operation, comparison is canceled and restarted. When the external clock is used for comparison or recomparison, comparison and recomparison cannot be exe cuted by the program.

(3) End

When the result of the comparison meets the conditions specified by SIFM (bit 1) of ADC1, ADI (bit 3) of ADC1 is set. At that time, an interrupt request is output when ADIE (bit 2) of ADC2 is 1. If the result of the operation does not meet the specified conditions, ADI (bit 3) of ADC1 is not set. In this case, check that ADMV (bit 2) of ADC1 is 0.

The preset contents of the data register are held without loss by the comparison operation.

(4) Continuous start of comparison by external clock

Comparison can be started continuously by providing an external clock based on the comparison time.

(5) Precautions for A/D converter

(a) The A/D conversion and comparison are stopped and all registers are initialized by a reset. The operating flag bit [ADMV (bit 2) of ADC1] is cleared and other bits are not changed.

(b) Activation cannot be performed by the program [AD (bit 1) of ADC1] when an external-clock start is selected.

(c) Do not rewrite each register during conversion and comparison. When an external-clock start is selected, change the settings of the registers after writing 0 at EXT (bit 1) of ADC2 when operation is stopped [ADMV (bit 2) of ADC1 is 0] to inhibit an external-clock start. However, when program starting is selected [AD (bit 1) of ADC1], the analog input channel can be reselected and the inter rupt source for the sense mode can be switched at reset.

(d) Switch the A/D or sense mode after clearing the ADI interrupt flag (bit 3) of ADC1.

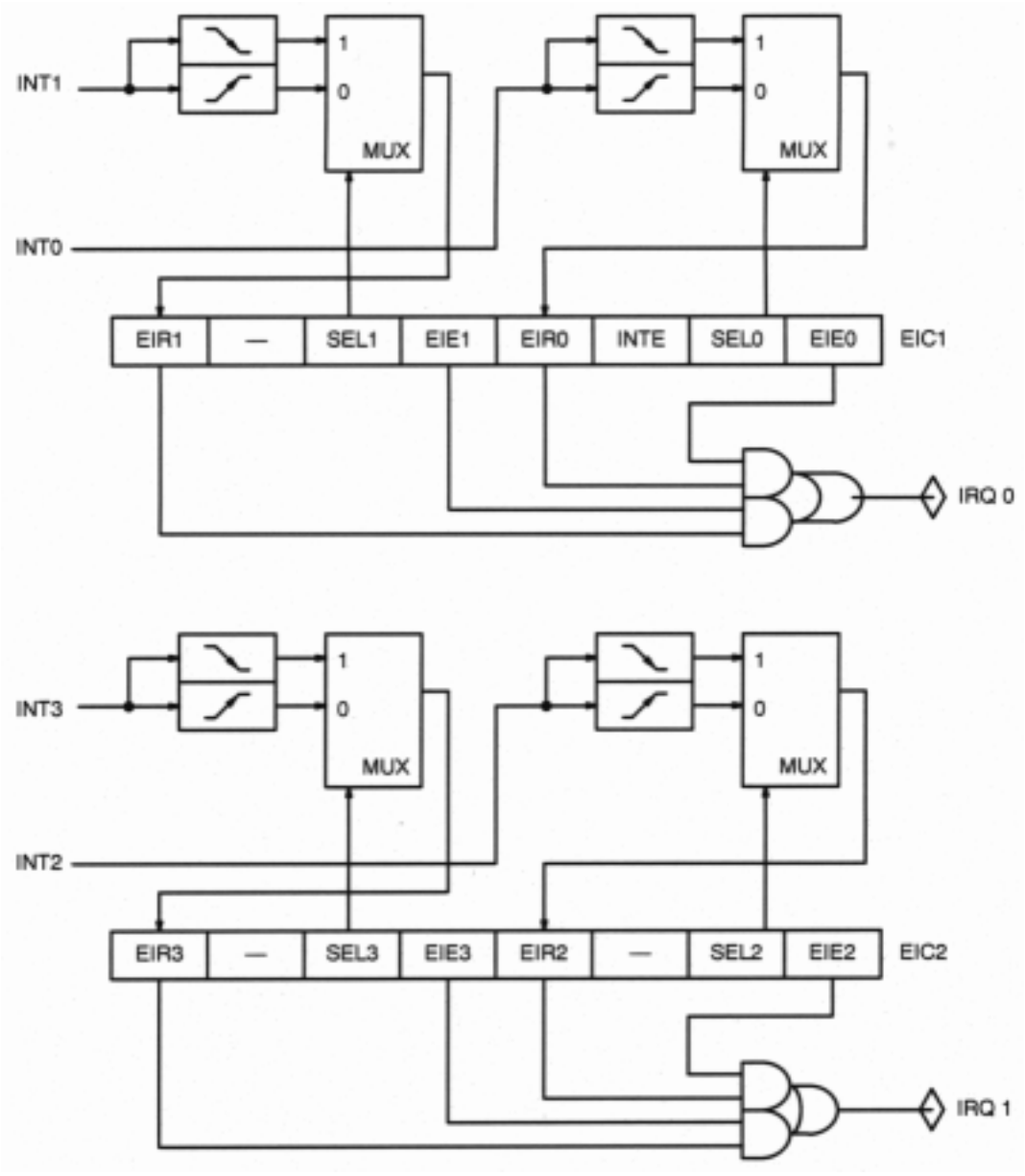
(e) To perform continuous conversion or comparison by an external clock, provide the clock based on the conversion or comparison time and the operation result reading time. The A/D conversion re sult is valid until the next conversion is started. The value set in the data register in the sense mode is held without loss by the comparison operation.

2.2.8 External Interrupt Circuit

- The edges of four external-interrupt sources (INT0 to INT3) can be detected to set the corresponding flag.
- An interrupt can be generated at the same time the flag is set.
- The four interrupts can release the STOP, SLEEP or watch mode.

(1) Registers

(2) Block diagram



(3) Description of registers

(a) External-interrupt 1 control register 1 (EIC1)

The EIC1 controls interrupts by the INT0 and INT1 pins.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0024_H	EIR1	—	SEL1	EIE1	EIR0	INTE	SEL0	EIE0	$0X00\ 0000_B$
	(R/W)		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Note: The bit manipulation instructions (Read Modify instructions) should not be used for this register.

[Bit 7] EIR1: External-interrupt request flag

When the edge specified by the SEL1 bit is input to the INT1 pin, bit 7 is set to 1. When the EIE1 bit is 1, an interrupt request (IRQ0) is output if this bit is set.

The meaning of each bit to be read is as follows:

0	Specified edge not input to INT1 pin
1	Specified edge input to INT1 pin (IRQ0 is output.)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 5] SEL1: Edge-polarity select bit

Bit 5 is used to control the input edge polarity of the INT1 pin.

0	Rising edge
1	Falling edge

[Bit 4] EIE1: Interrupt-enable bit

Bit 4 is used to enable an external-interrupt request by the INT1 pin.

0	Interrupt request disabled
1	Interrupt request enabled by EIR1 setting

[Bit 3] EIR0: External-interrupt request flag

When the edge specified by the SEL0 bit is input to the INT0 pin, bit 3 is set to 1. When the EIE0 is 1, an interrupt request (IRQ0) is output if this bit is set.

The meaning of each bit to be read is as follows:

0	Specified edge not input to INT0 pin
1	Specified edge input to INT0 pin (IRQ0 is output.)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 2] INTE: Testing bit

Bit 2 is used only for testing. Always write 0 in this bit.

[Bit 1] SEL0: Edge-polarity select bit

Bit 1 is used to control the input edge polarity of the INT0 pin.

0	Rising edge
1	Falling edge

[Bit 0] EIE0: Interrupt-enable bit

Bit 0 is used to enable an external-interrupt request by the INT0 pin.

0	Interrupt request disabled
1	Interrupt request enabled by EIR0 setting

(b) External-interrupt control register 2 (EIC2)

The EIC2 controls an interrupt by the INT2 and INT3 pins.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0025_H	EIR3	—	SEL3	EIE3	EIR2	—	SEL2	EIE2	$0X00\ 0X00_B$
	(R/W)		(R/W)	(R/W)	(R/W)		(R/W)	(R/W)	

[Bit 7] EIR3: External-interrupt request flag

When the edge specified by the SEL3 bit is input to the INT3 pin, bit 7 is set to 1. When the EIE3 bit is 1, an interrupt request (IRQ1) is output if this bit is set.

The meaning of each bit to be read is as follows:

0	Specified edge not input to INT3 pin
1	Specified edge input to INT3 pin (IRQ1 is output.)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 5] SEL3: Edge-polarity select bit

Bit 5 is used to control the input edge polarity of the INT3 pin.

0	Rising edge
1	Falling edge

[Bit 4] EIE3: Interrupt-enable bit

Bit 4 is used to enable an external-interrupt request by the INT3 pin.

0	Interrupt request disabled
1	Interrupt request enabled by setting of EIR3

[Bit 3] EIR2: External-interrupt request flag

When the edge specified by the SEL2 bit is input to the INT2 pin, bit 3 is set to 1. When the EIE2 is 1, an interrupt request (IRQ2) is output if this bit is set.

The meaning of each bit to be read is as follows:

0	Specified edge not input to INT2 pin
1	Specified edge input to INT2 pin (IRQ1 is output.)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 1] SEL2: Edge-polarity select bit

Bit 1 is used to control the input edge polarity of the INT2 pin.

0	Rising edge
1	Falling edge

[Bit 0] EIE2: Interrupt-enable bit

Bit 0 is used to enable an external-interrupt request by the INT2 pin.

0	Interrupt request disabled
1	Interrupt request enabled by setting of EIR2

(4) Precautions for external-interrupt circuit

When enabling an interrupt after clearing reset, always clear the interrupt flag simultaneously. An interrupt request is output immediately when the interrupt flags (EIR3, EIR2, EIR1, EIR0) are set to 1.

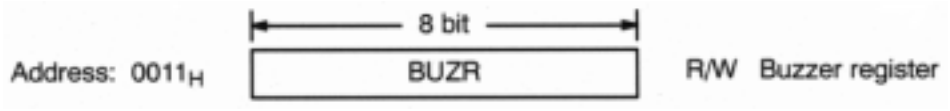
Don't use INT0 and INT1 when double clock operation is specified.

If an interrupt is selected on the rising edge, the pull-up option for the pin should not be used.

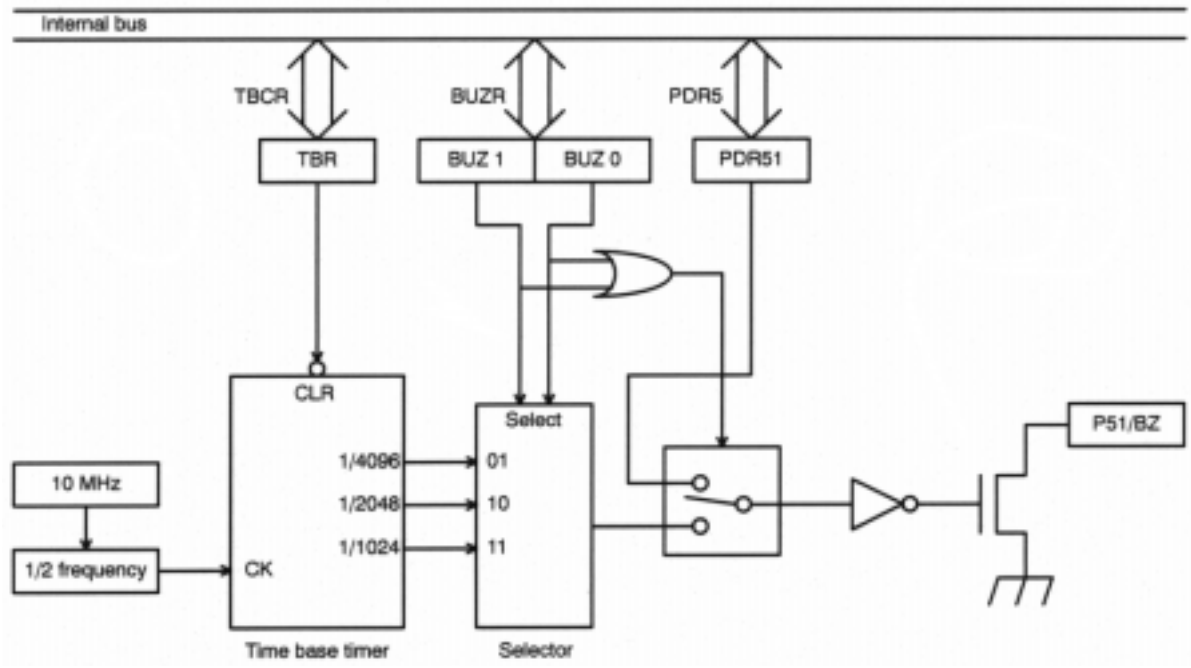
2.2.9 Buzzer Output Circuit

- The buzzer output sound for checking key input can be output from port 51.
- Three frequencies can be output by setting the registers.

(1) RegistersTBTC



(2) Block diagram



(3) Detailed description of registers

(a) Buzzer register (BUZR)

This 8-bit register enables buzzer output and selects the frequency.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0011_H	—	—	—	—	—	—	BUZ1	BUZ0	XXXX $XX00_B$
							(R/W)	(R/W)	

[Bits 1 and 0] BUZ1 and BUZ0: Buzzer-select bits

Bits 1 and 0 are used to enable buzzer output and select the frequency. The buzzer output function is disabled by 00 and the port operates normally. In other cases, the frequencies listed in the table below are selected.

Table 2.11 Buzzer Output Frequencies (at 10 MHz Oscillation)

BUZ1	BUZ0	Buzzer output frequency
0	0	General-purpose port operation
0	1	1220 Hz
1	0	2441 Hz
1	1	4883 Hz

(4) Description of operation

This circuit outputs a signal for use as a check sound. The buzzer register is used to enable buzzer output and select the frequency. When values other than 00 are set at the BUZR register, the square wave of the set frequency is output at the port.

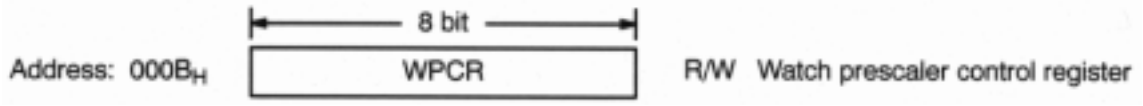
(5) Precautions for buzzer output circuit

Part of the time-base timer is used as the buzzer output. Therefore, clearing the time-base timer affects the circuit.

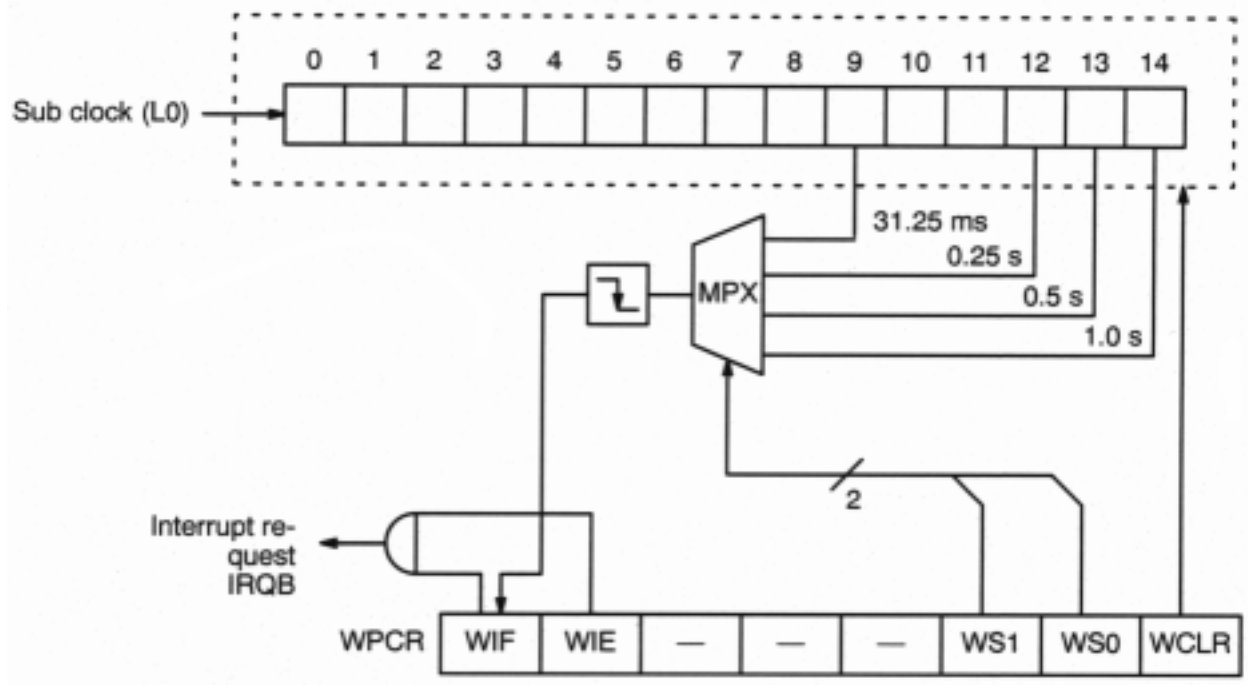
2.2.10 Watch Prescaler

- This prescaler has a 15-bit binary counter
- Four interval times can be selected.
- This function cannot be used when the single clock module is selected by the mask option.

(1) Registers



(2) Block diagram



(3) Description of registers

(a) Watch prescaler control register (WPCR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $000B_H$	WIF	WIE	—	—	—	WS1	WS0	WCLR	$00XX\ X000_B$
	(R/W)	(R/W)				(R/W)	(R/W)	(R/W)	

[Bit 7] WIF: Watch interrupt flag

When writing, this bit is used to clear the watch interrupt flag.

0	Clears watch interrupt flag
1	No operation

When reading, this bit indicates that the watch interrupt has occurred.

0	Watch interrupt not occurred
1	Watch interrupt occurred

1 is read when the Read Modify Write instruction is read. If the WIF bit is set to 1 when the WIE bit is 1, an interrupt request is output. This bit is cleared upon reset.

[Bit 6] WIE: Watch interrupt enable bit

This bit is used to enable an interrupt by the watch.

0	Interrupt by watch disabled
1	Interrupt by watch enabled

[Bit 2] WS1: Interrupt interval time specification bit by watch

[Bit 1] WS0: Interrupt interval time specification bit by watch

These bits are used to specify the interrupt cycles.

WS1	WS0	Interrupt cycle	
0	0	31.25 [ms]	2^{10}/fcl
0	1	0.25 [s]	2^{13}/fcl
1	0	0.50 [s]	2^{14}/fcl
1	1	1.00 [s]	2^{15}/fcl

/fcl: Subclock oscillation frequency

[Bit 0] WCLR: Bit clearing watch prescaler

This bit is used to clear the watch prescaler.

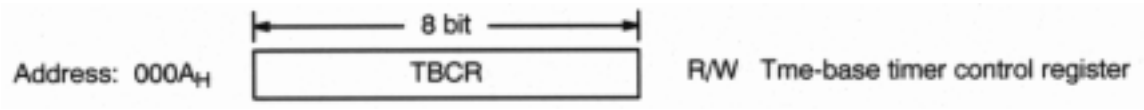
0	Watch prescaler cleared
1	No operation

1 is always read when this bit is read.

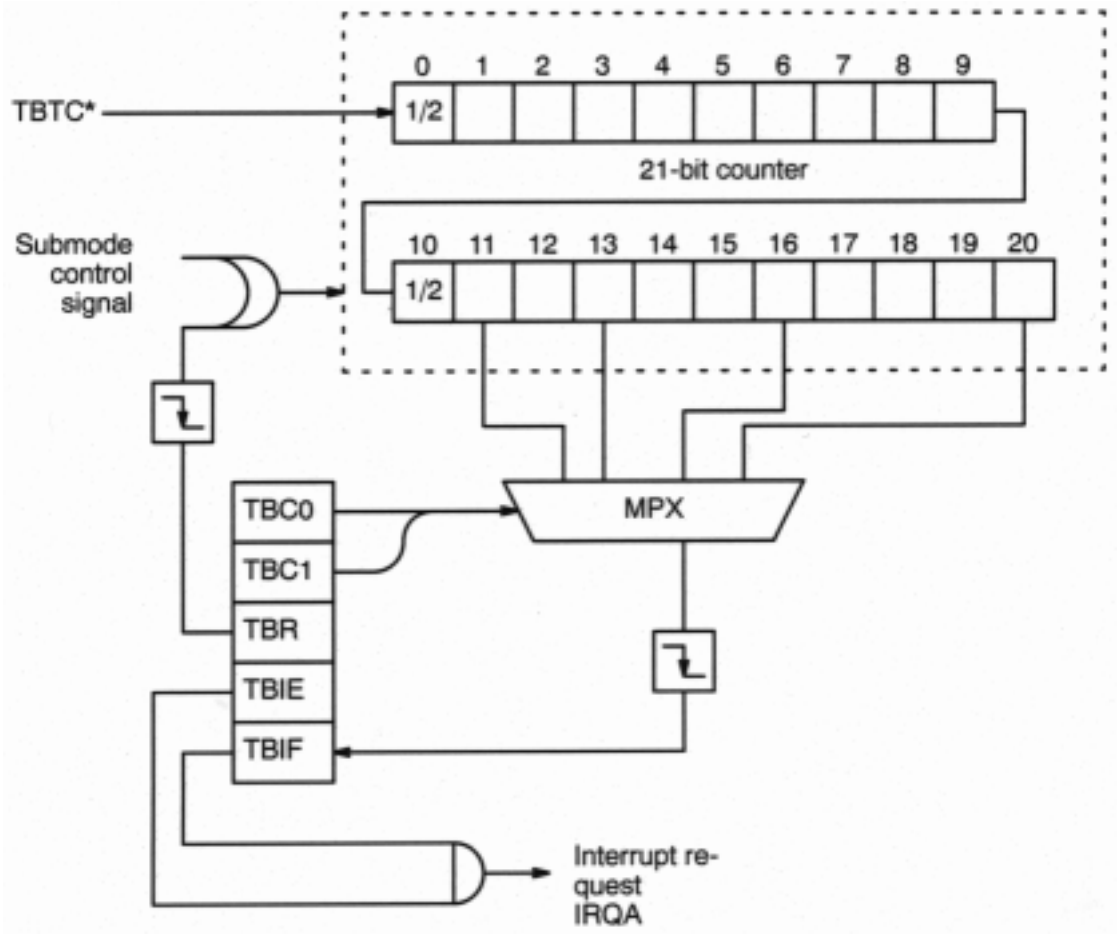
2.2.11 Time-base Timer

- This timer has a 21-bit binary counter and uses a clock pulse with 1/2 oscillation of the main clock.
- Four interval times can be selected.
- This function cannot be used when the main clock is stopped.

(1) Registers



(2) Block diagram



* TBTC is a clock pulse with 1/2 oscillation of the main clock.

(3) Description of registers

(a) Time-base timer control register (TBCR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $000A_H$	TBOF	TBIE	—	—	—	TBC1	TBC0	TBR	$00XX\ X000_B$
	(R/W)	(R/W)				(R/W)	(R/W)	(W)	

[Bit 7] TBOF: Interval timer overflow bit

When writing, this bit is used to clear the interval timer overflow flag.

0	Interval timer overflow flag cleared
1	No operation

When reading, this bit indicates that an interval timer overflow has occurred.

0	Interval timer overflow not occurred
1	Interval timer overflow occurred

1 is read when the Read Modify Write instruction is read. If the TBIF bit is set to 1 when the TBIE bit is 1, an interrupt request is output. This bit is cleared upon reset.

[Bit 6] TBIE: Interval-timer interrupt enable bit

This bit is used to enable an interrupt by the interval timer.

0	Interval interrupt disabled
1	Interval interrupt enabled

[Bit 2] TBC1: Interval time specification bit

[Bit 1] TBC2: Interval time specification bit

Bits 1 and 2 are used to specify interval timer cycle.

TBC1	TBC0	Interval time	At 10 MHz oscillation
0	0	2^{13}/fch	0.81 [ms]
0	1	2^{15}/fch	3.27 [ms]
1	0	2^{18}/fch	26.21 [ms]
1	1	2^{22}/fch	0.419 [s]

/fch: main clock frequency

[Bit 0] TBR: Time-base timer clear bit

This bit is used to clear time-base timer.

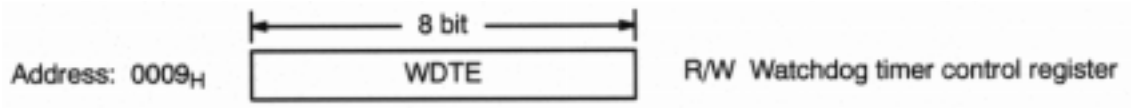
0	Time-base timer cleared
1	No operation

1 is always read when this bit is read.

2.2.12 Watchdog Timer Reset

Either of a signal output from the time-base timer for counting with the main clock or a signal output from the watch prescaler for counting with the subclock can be selected as a clock.

(1) Registers



(2) Block diagram

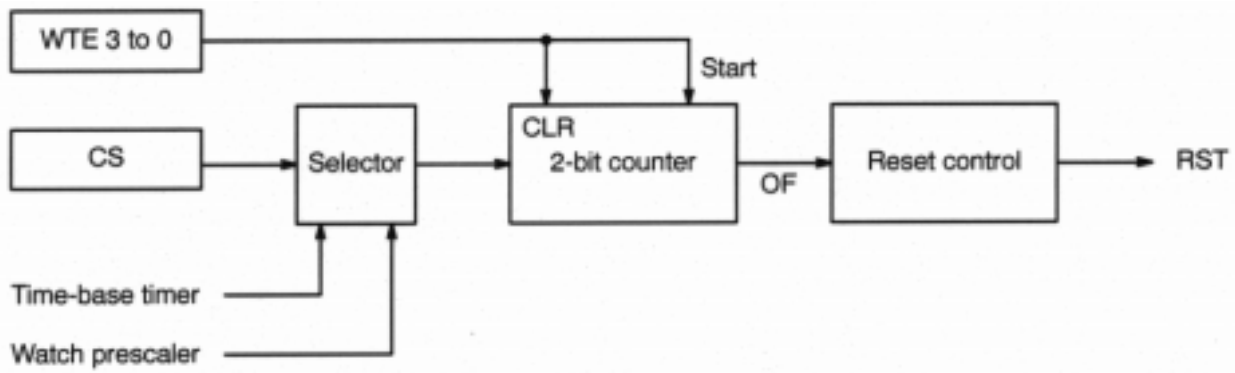
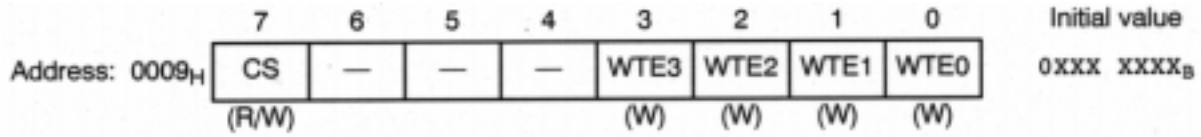


Fig. 2.14 Block Diagram of Watchdog Timer

(3) Description of register

Watchdog timer control register (WDTE)



[Bit 7] CS: Clock source switching bit

Bit 7 is used to select a count clock from either the watch prescaler or time-base timer.

0	Time-base timer Period $1/2^{22}$ fch
1	Watch prescaler Period $1/2^{14}$ fcl

fch: Main clock frequency
fcl: Subclock frequency

Set this bit as soon as the watchdog timer is started. Do not change the bit after the timer is started. When using the submode, always select the watch prescaler.

[Bits 3 to 0] WTE3 to WTE0: Watchdog timer control bit

Bits 3 to 0 control the watchdog timer.

First write only after reset

0101	Watchdog timer started
Other than the above	No operation

Second and later write

0101	Watchdog timer counter cleared.
Other than the above	No operation

The watchdog timer can be stopped only by reset. 1111 is read when these bit are read.

(4) Description of operation

The watchdog timer enables detection of a program nullfunction.

- Starting watchdog timer

  The watchdog timer starts when 0101 is written at the watchdog timer control bits.

- Clearing watchdog timer

  When 0101 is written at the watchdog timer control bits after start, the watchdog timer is cleared. The counter of the watchdog timer is cleared when changing to the standby mode (STOP, SLEEP, CLOCK) or hold mode.

- Watchdog timer reset

  If the watchdog timer is not cleared within the time given in the table below, a watchdog timer reset occurs to reset the chip internally.

	Clock source		
	Time-base timer	Watch prescaler	
Minimum time	Approx. 419.4 ms	Approx. 512 ms	at high-speed 10 MHz clock
Maximum time	Approx. 838.8 ms	Approx. 1024 ms	at low-speed 32 kHz clock

- Stopping watchdog timer

  Once started, the watchdog timer will not stop until a reset occurs.

3. OPERATION

3.1 CLOCK PULSE GENERATOR 3-3
3.2 RESET 3-4
3.3 INTERRUPT 3-6
3.4 MEMORY ACCESS MODE 3-8
3.5 READY AND HOLD FUNCTIONS 3-10
3.6 LOW-POWER CONSUMPTION MODES 3-12
3.7 PIN STATES FOR SLEEP, STOP, HOLD, AND RESET 3-13

3.1 CLOCK PULSE GENERATOR

The MB89630 series of microcontrollers incorporate the system clock pulse generator. The crystal oscillator is connected to the X0 and X1 pins to generate clock pulses. Clock pulses can also be supplied internally by inputting externally-generated clock pulses to the X0 pin. The X1 pin should be kept open.

The X0A and A1A pins are for subclock inputs. They function like the X0 and X1 pins.

When the single-channel option is selected, the X0A and X1A pins serve as P71/INT1 and P70/INT2, respec tively.

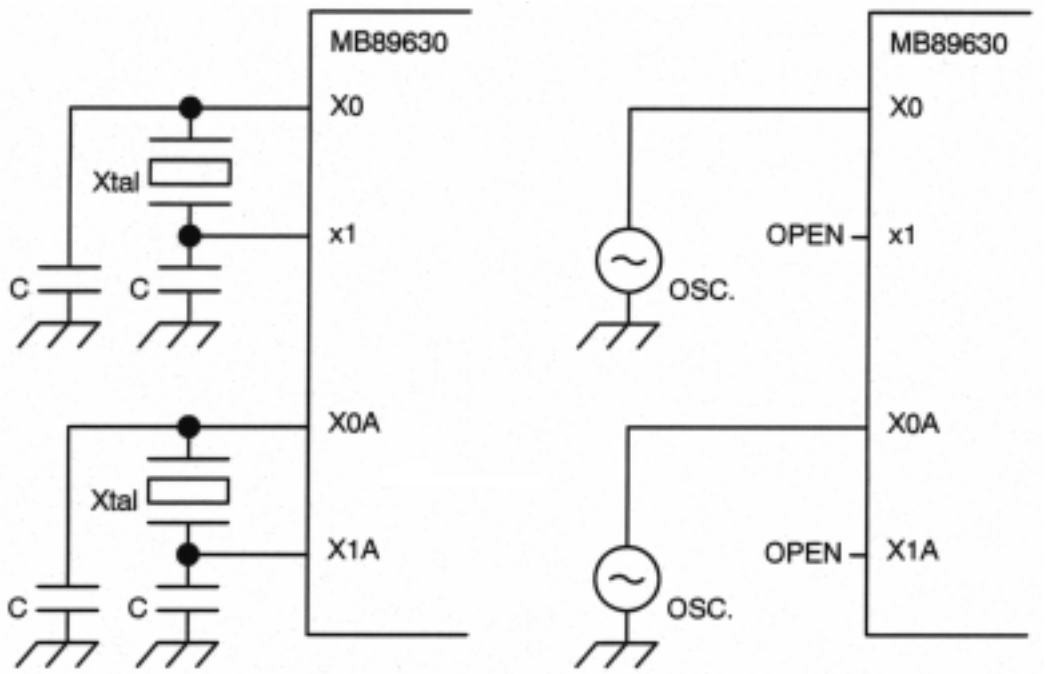


Fig. 3.15 Clock Pulse Generator

3.2 RESET

3.2.1 Reset Operation

When reset conditions occur, the MB89630 series of microcontrollers suspend the currently-executing in struction to enter the reset state. The contents written at the RAM do not change before and after reset. How ever, if a reset occurs during writing of 16-bit long data, data is written to the upper bytes and may not be written to lower bytes. If a reset occurs around write timing, the contents of the addresses being written are not as sured.

When the reset conditions are cleared, the MB89630 series of microcontrollers are released from the reset state and start operation after fetching the mode data from address **$FFFD_H$**, the upper bytes of the reset vec tors from address **$FFFE_H$**, and the lower bytes from address **$FFFF_H$**, in that order. Figure 3.2 shows the flow chart for the reset operation.

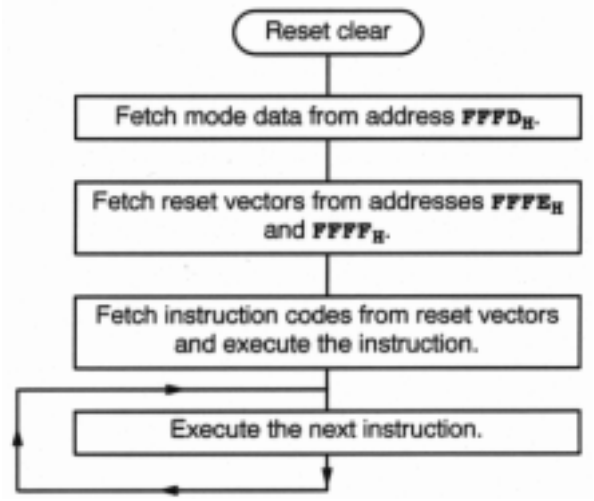


Fig. 3.16 Outline of Reset Operation

Table 3-1 indicates the structure of data to be stored in addresses **$FFFD_H$**, **$FFFE_H$**, and **$FFFF_H$**.

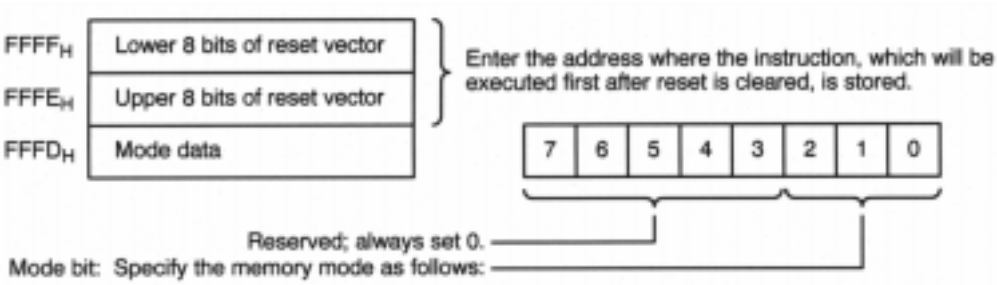


Table 3.12 Reset Vector Structure

T2	T1	T0	Operation
0	0	0	External-access disable (single chip)
0	0	1	External-access enable (external-bus enable)
Other than above			Reserved; do not set.

3.2.2 Reset Sources

The MB89630 series of microcontrollers have the following reset sources.

(1) External pin
A Low level is input to the $\overline{RST}$ pin.

(2) Specification by software
0 is written at the RST bit of the standby-control register.

(3) Power-on
The power is turned on when the power-on reset option is selected.

(4) Watchdog function
The watchdog function is enabled by the watchdog-control register and reaccess to this register is not obtained within the specified time.

When the stop mode is cleared by reset or power-on reset (option selected), operation is started after elapse of the oscillation stabilization time.

See the state transition diagram and (d) Reset in 2.1.5 for details of the reset operation.

3.3 INTERRUPT

If the interrupt controller and CPU are ready to accept interrupts when an interrupt request is output from the resources or by an external-interrupt input, the CPU temporarily suspends the currently-executing instruction and executes the interrupt-processing program. Figure 3.3 shows the interrupt-processing flow-chart.

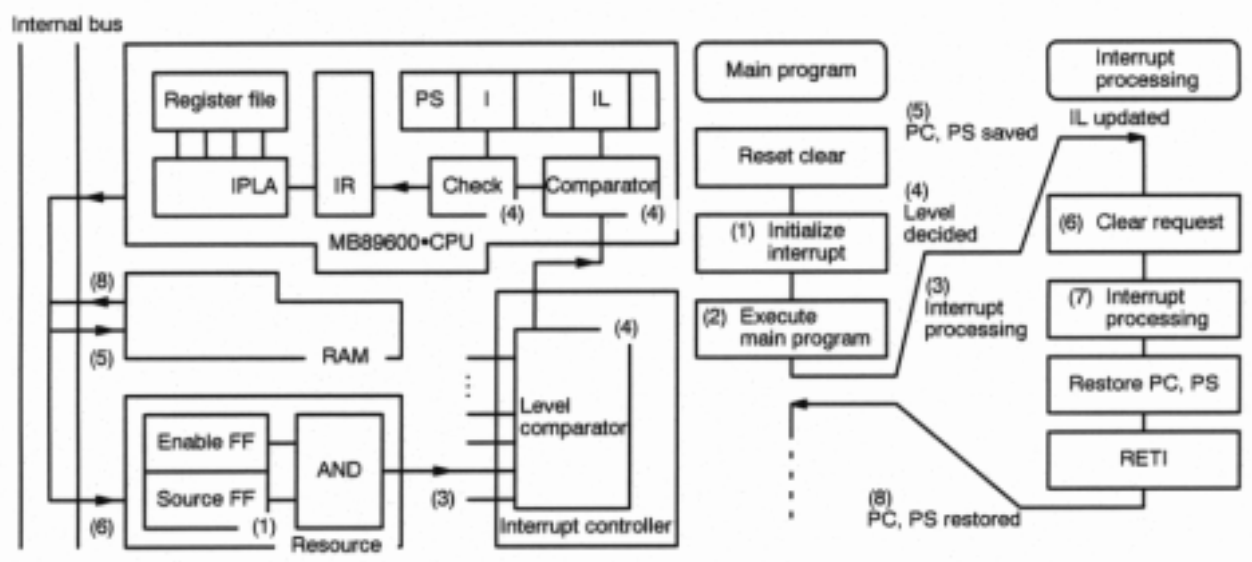


Fig. 3.17 Interrupt-processing Flowchart

All interrupts are disabled after a reset is cleared. Therefore, initialize interrupts in the main program (1). Each resource generating interrupts and the interrupt-level-setting registers (ILR1 - ILR3) in the interrupt controller corresponding to these interrupts are to be initialized. The levels of all interrupts can be set by the interrupt-level-setting registers (ILR1 - ILR3) in the interrupt controller. The interrupt level can be set from 1 to 3, where 1 indicates the highest level, and 2 the second highest level. Level 3 indicates that no interrupt occurs. The interrupt request of this level can be accepted. After initializing the resource registers, the main program exe cutes various controls (2). Interrupts are generated from the resources (3). The highest-priority interrupt re quests are identified from those occurring at the same time by the interrupt controller and are transferred to the CPU. The CPU then checks the current interrupt level and the status of the I-flag (4), and starts the interrupt processing.

The CPU performs the interrupt processing to save the contents of the current PC and PS in the stack (5) and fetches the entry addresses of the interrupt program from the interrupt vectors. After updating the IL value in the PS to the required one, the CPU starts executing the interrupt-processing routine.

Clear the interrupt sources (6) and process the interrupts in the user's interrupt-processing routine. Finally, restore the PC and PS values saved by the RETI instruction in the stack (8) to return to the interrupted instruc tion.

Note: Unlike the F^2MC-8, A and T are not saved in the stack at the interrupt time.

Table 3-2 lists the relationships between each interrupt source and interrupt vector.

Table 3.13 Interrupt Sources and Interrupt Vectors

Interrupt source	Upper vector address	Lower vector address
IRQ0 (External interrupt 1#1)	$FFFA_H$	$FFFB_H$
IRQ1 (External interrupt 1#2)	$FFF8_H$	$FFF9_H$
IRQ2 (8-bit serial I/O)	$FFF6_H$	$FFF7_H$
IRQ3 (8-bit PWM timer #2)	$FFF4_H$	$FFF5_H$
IRQ4 (8-bit PWM timer #2)	$FFF2_H$	$FFF3_H$
IRQ5 (Pulse-width count timer)	$FFF0_H$	$FFF1_H$
IRQ6 (URAT receiver interrupt)	$FFEE_H$	$FFEF_H$
IRQ7 (URAT transmitter interrupt)	$FFEC_H$	$FFED_H$
IRQ8 (8-bit serial I/O#2)	$FFEA_H$	$FFEB_H$
IRQ9 (A/D converter)	$FFE8_H$	$FFE9_H$
IRQA (Interval timer)	$FFE6_H$	$FFE7_H$
IRQB (Watch)	$FFE4_H$	$FFE5_H$

3.4 MEMORY ACCESS MODE

When external access is enabled by setting bits 2 to 0 of the mode data at address **$FFFD_H$**, the ☐ areas in Figure 3.4 are externally accessed via the P0 to P2 pins.

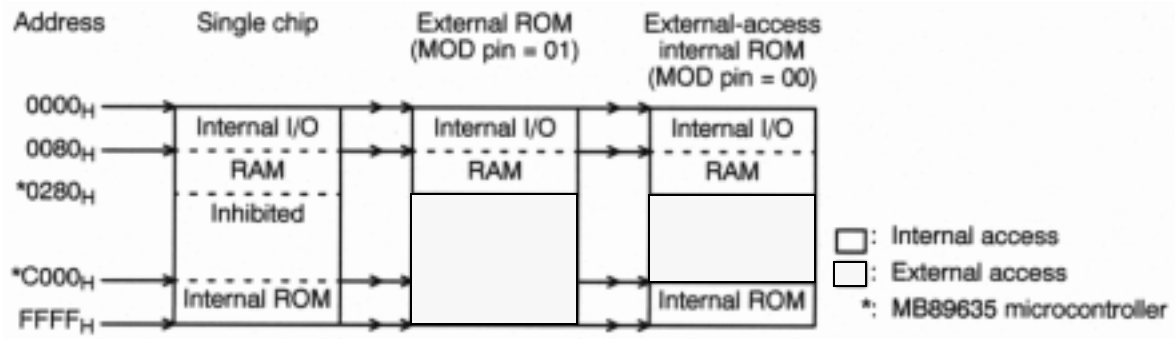


Fig. 3.18 Memory Map in Various Modes

As shown in Figure 3.5, when accessing by the external pins, specify the address of the external peripheral/ memory to be accessed according to the access information to be output to the address and address-data pins. The lower 8 bits of the address are input and output by time-sharing with the data bus. Therefore, the external circuit should be created so that the address information can be latched at the falling edge of the ALE signal to be output to the ALE pin. For access, when reading, input data from the external peripheral/ memory to the data pin in synchronization with the read strobes to be output to the $\overline{RD}$ pin; when writing, write the data to be output to the data pin to the external peripheral/memory in synchronization with the write strobes to be output to the $\overline{WR}$ pin.

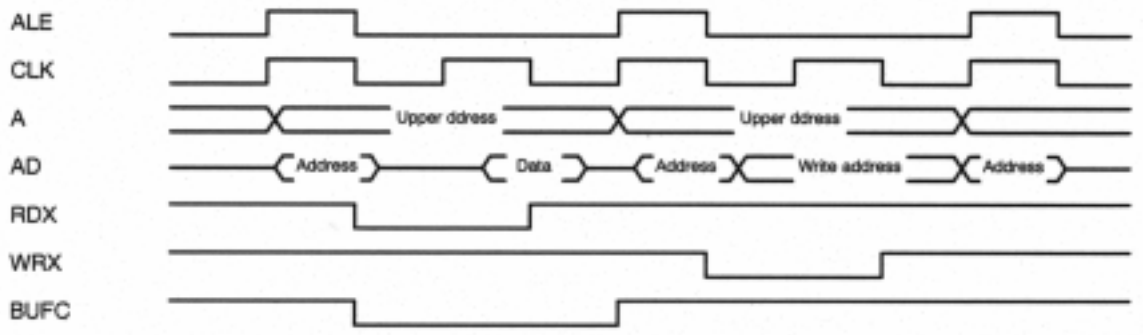


Fig. 3.19 External-access Timing Chart

The BUFC signal is used when the address-data bus has an external buffer. It controls the buffer direction. This signal can be used to facilitate buffer control.

Figure 3.6 shows an example of connecting the external peripheral/memory to the MB89630 series of micro controllers. In this circuit, the external bus is used after enabling the operation of the $\overline{\text{HAK}}$ pin by the external ROM. When using the hold function, the pull-up resistor must be attached externally to the $\overline{\text{HAK}}$ pin.

At access to internal ROM, A15 to A08, AD7 to AD0, and ALE are output but $\overline{\text{WR}}$ and $\overline{\text{RD}}$ are not output.

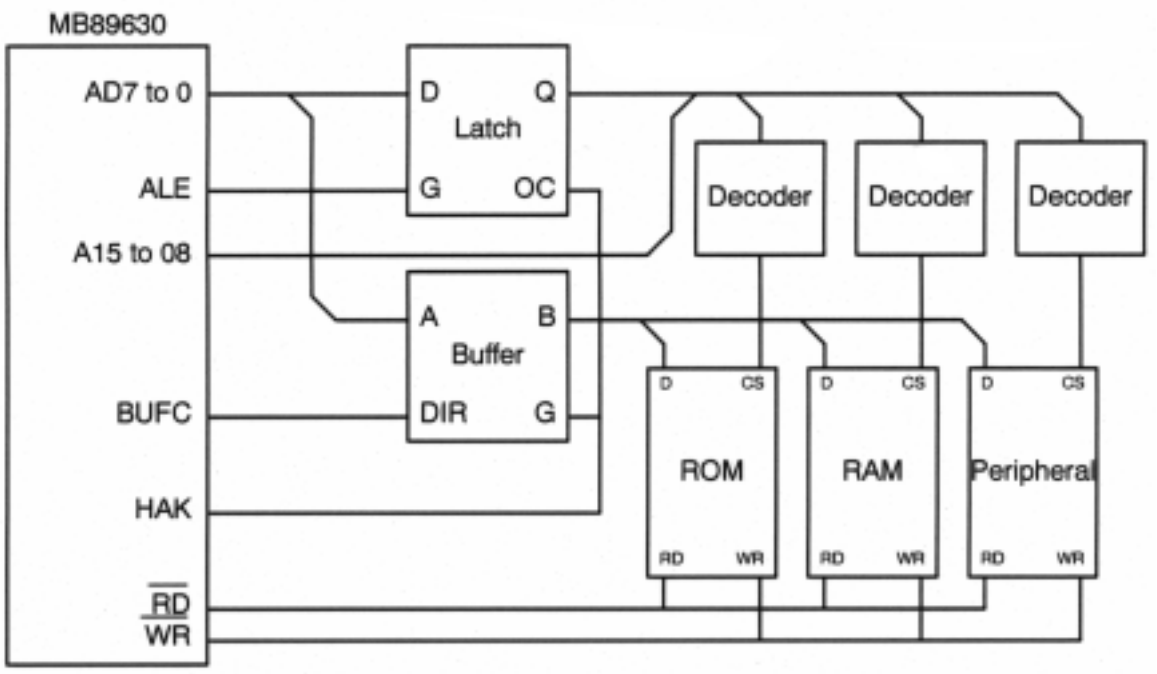
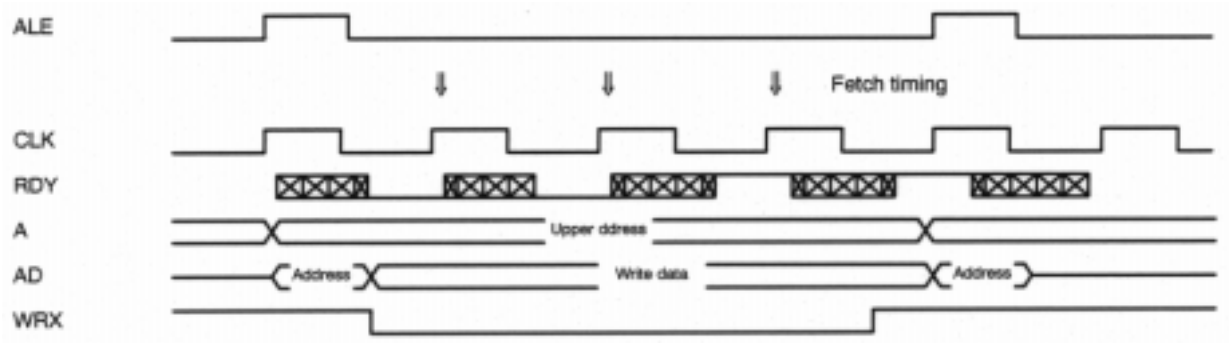


Fig. 3.20 External Peripheral/Memory Connection

3.5 READY AND HOLD FUNCTIONS

3.5.1 Ready Function

The RDY pin allows access to the low-speed memory and resources. When the RDY pin goes Low while the CPU is conducting external access, the CPU prolongs the last bus cycle by double oscillations. When the CPU conducts an internal access, the value of the RDY pin is ignored. As shown in Figure 3.7, the Ready signal is input near the center of the $\overline{RD}$ or $\overline{WR}$ pin. In the not-ready state, the Ready signal is input around the CLK rising edge. The Ready/Not-ready signal can be generated in the circuit as shown in Figure 3.8.



Note: The read cycle is also prolonged in the same manner.

Fig. 3.21 Ready Input Timing Chart (Write Cycle)

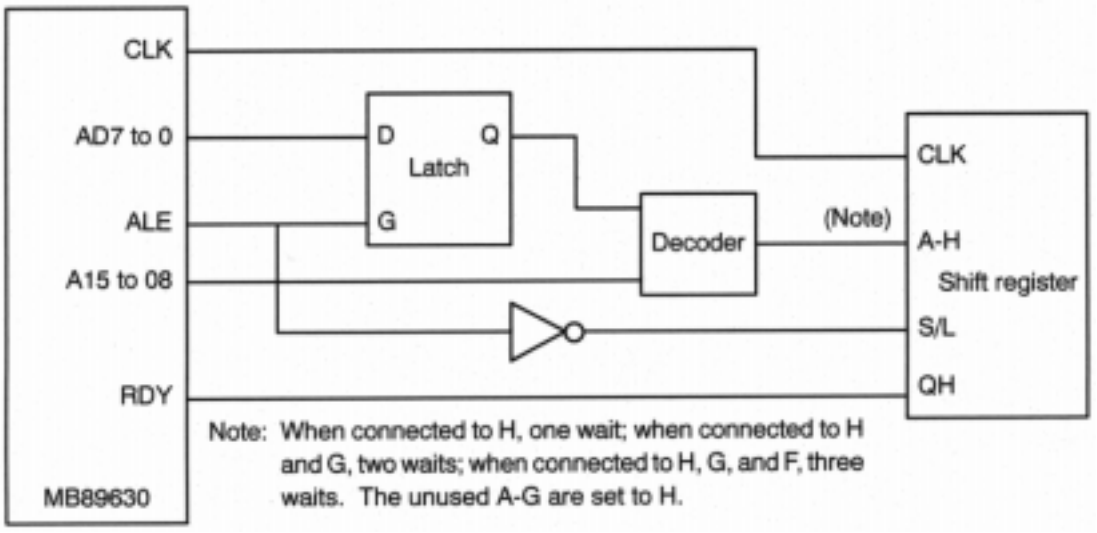


Fig. 3.22 Ready Generation Circuit

3.5.2 Hold Function

The CPU samples the user hold-request input to the HRQ pin at the boundary of each instruction and sets the HAK pin to Low to open the bus. When the CPU detects that the HRQ pin is active, it temporarily suspends operation to set the address, data, RD, WR, and BUFC pins to High impedance, and also enters the hold state after outputting a Low level from the HAK pin. Figure 3.9 shows the hold timing.

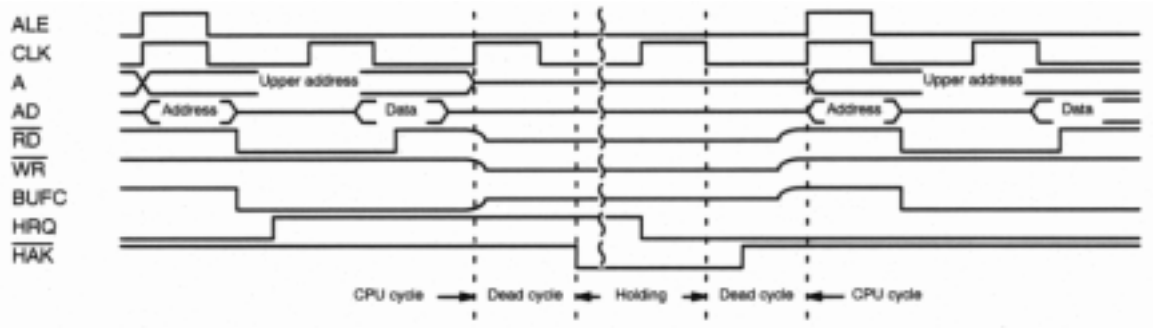


Fig. 3.23 Hold Timing

The CPU does not accept any hold requests in the stop and sleep modes. The use of the hold-acknowledge signal with an external buffer is shown in Figure 3.6.

In the hold mode, the CPU is stopped but each resource is operable. No watchdog reset occurs during the hold mode because the watchdog timer counter is cleared.

3.6 LOW-POWER CONSUMPTION MODES

The MB89630 series of microcontrollers have three standby modes: sleep, stop, and watch to reduce the power consumption. Writing to the standby-control register (STBC) gives these three standby modes. Clear ing is performed by an interrupt or at reset. See 2.1.5 for setting and releasing each mode.

The MB89630 series of microcontrollers have a dual-clock module, and the low-power consumption modes vary with the main clock and subclock modes. In addition, whether or not an oscillation stabilization period is required at release from the low-power consumption mode depends on the mask option of the power-on reset. (See the state transition diagram in 2.1.5.)

If the single-clock module is specified with the mask option, the MB89630 series of microcontrollers can be used as single clocks. If the microcontrollers are used as single clocks without specifying the single-clock module with the mask option, once the subclock mode is entered, it cannot be released. Therefore, when using these controllers as a single clock, specify the single-clock module with the mask option.

Table 3.14 Low-power Consumption Mode at Each Clock Mode

Function		Note	Main Mode			Sub Mode			
			RUN	SLEEP	STOP	RUN	SLEEP	STOP	WATCH
Main clock		—	Operate	Operate	Stop	Stop	Stop	Stop	Stop
Subclock		—	Operate	Operate	Operate	Operate	Operate	Stop	Operate
CPU	Instruction	—	Operate	Stop	Stop	Operate	Stop	Stop	Stop
	ROM	—	Operate	Hold	Hold	Operate	Hold	Hold	Hold
	RAM	—							
Resource	I/O	○	Operate	Hold	Hold	Operate	Hold	Hold	Hold
	Watch prescaler	×	Operate	Operate	Operate*	Operate	Operate	Stop	Operate
	Time-base timer	×	Operate	Operate	Stop	Stop	Stop	Stop	Stop
	8-bit PWM	○	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	8-bit PWC	○	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	16-bit timer	○	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	8-bit timer	○	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	8-bit SIO	○	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	UART	○	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	A/DC	○	Operate	Operate	Stop	Operate**	Operate**	Stop	Stop
	External interrupt	○	Operate	Operate	Operate	Operate	Operate	Operate	Operate
	Buzzer output	×	Operate	Operate	Stop	Stop	Stop	Stop	Stop
	Watchdog timer	×	Operate	Stop	Stop	Operate***	Stop	Stop	Stop

Notes:

○ : Clock mode (for main mode or submode) where operation speed affected by gear function.
X : Clock mode (for main mode or submode) where operation speed not affected by gear function.
* : The watch prescaler can operate counting but the watch interrupt cannot be operated.
** : These functions can be operated but do not use them.
** : When clock source used as watch prescaler.

3.7 PIN STATES FOR SLEEP, STOP, HOLD, AND RESET

The state of each pin of the MB89630 series of microcontrollers at sleep, stop, hold, and reset is as follows:

(1) Sleep

The pin state immediately before the sleep state is held.

(2) Stop

The pin state immediately before the stop state is held when the stop mode is started and bit 5 of the stand by-control register (STBC) is set to 0; the impedance of the output and input/output pins goes High when the bit is set to 1.

(3) Hold

The impedance of the bus pins goes High.

(4) Reset

When the MOD pin is 00, the impedance of all I/O and resource pins (excluding pins for pull-up option) goes High. When the MOD pin is 01, the ALE, CLK, RDY, and BUFC signals become active.

The detailed pin state in each mode is described on the following pages.

Normal Pins for MB89630 Series of Microcontrollers (in Single-Chip Mode)

Pin name		Normal	Sleep	Stop (Sub) SPL = 0	Stop (Sub) SPL = 1	Reset
P00/AD0 to P07/AD7		Port input/output	Port input/output	Port input/output	High impedance (Note 1)	High impedance
P10/A08 to P17/A15		Port input/output	Port input/output	Port input/output	High impedance (Note 1)	High impedance
X0		Input for oscillation	Input for oscillation	High impedance (Note 1)	High impedance (Note 1)	Input for oscillation
P71	X0A (Note 3)	Input for oscillation	Input for oscillation	High impedance	High impedance	Input for oscillation
	INT1 (Note 2)	Port/resource input	Port/resource input	Port/resource input	Resource input	High impedance
X1		Output for oscillation	Output for oscillation	H output	H output	Output for oscillation
P70	X1A (Note 3)	Output for oscillation	Output for oscillation	H output	H output	Output for oscillation
	INT0 (Note 2)	Port/resource input	Port/resource input	Port/resource input	Resource input	High impedance
MOD0 MOD1		Mode input	Mode input	Mode input	Mode input	Mode input
$\overline{RST}$		Reset input	Reset input	Reset input	Reset input	Reset input (Note 4)
P27/ALE		Port output	Port output	Port output	High impedance	High impedance
P26/$\overline{RD}$		Port output	Port output	Port output	High impedance	High impedance
P25/$\overline{WR}$		Port output	Port output	Port output	High impedance	High impedance
P24/CLK		Port output	Port output	Port output	High impedance	High impedance
P23/RDY		Port output	Port output	Port output	High impedance	High impedance
P22/HRQ		Port output	Port output	Port output	High impedance	High impedance
P21/$\overline{HAK}$		Port output	Port output	Port output	High impedance	High impedance
P20/BUFC		Port output	Port output	Port output	High impedance	High impedance
P30/UCK1 to P37/WTO		Port/resource input/ output	Port/resource input/ output	Port/resource output (Note 5)	High impedance (Note 1)	High impedance
P40/UCK2 to P43/PTO1		Port/resource input/ output	Port/resource input/ output	Port/resource output (Note 5)	High impedance (Note 1)	High impedance
P50/ADST to P53/PTO2		Port/resource input/ output	Port/resource input/ output	Port/resource output (Note 5)	High impedance (Note 1)	High impedance
P60/AN0 to P67/AN7		Port/resource input	Port/resource input	Port/resource output (Note 5)	High impedance (Note 1)	High impedance
P72/INT2 to P74/EC		Port/resource input	Port/resource input	Port/resource input	Resource input	High impedance

Notes:

1 : The input level is fixed to prevent leakage due to open input.

2 : When single clock is operated.

3 : When double clocks are operated.

4 : The reset pin may serve as and output depending on the option setting.

5 : When these pins are used for port or resource inputs, the input level is fixed to prevent leakage due to open input.

Normal Pins for MB89630 Series of Microcontrollers (in External-ROM and External-Access Internal-ROM Modes)

Pin name		Normal	Hold	Sleep	Stop (Sub) SPL = 0	Stop (Sub) SPL = 1	Reset (MOD = 00)	Reset (MOD = 01)
P00/AD0 to P07/AD7		Address/data input/output	High impedance	Data output	Data output	High impedance (Note 1)	High impedance	Undefined
P10/A08 to P17/A15		Address output	High impedance	Address output	Address output	High impedance (Note 1)	High impedance	Undefined
X0		Input for oscillation	Input for oscillation	Input for oscillation	High impedance (Note 1)	High impedance (Note 1)	Input for oscillation	Input for oscillation
P71/	X0A (Note 3)	Input for oscillation	Input for oscillation	Input for oscillation	High impedance (Note 1)	High impedance (Note 1)	Input for oscillation	Input for oscillation
	INT1 (Note 2)	Port/resource input	Port/resource input	Port/resource input	Port/resource input	Port/resource input	High impedance	High impedance
X1		Output for oscillation	Output for oscillation	Output for oscillation	H output	H output	Output for oscillation	Output for oscillation
P70/	X1A (Note 3)	Output for oscillation	Output for oscillation	Output for oscillation	H output	H output	Output for oscillation	Output for oscillation
	INT0 (Note 2)	Port/resource input	Port/resource input	Port/resource input	Port/resource input	Port/resouce input	High impedance	High impedance
MOD0 MOD1		Mode input	Mode input	Mode input	Mode input	Mode input	Mode input	Mode input
$\overline{RST}$		Reset input	Reset input	Reset input	Reset input	Reset input	Reset input (Note 2)	Reset input (Note 4)
P27/ALE		ALE output	L output	L output	L output	High impedance	High impedance	L output
P26/$\overline{RD}$		RD output	High impedance	H output	H output	High impedance	High impedance	H output
P25/$\overline{WR}$		WR output	High impedance	H output	H output	High impedance	High impedance	H output
P24/CLK		CLK output	CLK output	CLK output	H output	High impedance	High impedance	CLK output
P23/RDY		RDY input	High impedance	High impedance	High impedance (Note 1)	High impedance	High impedance	RDY input
P22/$\overline{HRQ}$		HRQ input (Note 5)	HRQ input (Note 5)	High impedance (Note 5)	High impedance (Notes 1 and 5)	High impedance (Note 1)	High impedance	Port output (Low level)
P21/HAK		HAK output (Note 4)	L output	H output (Note 5)	H output (Note 5)	High impedance	High impedance	Port output (Low level)
P20/BUFC		BUFC output	High impedance (Note 5)	H output (Note 5)	H output (Note 5)	High impedance	High impedance	H output
P30/UCK1 to P37/WTO		Port/resource input/output	Port/resource input/output	Port/resource input/output	Port/resource output (Note 6)	High impedance (Note 1)	High impedance	High impedance
P40/UCK2 to P43/PTO1		Port/resource input/output	Port/resource input/output	Port/resource input/output	Port/resource output (Note 6)	High impedance (Note 1)	High impedance	High impedance
P50/ADST to P53/PTO2		Port/resource input/output	Port/resource input/output	Port/resource input/output	Port/resource output (Note 6)	High impedance (Note 1)	High impedance	High impedance
P60/AN0 to P67/AN7		Port/resource input/output	Port/resource input/output	Port/resource input/output	Port/resource output (Note 6)	High impedance (Note 1)	High impedance	High impedance
P72/INT2 to P74/EC		Port/resource input	Port/resource input	Port/resource input	Port/resource input	Port/resource input	High impedance	High impedance

Notes:

1 : The input level is fixed to prevent leakage due to open input.

2 : Single clock

3 : Double clocks

4 : The reset pin may serve as an output depending on the option setting.

5 : This may operate as a port depending on the setting of the bus-control register (BCTR).

6 : When these pins are used for port or resource inputs, the input level is fixed to prevent leakage due to open input.

4. COMMAND

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4.1 TRANSFER INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
2	MOV @IX+off,A	4	2	((IX)+off) ← (A)	–	–	–	– – – –	46
3	MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
4	MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
5	MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
6	MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
7	MOV A,dir	3	2	(A) ← dir	AL	–	–	+ + – –	05
8	MOV A,@IX+off	4	2	(A) ← ((IX)+off)	AL	–	–	+ + – –	06
9	MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
10	MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
11	MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
12	MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
13	MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
14	MOV @IX+off,#d8	5	3	((IX)+off)← d8	–	–	–	– – – –	86
15	MOV @EP,#d8	4	2	((EP))← d8	–	–	–	– – – –	87
16	MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
17	MOVW dir,A	4	2	(dir) ←(AH),(dir+1)← (AL)	–	–	–	– – – –	D5
18	MOVW @IX+off,A	5	2	((IX)+off)←(AH),((IX)+off+1)←(AL)	–	–	–	– – – –	D6
19	MOVW ext,A	5	3	(ext) ← (AH),(ext+1)←(AL)	–	–	–	– – – –	D4
20	MOVW @EP,A	4	1	((EP)) ← (AH),((EP)+1)← (AL)	–	–	–	– – – –	D7
21	MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
22	MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
23	MOVW A,dir	4	2	(AH)←(dir),(AL)←(dir+1)	AL	AH	dH	+ + – –	C5
24	MOVW A,@IX+off	5	2	(AH)←((IX)+off),(AL)←((IX)+off+1)	AL	AH	dH	+ + – –	C6
25	MOVW A,ext	5	3	(AH)←(ext),(AL)←(ext+1)	AL	AH	dH	+ + – –	C4
26	MOVW A,@A	4	1	(AH)←((A)),(AL)← ((A)+1)	AL	AH	dH	+ + – –	93
27	MOVW A,@EP	4	1	(AH)←((EP)),(AL) ←((EP)+1)	AL	AH	dH	+ + – –	C7
28	MOVW A,EP	2	1	(A) ←(EP)	–	–	dH	– – – –	F3
29	MOVW EP,#d16	3	3	(EP)←d16	–	–	–	– – – –	E7
30	MOVW IX,A	2	1	(IX)←(A)	–	–	–	– – – –	E2
31	MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
32	MOVW SP,A	2	1	(SP)← (A)	–	–	–	– – – –	E1
33	MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
34	MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
35	MOVW @A,T	4	1	((A)) ← (TH),((A)+1) ← (TL)	–	–	–	– – – –	83
36	MOVW IX,#d16	3	3	(IX)← d16	–	–	–	– – – –	E6
37	MOVW A,SP	2	1	(A) ← (PS)	–	–	dH	– – – –	70
38	MOVW PS,A	2	1	(PS)← (A)	–	–	–	+ + + +	71
39	MOVW SP,#d16	3	3	(SP)← d16	–	–	–	– – – –	E5
40	SWAP	2	1	(AH) ⇔ (AL)	–	–	AL	– – – –	10
41	SETB dir:n	4	2	(dir):n ← 1	–	–	–	– – – –	A8 to AF
42	CLRB dir:n	4	2	(dir):n ← 0	–	–	–	– – – –	A0 to A7
43	XCH A,T	2	1	(AL) ⇔ (TL)	AL	–	–	– – – –	42
44	XCHW A,T	3	1	(A) ⇔ (T)	AL	AH	dH	– – – –	43
45	XCHW A,EP	3	1	(A) ⇔ (EP)	–	–	dH	– – – –	F7
46	XCHW A,IX	3	1	(A) ⇔ (IX)	–	–	dH	– – – –	F6
47	XCHW A,SP	3	1	(A) ⇔ (SP)	–	–	dH	– – – –	F5
48	MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Note:

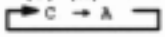
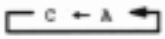
1 : In byte transfer to A, T ← A is only for low bytes.

2 : Operands for two or more operand instructions should be stored in the order designated in MNEMONIC (Opposite order to F^2MC-8 family).

~ : Cycles

: Byte counts

4.2 OPERATION INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	ADDC A,Ri	3	1	(A) ← (A)+(Ri)+C	–	–	–	+ + + +	28 to 2F
2	ADDC A,#d8	2	2	(A) ← (A)+d8+C	–	–	–	+ + + +	24
3	ADDC A,dir	3	2	(A) ← (A)+(dir)+C	–	–	–	+ + + +	25
4	ADDC A,@IX+off	4	2	(A) ← (A)+((IX)+off)+C	–	–	–	+ + + +	26
5	ADDC A,@EP	3	1	(A) ← (A)+((EP))+C	–	–	–	+ + + +	27
6	ADDCW A	3	1	(A) ← (A)+(T)+C	–	–	dH	+ + + +	23
7	ADDC A	2	1	(AL)← (AL)+(TL)+C	–	–	–	+ + + +	22
8	SUBC A,Ri	3	1	(A) ← (A)-(Ri)-C	–	–	–	+ + + +	38 to 3F
9	SUBC A,#d8	2	2	(A) ← (A)-d8-C	–	–	–	+ + + +	34
10	SUBC A,dir	3	2	(A) ← (A)-(dir)-C	–	–	–	+ + + +	35
11	SUBC A,@IX+off	4	2	(A) ← (A)-((IX)+off)-C	–	–	–	+ + + +	36
12	SUBC A,@EP	3	1	(A) ← (A)-((EP))+C	–	–	–	+ + + +	37
13	SUBCW A	3	1	(A) ← (T)-(A)-C	–	–	dH	+ + + +	33
14	SUBC A	2	1	(AL)← (TL)-(AL)-C	–	–	–	+ + + +	32
15	INC Ri	4	1	(Ri)← (Ri)+1	–	–	–	+ + + –	C8 to CF
16	INCW EP	3	1	(EP)← (EP)+1	–	–	–	– – – –	C3
17	INCW IX	3	1	(IX)← (IX)+1	–	–	–	– – – –	C2
18	INCW A	3	1	(A) ← (A)+1	–	–	dH	+ + – –	C0
19	DEC Ri	4	1	(Ri)← (Ri)-1	–	–	–	+ + + –	D8 to DF
20	DECW EP	3	1	(EP)← (EP)-1	–	–	–	– – – –	D3
21	DECW IX	3	1	(IX)← (IX)-1	–	–	–	– – – –	D2
22	DECW A	3	1	(A) ← (A)-1	–	–	dH	+ + – –	D0
23	MULU A	19	1	(A) ← (AL)*(TL)	–	–	dH	– – – –	01
24	DIVU A	21	1	(A) ← (T)/(AL), MOD→(T)	dL	00	00	– – – –	11
25	ANDW A	3	1	(A) ← (A) ^ (T)	–	–	dH	+ + R –	63
26	ORW A	3	1	(A) ← (A)∨(T)	–	–	dH	+ + R –	73
27	XORW A	3	1	(A) ← (A)∀(T)	–	–	dH	+ + R –	53
28	CMP A	2	1	(TL)-(AL)	–	–	–	+ + + +	12
29	CMPW A	3	1	(T)-(A)	–	–	–	+ + + +	13
30	RORC A	2	1		–	–	–	+ + – +	03
31	ROLC A	2	1		–	–	–	+ + – +	02
32	CMP A,#d8	2	2	(A)- d8	–	–	–	+ + + +	14
33	CMP A,dir	3	2	(A)- (dir)	–	–	–	+ + + +	15
34	CMP A,@EP	3	1	(A)- ((EP))	–	–	–	+ + + +	17
35	CMP A,@IX+off	4	2	(A)- ((IX)+off)	–	–	–	+ + + +	16
36	CMP A,Ri	3	1	(A)- (Ri)	–	–	–	+ + + +	18 to 1F
37	DAA	2	1	decimal adjust for addition	–	–	–	+ + + +	84
38	DAS	2	1	decimal adjust for subtraction	–	–	–	+ + + +	94
39	XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
40	XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
41	XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
42	XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
43	XOR A,@IX+off	4	2	(A) ← (AL) ∀ ((IX)+off)	–	–	–	+ + R –	56
44	XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
45	AND A	2	1	(A) ← (AL) ^ (TL)	–	–	–	+ + R –	62
46	AND A,#d8	2	2	(A) ← (AL) ^ d8	–	–	–	+ + R –	64
47	AND A,dir	3	2	(A) ← (AL) ^ (dir)	–	–	–	+ + R –	65
48	AND A,@EP	3	1	(A) ← (AL) ^ ((EP))	–	–	–	+ + R –	67
49	AND A,@IX+off	4	2	(A) ← (AL) ^ ((IX)+off)	–	–	–	+ + R –	66
50	AND A,Ri	3	1	(A) ← (AL) ^ (Ri)	–	–	–	+ + R –	68 to 6F
51	OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
52	OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
53	OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
54	OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
55	OR A,@IX+off	4	2	(A) ← (AL) ∨ ((IX)+off)	–	–	–	+ + R –	76
56	OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
57	CMP dir,#d8	5	3	(dir) - d8	–	–	–	+ + + +	95
58	CMP @EP,#d8	4	2	((EP))- d8	–	–	–	+ + + +	97
59	CMP @IX+off,#d8	5	3	((IX)+off) - d8	–	–	–	+ + + +	96
60	CMP Ri,#d8	4	2	(Ri) - d8	–	–	–	+ + + +	98 to 9F
61	INCW SP	3	1	(SP)← (SP) + 1	–	–	–	– – – –	C1
62	DECW SP	3	1	(SP)← (SP) - 1	–	–	–	– – – –	D1

4.3 BRANCH INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	BZ/BEQ rel	3	2	if Z=1 then PC ←PC+rel	–	–	–	– – – –	FD
2	BNZ/BNE rel	3	2	if Z=0 then PC ←PC+rel	–	–	–	– – – –	FC
3	BC/BLO rel	3	2	if C=1 then PC ←PC+rel	–	–	–	– – – –	F9
4	BNC/BHS rel	3	2	if C=0 then PC ←PC+rel	–	–	–	– – – –	F8
5	BN rel	3	2	if N=1 then PC ←PC+rel	–	–	–	– – – –	FB
6	BP rel	3	2	if N=0 then PC ←PC+rel	–	–	–	– – – –	FA
7	BLT rel	3	2	if V⊻N=1 then PC←PC+rel	–	–	–	– – – –	FF
8	BGE rel	3	2	if V⊻N=0 then PC←PC+rel	–	–	–	– – – –	FE
9	BBC dir:b,rel	5	3	if (dir:b)=0 then PC←PC+rel	–	–	–	– + – –	B0 to B7
10	BBS dir:b,rel	5	3	if (dir:b)=1 then PC←PC+rel	–	–	–	– + – –	B8 to BF
11	JMP @A	2	1	(PC)←(A)	–	–	–	– – – –	E0
12	JMP ext	3	3	(PC)←ext	–	–	–	– – – –	21
13	CALLV #vct	6	1	vector call	–	–	–	– – – –	E8 to EF
14	CALL ext	6	3	subroutine call	–	–	–	– – – –	31
15	XCHW A,PC	3	1	(PC)←(A), (A)←(PC)+1	–	–	dH	– – – –	F4
16	RET	4	1	return from subroutine	–	–	–	– – – –	20
17	RETI	6	1	return from interrupt	–	–	–	restore	30

4.4 OTHER INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	PUSHW A	4	1	SP ← SP−2 (SP) ← A	–	–	–	– – – –	40
2	POPW A	4	1	A ← (SP) SP ← SP+2	–	–	dH	– – – –	50
3	PUSHW IX	4	1	SP ← SP−2 (SP) ← IX	–	–	–	– – – –	41
4	POPW IX	4	1	IX ← (SP) SP ← SP+2	–	–	–	– – – –	51
5	NOP	1	1	No operation	–	–	–	– – – –	00
6	CLRC	1	1	C ← 0	–	–	–	– – – R	81
7	SETC	1	1	C ← 1	–	–	–	– – – S	91
8	CLRI	1	1	C ← 0	–	–	–	– – – –	80
9	SETI	1	1	C ← 1	–	–	–	– – – –	90

4.5 F²MC-8L INSTRUCTION MAP

L / H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir :0,rel	INCW A	DECW A	JMP #A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir :1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV A,#A,T	MOV A,#A	CLRB dir:2	BBC dir :2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW A,#A,T	MOVW	CLRB dir:3	BBC dir :3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#dir	CMP A,#dir	ADDC A,#dir	SUBC A,#dir		XOR A,#dir	AND A,#dir	OR A,#dir	DAA	DAS	CLRB dir:4	BBC dir :4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV A,dir	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#dir	CMP dir,#dir	CLRB dir:5	BBC dir :5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC A,@IX+d	SUBC A,@IX+d	MOV @IX+d,A	XOR A,@IX+d	AND A,@IX+d	OR A,@IX+d	MOV @IX+d,#	CMP @IX+d,#	CLRB dir:6	BBC dir :6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#dir	CMP @EP,#dir	CLRB dir:7	BBC dir :7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#dir	CMP R0,#dir	SETB dir:0	BBS dir :0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#dir	CMP R1,#dir	SETB dir:1	BBS dir :1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#dir	CMP R2,#dir	SETB dir:2	BBS dir :2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#dir	CMP R3,#dir	SETB dir:3	BBS dir :3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#dir	CMP R4,#dir	SETB dir:4	BBS dir :4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#dir	CMP R5,#dir	SETB dir:5	BBS dir :5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#dir	CMP R6,#dir	SETB dir:6	BBS dir :6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#dir	CMP R7,#dir	SETB dir:7	BBS dir :7,rel	INC R7	DEC R7	CALLV #7	BLT rel

5. MASK OPTIONS

Table 5.15 Mask Options

NO	Type	MB89635 MB89636 MB89637	MB89P637 MB89W637	MB89PV630 MB89T635
	Specification method	**Select when ordering mask**	**Set by EPROM writer**	**Cannot be set**
1	Pull-up resistor P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	Can be selected for each pin (Note 1)	Can be set for each pin (Note 1, 2)	Pull-up resister not provided
2	Power-on reset Power-on reset available Power-on reset not available	Can be selected	Can be set	Power-on reset available
3	Main clock oscillation stabilization time selection (10 MHz) Approx.2^{18}/fch (Approx. 26.2 ms) Approx.2^{17}/fch (Approx. 13.1 ms) Approx.2^{14}/fch (Approx. 1.6 ms) Approx.2^{4}/fch (Approx. 0 ms) fch: Main clock frequency	Can be selected	Can be set	2^{18}/fch (26.2 ms)
4	Reset pin output Reset output provided Reset output not provided	Can be selected	Can be set	Reset output provided
5	System clock selection (Initial value)	Fixed to 64/fch (6.4 μs)	Fixed to 64/fch (6.4 μs)	Fixed to 64/fch (6.4 μs)
6	Single clock option Single clock Double clocks	Can be selected	Can be selected	MB89PV630-101 Single clock MB89T635-101 Single clock
				MB89PV630-102 Double clock MB89T635-102 Double clock

Notes:

1: When using P72 and P73 as standby cancel pins, the pull-up resistor should not be set.

2: Pull-up resistor cannot be selected for P50 to P53.

APPENDIX

APPENDIX 1 I/O MAP App.-3
APPENDIX 2 WRITING TO EPROM OF MB89P637 . App.-5
APPENDIX 3 SETTING PROM OPTION App.-6

APPENDIX 1 I/O MAP

Address	Read /Write	Register abbr	Register name	Bit name							
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	R/W	PDR0	Port 0 data register	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
01H	W	DDR0	Port 0 direction register	DD07	DD06	DD05	DD04	DD03	DD02	DD01	DD00
02H	R/W	PDR1	Port 1 data register	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10
03H	W	DDR1	Port 1 direction register	DD17	DD16	DD15	DD14	DD13	DD12	DD11	DD10
04H	R/W	PDR2	Port 2 data register	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20
05H	W	BCTR	External bus pin control register	—	—	—	—	—	—	HLD	BUF
06H	—	—	—	—	—	—	—	—	—	—	—
07H	R/W	SYCC	System clock control register	SCM	—	—	WT1	WT0	SCS	CS1	CS0
08H	R/W	STBC	Standby control register	STP	SLP	SPL	RST	TMD	—	—	—
09H	R/W	WDTE	Watchdog timer control register	CS	—	—	—	WTE3	WTE2	WTE1	WTE0
0AH	R/W	TBCR	Time-base timer control register	TBCF	TBIE	—	—	—	TBC1	TBC0	TBR
0BH	R/W	WPCR	Watch prescaler control register	WIF	WIE	—	—	—	WS1	WS0	WCLR
0CH	R/W	CHG3	Port 3 change register	—	—	CG35	CG34	CG33	—	—	—
0DH	R/W	PDR3	Port 3 data register	PD37	PD36	PD35	PD34	PD33	PD32	PD31	PD30
0EH	W	DDR3	Port 3 direction register	DD37	DD36	DD35	DD34	DD33	DD32	DD31	DD30
0FH	R/W	PDR4	Port 4 data register	—	—	—	—	PD43	PD42	PD41	PD40
10H	W	DDR4	Port 4 direction register	—	—	—	—	DD43	DD42	DD41	DD40
11H	R/W	BUZR	Buzzer register	—	—	—	—	—	—	BUZ1	BUZ0
12H	R/W	PDR5	Port 5 data register	—	—	—	—	PD53	PD52	PD51	PD50
13H	R/W	PDR6	Port 6 data register	PD67	PD66	PD65	PD64	PD63	PD62	PD61	PD60
14H	R	PDR7	Port 7 data register	—	—	—	PD74	PD73	PD72	PD71	PD70
15H	R/W	PCR1	PWC pulse width control register 1	EN	TOE	IE	—	—	UF	IR	BF
16H	R/W	PCR2	PWC pulse width control register 2	FC	RM	TO	—	C1	C0	W1	W0
17H	R/W	RLBR	PWC reload buffer register	RLB7	RLB6	RLB5	RLB4	RLB3	RLB2	RLB1	RLB0
18H	R/W	TMCR	16-bit timer control register	—	—	TCR	TCS1	TCS0	TCEF	TCIE	TCS
19H	R/W	TCHR	16-bit timer count register (H)	TC15	TC14	TC13	TC12	TC11	TC10	TC09	TC08
1AH	R/W	TCLR	16-bit timer count register (L)	TC07	TC06	TC05	TC04	TC03	TC02	TC01	TC00
1BH	—	—	—	—	—	—	—	—	—	—	—
1CH	R/W	SMR1	Serial mode register	SIOF	SICE	SCKE	SOE	CKS1	CKS0	BDS	SST
1DH	R/W	SDR1	Serial data register	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00
1EH	—	—	—	—	—	—	—	—	—	—	—
1FH	—	—	—	—	—	—	—	—	—	—	—
20H	R/W	ADC1	A/D control register 1	ANS3	ANS2	ANS1	ANS0	ADI	ADMV	SIFM	AD
21H	R/W	ADC2	A/D control register 2	—	TIM1	TIM0	ADCK	ADIE	ADMD	EXT	TEST
22H	R/W	ADDH	A/D data register (H)	—	—	—	—	—	—	ADD9	ADD8
23H	R/W	ADDL	A/D data register (L)	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
24H	R/W	EIC1	External interrupt control register 1	EIR1	—	SEL1	EIE1	EIR0	INTE	SEL0	EIE0
25H	R/W	EIC2	External interrupt control register 2	EIR3	—	SEL3	EIE3	EIR2	—	SEL2	EIE2
26H	—	—	—	—	—	—	—	—	—	—	—
27H	—	—	—	—	—	—	—	—	—	—	—
28H	R/W	CNTR1	PWM timer control register 1	PTX1	PTX2	P7M1	P7M2	SC11	SC10	SC21	SC20
29H	R/W	CNTR2	PWM timer control register 2	TPE1	TPE2	CK12	—	TIR1	TIR2	TIE1	TIE2

Address	Read /Write	Register abbr	Register name	Bit name							
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2AH	R/W	CNTR3	PWM timer control register 3	—	OE2	OE3	CH12	—	—	—	—
2BH	W	COMR1	PWM timer compare register 1	CM17	CM16	CM15	CM14	CM13	CM12	CM11	CM10
2CH	W	COMR2	PWM timer compare register 2	CM27	CM26	CM25	CM24	CM23	CM22	CM21	CM20
2DH	R/W	SMC	UART serial mode control register	PEN	SBL	CM1	CM0	SMDE	—	UCKE	UOE
2EH	R/W	SRC	UART serial rate control register	—	—	CR	SCS1	SCS0	RC2	RC1	RC0
2FH	R/W	SSD	UART serial status & data register	RDRF	ORRE	TDRE	TIE	RIE	PSEL	TD0/TP	RD0/RP
30H	R W	SIDR SODR	UART serial input data register UART serial output data register	SID7 SOD7	SID6 SOD6	SID5 SOD5	SID4 SOD4	SID3 SOD3	SID2 SOD2	SID1 SOD1	SID0 SOD0
31H to 7BH	—	—	—	—	—	—	—	—	—	—	—
7CH	W	ILR1	Interrupt level setting register 1	L31	L30	L21	L20	L11	L10	L01	L00
7DH	W	ILR2	Interrupt level setting register 2	L71	L70	L61	L60	L51	L50	L41	L40
7EH	W	ILR3	Interrupt level setting register 3	LB1	LB0	LA1	LA0	L91	L90	L81	L80
7FH	—	—	—	—	—	—	—	—	—	—	—

Note: – is empty space. Do not use this space.

APPENDIX 2 WRITING TO EPROM OF MB89P637

Use of a dedicated conversion socket permits writing to the MB89P637A with a general-purpose EPROM writ er. This allows the MB89P657A to have the functions equivalent to those of the MBM27C256A.

However, electronic signature mode cannot be used.

<Writing>

(1) Set the EPROM writer to the write mode of the MBM27C256A.

(2) Load program data into the addresses **0007_H** to **$7FFF_H$** of the EPROM writer.

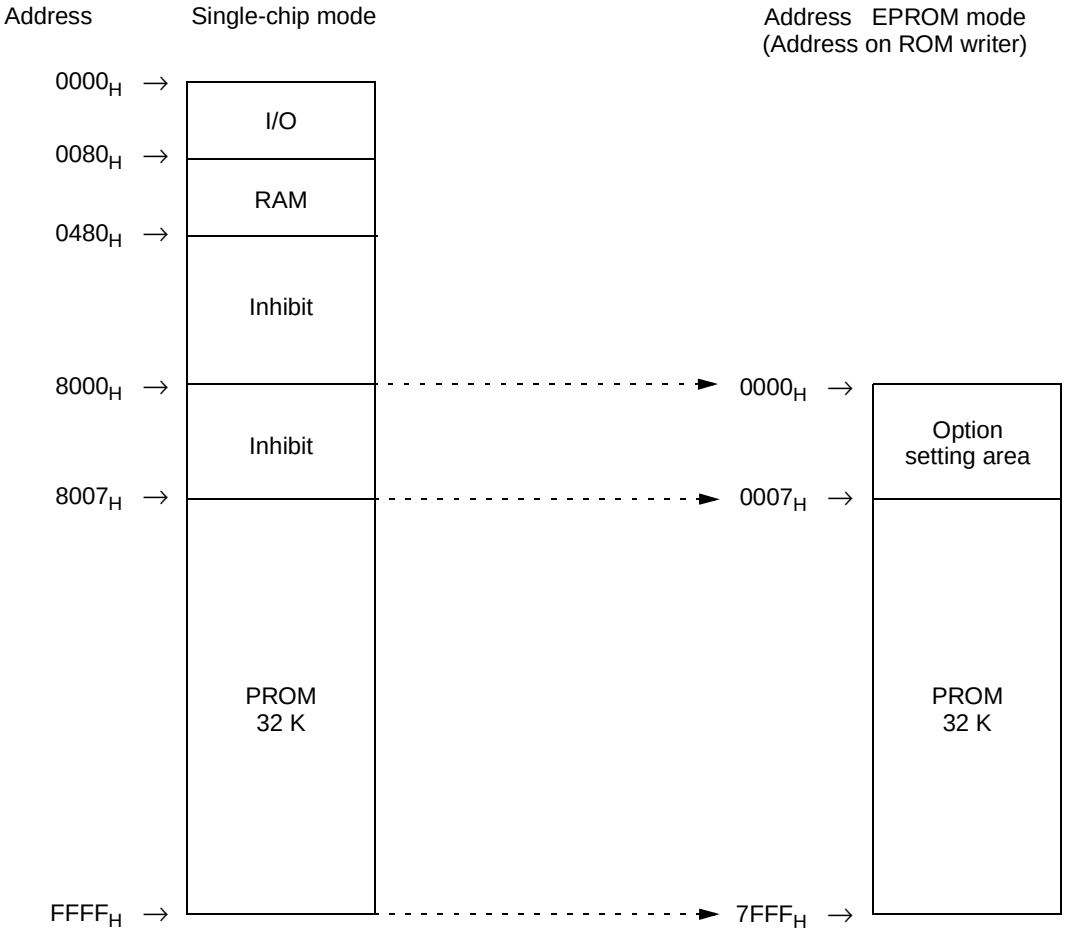
(Addresses **8000_H** to **$7FFF_H$** in single-chip operation correspond to the addresses **0000_H** to **$7FFF_H$** in the EPROM mode.)

Load the option information into the addresses **0000_H** to **0006_H** of the EPROM writer.

(See bit map in App. 6 for the correspondence of each option.)

(3) Use the EPROM writer to write data to the addresses **0000_H** to **$7FFF_H$**.

The memory space in each mode, such as PROM32K and option PROM, is shown below.



APPENDIX 3 SETTING PROM OPTION

Bit Map for PROM Option

	7	6	5	4	3	2	1	0
0000_H	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Single clock specification 1 Double clocks 2 Single clock	Reset pin output 1 Available 2 Unavailable	Power-on reset 1 Available 2 Unavailable	Oscillation stabilization (/fch) 11: 2^{18} 01: 2^{17} 10: 2^{14} 00: 2^{6}	
0001_H	P07 Pull-up resistor 1 Unavailable 0 Available	P06 Pull-up resistor 1 Unavailable 0 Available	P05 Pull-up resistor 1 Unavailable 0 Available	P04 Pull-up resistor 1 Unavailable 0 Available	P03 Pull-up resistor 1 Unavailable 0 Available	P02 Pull-up resistor 1 Unavailable 0 Available	P01 Pull-up resistor 1 Unavailable 0 Available	P00 Pull-up resistor 1 Unavailable 0 Available
0002_H	P17 Pull-up resistor 1 Unavailable 0 Available	P16 Pull-up resistor 1 Unavailable 0 Available	P15 Pull-up resistor 1 Unavailable 0 Available	P14 Pull-up resistor 1 Unavailable 0 Available	P13 Pull-up resistor 1 Unavailable 0 Available	P12 Pull-up resistor 1 Unavailable 0 Available	P11 Pull-up resistor 1 Unavailable 0 Available	P10 Pull-up resistor 1 Unavailable 0 Available
0003_H	P37 Pull-up resistor 1 Unavailable 0 Available	P36 Pull-up resistor 1 Unavailable 0 Available	P35 Pull-up resistor 1 Unavailable 0 Available	P34 Pull-up resistor 1 Unavailable 0 Available	P33 Pull-up resistor 1 Unavailable 0 Available	P32 Pull-up resistor 1 Unavailable 0 Available	P31 Pull-up resistor 1 Unavailable 0 Available	P30 Pull-up resistor 1 Unavailable 0 Available
0004_H	P53 Pull-up resistor 1 Unavailable 0 Available	P52 Pull-up resistor 1 Unavailable 0 Available	P51 Pull-up resistor 1 Unavailable 0 Available	P50 Pull-up resistor 1 Unavailable 0 Available	P43 Pull-up resistor 1 Unavailable 0 Available	P42 Pull-up resistor 1 Unavailable 0 Available	P41 Pull-up resistor 1 Unavailable 0 Available	P40 Pull-up resistor 1 Unavailable 0 Available
0005_H	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	P74 Pull-up resistor 1 Unavailable 0 Available	P73 Pull-up resistor 1 Unavailable 0 Available	P72 Pull-up resistor 1 Unavailable 0 Available	Empty Read/write possible	Empty Read/write possible
0006_H	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Reserved* Read/write possible

Notes:

* Always write 1 to reserved bit.

** Each bit is set to 1 when PROM data is erased.