mas
MICRO ANALOG SYSTEMS

MAS9191A

Single Chip AMPS/ETACS/NAMPS Audio/Data Processor

- **Single chip solution for all audio and data processing**
- **Low power consumption with several power down modes**
- **SAT decoding and transponding circuitry**
- **Simple 4-wire serial interface**

DESCRIPTION

The MAS9191A is a high integration BeCMOS IC for implementing the audio and data signal processing in AMPS, ETACS or NAMPS cellular phones. The power consumption of the device is very low due to several automatic and software controlled power down modes as well as the low power characteristics of the BeCMOS process. DTMF receiver is also included to enable answering machine functions for the cellular phone. Only a minimal number of external components are needed to meet typical baseband requirements.

FEATURES

- Voice signal processing including compressor, expander, de-emphasis and pre-emphasis filters and digital gain adjustments
- DTMF and ST generators and DTMF receiver
- Busy/Idle extraction and arbitration with TX block, voting, BCH, data buffering and framing, DCC coding with hardware
- Three 8-bit DACs and two operational amplifiers
- On-chip oscillator with clock output for uP
- 3.3V or 5V operation with low power consumption(RX block at 2mA/3.3V)
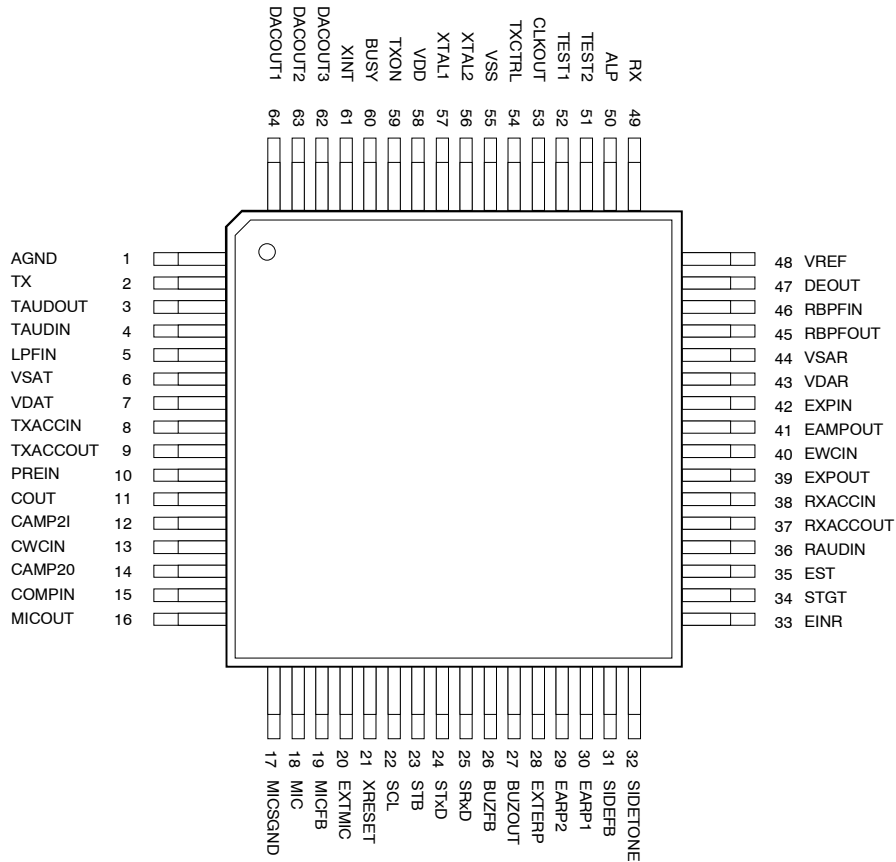- 64-pin TQFP package, -40..85°C operation range

APPLICATIONS

- AMPS/ETACS Cellular phone
- NAMPS Cellular phone

BLOCK DIAGRAM

1

mas MICRO ANALOG SYSTEMS
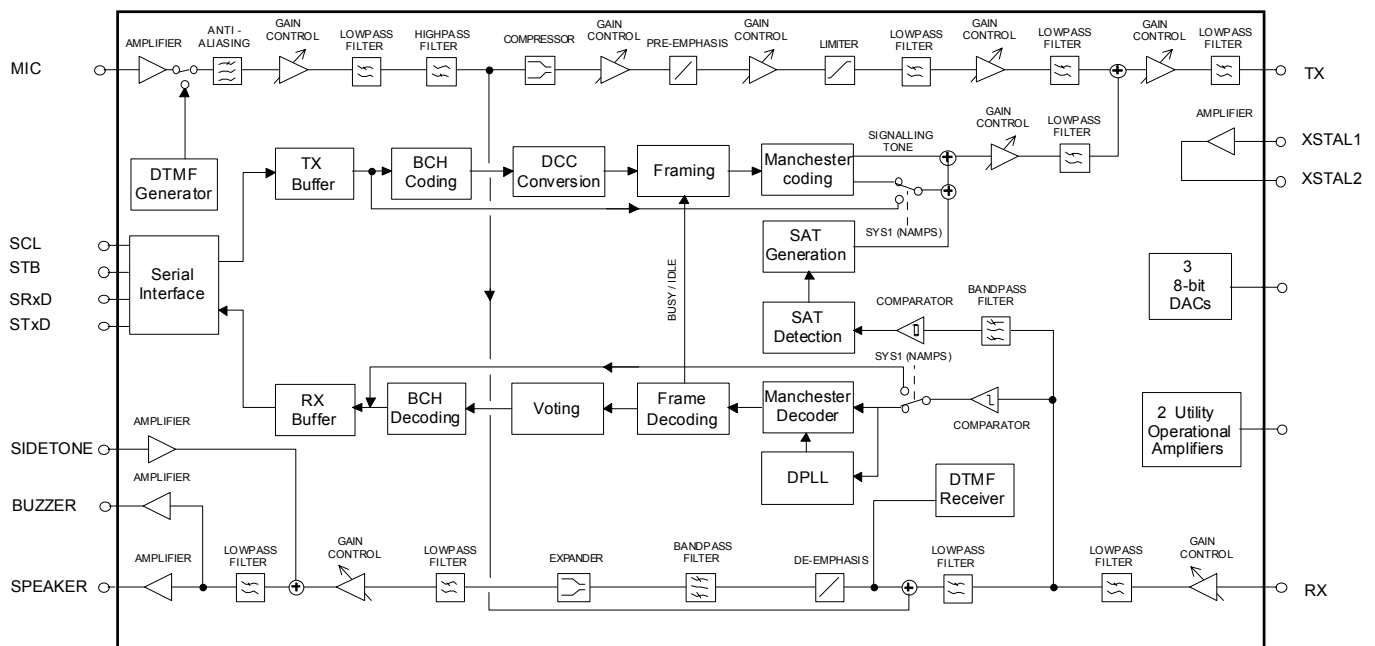
PIN CONFIGURATION

TQFP64 package

PIN DESCRIPTION

Pin name	Pin	Type	Function
AGND	1	AO	Signal ground. The signal ground is generated internally and is equal to $V_{DD}/2$. The analog ground needs an external capacitor connected to system ground.
TX	2	AO	Transmitted data signal output. Connect this output through a 22nF capacitor to the transmitter.
TAUDOUT	3	AO	TX audio output from the TX audio block..
TAUDIN	4	AI	TX audio input. The input for the TX audio signal, normally connected through a 22nF capacitor to TAUDOUT
LPFIN	5	AI	Input for TX limiter, lowpass filter or GC6 depending on the position of switches S15 and S16. The pin is normally left unconnected.
VSAT	6	G	Ground for TX. Connect to system ground.
VDAT	7	P	Power supply for TX block. Use a bypass capacitor between pins VSAT and VDAT.
TXACCIN	8	AI	TX block extra Op Amp input. See application note in the APPLICATIONS section.
TXACCOUT	9	AO	TX block Op Amp output.
PREIN	10	AI	Pre-emphasis filter input. Filter has a +6dB/octave (±1dB) frequency response in the range 300Hz...3kHz.
COUT	11	AO	Compressor output signal. The compression ratio is 2:1

PIN DESCRIPTION

Pin name	Pin	Type	Function
CAMP2I	12	AI	Compressor 2nd amplifier input as well as GC4 input. Use an external 22nF capacitor between COUT and this pin.
CWCIN	13	AI	Compressor window comparator input. Use an external 22nF capacitor between CAMP2O and this pin.
CAMP2O	14	AO	Compressor 2nd amplifier output.
COMPIN	15	AI	Compressor input. The input is connected through a 22nF capacitor to MICOUT.
MICOUT	16	AO	Microphone amplifier output. See COMPIN. This output is used as a source for the side tone and for detection of the TX audio level.
MICSGND	17	AO	Microphone signal ground. This is the internal signal ground $V_{DD}/2$. If noise appears on the microphone signal an external capacitor may be needed between this pin and system ground.
MIC	18	AI	Microphone amplifier input. Using this pin and the MICFB output the microphone amplifier frequency response can be adjusted according to the microphone used. The level at this input should be in the range 5..10mVrms. The maximum gain of the microphone amplifier is 30 dB.
MICFB	19	AO	Microphone amplifier feedback output
EXTMIC	20	AI	External microphone input. The level should be 100mVrms at 1kHz.
XRESET	21	I	Master reset. Active low.
SCL	22	I	Serial interface clock input. The data is transferred in both directions at the rising edge of this signal.
STB	23	I	Serial interface strobe signal. With strobe signal the MAS9191A stores the given address from the serial interface buffer and enters the data mode. The serial interface stays in the data mode until eight SCL pulses are received after the strobe signal.
STxD	24	O	Serial interface transmit data output.
SRxD	25	I	Serial interface receive data input
BUZFB	26	AI	Buzzer feedback is the input for the buzzer driver.
BUZOUT	27	AO	Buzzer output.
EXTERP	28	AO	Output for external accessories
EARP1	29	AO	Earpiece differential outputs of earpiece amplifier. The outputs are capable of driving a ceramic earpiece directly.
EARP2	30	AO	
SIDEFB	31	AO	Side tone feedback output
SIDETONE	32	AI	Side tone input. The level of the side tone is controlled with external components.
EINR	33	AI	External RX input.
STGT	34	AI	Steering control input for DTMF receiver. When the level at this input changes from below $V_{DD}/2$ to above $V_{DD}/2$ the pin is pulled up internally. When this occurs the DTMF tone is stored and an interrupt is generated.
EST	35	AO	Enable Steering output. This pin is high when the DTMF receiver has detected a valid DTMF tone.
RAUDIN	36	AI	Input for filter 6. Connect through a 22nF capacitor to the expander output (EXPOUT).
RXACCOUT	37	AO	Output of uncommitted Op Amp in MAS9191A. The Op Amp is normally used for RX audio level detection. The application circuit for this function is in the APPLICATIONS section. Connect the level detected by the circuit to the A/D converter of the general purpose micro controller.

PIN DESCRIPTION

Pin name	Pin	Type	Function
RXACCIN	38	AI	RX block extra Op Amp input
EXPOUT	39	AO	Expander output. The expander ratio is 1:2.
EWCIN	40	AI	Expander window comparator input. Connect a 22nF capacitor between EWCIN and EAMPOUT.
EAMPOUT	41	AO	Expander amplifier output.
EXPIN	42	AI	Expander input. Connect a 22nF capacitor between EXPIN and RBPFOUT.
VDAR	43	P	Power supply for RX audio block. Use a bypass capacitor between VDAR and VSAR.
VSAR	44	G	Ground for RX block. Connect to system ground.
RBPFOUT	45	AO	RX bandpass filter output.
RBPFIN	46	AI	RX bandpass filter input. Connect a 22nF capacitor between this pin and DEOUT
DEOUT	47	AO	RX de-emphasis filter output. The filter has a -6dB/octave (±1dB) frequency response in the range 300Hz...3kHz.
VREF	48	AO	Reference voltage. Connect a capacitor between this pin and system ground.
RX	49	AI	RX input from RF. This level is 100mVrms at 1kHz.
ALP	50	AI	Audio loop input. Connect through a 22nF capacitor to the TX pin.
TEST2	51	I	Test input. Connect to ground during normal operation.
TEST1	52	I	Test input. Connect to ground during normal operation. If connected to V_{DD} and TEST2 is connected to ground, the external clock can then be connected to XTAL1.
CLKOUT	53	O	4.8 MHz clock output from oscillator circuit.
TXCTRL	54	AO	Transmission control output. If a TX collision occurs this open-collector output is set to low. The TXCTRL will remain low until the TX block is reset with the TXRST bit or with XRESET.
VSS	55	G	Digital ground. Connect a bypass capacitor between VSS and VDD.
XTAL2	56	O	Crystal oscillator output.
XTAL1	57	I	Crystal oscillator input or external clock input if TEST1 is high and TEST2 is low.
VDD	58	P	Power supply input for digital block.
TXON	59	O	Transmission detection for debugging. This output indicates when a transmission is occurring.
BUSY	60	O	Busy/Idle output. Indicates the state of the busy/idle bit.
XINT	61	O	Active low interrupt output to micro controller. The interrupt is active until status register 10_{HEX} is read.
DACOUT3	62	AO	Output of DAC 3. The DAC output is connected to ground if the DAC is in power down mode. The output of the DAC is controlled by register 18_{HEX}. Enter the values in two's complement form into the DAC register.
DACOUT2	63	AO	Output of the DAC 2. The control register is located at 17_{HEX}.
DACOUT2	64	AO	Output of the DAC 1. The control register is located at 16_{HEX}.

MICRO ANALOG SYSTEMS

ABSOLUTE MAXIMUM RATINGS

(GND = 0V)

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage*	V_{DD}			6.0	V
Storage temperature*	Ts		-55	+125	^oC

RECOMMENDED OPERATION CONDITIONS

(GND = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage*	V_{DD}	Ta=-40...85^oC	3.0	3.3	3.6	V
Supply current	I_{DD}	Ta=-40...85^oC, V_{DD}=3.3V±5%	1.0	2.5	23	mA
Operating temperature*	Ta		-40		+85	^oC

ELECTRICAL CHARACTERISTICS

◆ **Digital inputs**

(Ta=-40...85^oC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage*	V_{IH}		$0.7V_{DD}$			V
Input low voltage*	V_{IL}				$0.7V_{DD}$	V
Input leakage current	I_{IL}		-10		+10	uA
Input capacitance load*	C_I				1	pF

◆ **Digital outputs**

(VDD = 3.3V±5%, Ta=-40...85^oC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output low voltage*	V_{OL}	XINT @ +0.4mA			$0.1V_{DD}$	V
Output high voltage*	V_{OH}	XINT @ -0.4mA	$0.9V_{DD}$			V

◆ **Analog inputs**

(Ta=-40...85^oC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
External microphone level*	V_{EXTMIC}			100		mV_{rms}
Microphone level*	V_{MIC}			10		mV_{rms}
RX input level*	V_{RX}			100		mV_{rms}

* Guaranteed by design only.

ELECTRICAL CHARACTERISTICS

◆ Analog outputs

(Ta=-40...85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	AGND		$V_{DD}/2-0.1V$		$V_{DD}/2+0.1V$	V
Reference voltage	V_{ref}			AGND +1.2V		V
Earpiece output impedance*	Z_O				500	Ω
Earpiece load resistance*	R_L		1			kΩ
Earpiece series load capacitance*	C_L				120	nF
External earpiece load resistance*	R_L		30			kΩ
External earpiece load capacitance*	C_L				1	nF
Earpiece amplifier gain	A_{vol}		1.26		3.26	dB
Rx level	V_O	RX level 100mV$_{rms}$		200		mV$_{rms}$
Earpiece level non-differential*	V_O	RX level 100mV$_{rms}$		70		mV$_{rms}$
Earpiece level differential*	V_O	RX level 100mV$_{rms}$		155		mV$_{rms}$
TX level	V_O	EXTMIC level 100mV$_{rms}$		200		mV$_{rms}$
DTMF signal levels at TX	V_O	f = 697 … 941 Hz	-1		+1	dB
		f = 1209 … 1633 Hz	-1		+1	
SAT signal level at TX	V_O	ETACS	131	148	163	mV$_{rms}$
		AMPS	123	138	152	
Data signal level at TX (AMPS/ETACS)	V_O		470	556	612	mV$_{rms}$
ST signal level at TX (AMPS/ETACS)	V_O		488	556	612	mV$_{rms}$
Data, ST, SAT level at TX	V_O	NAMPS, DTX mode off	81	93	105	mV$_{rms}$
		NAMPS, DTX mode on	325	373	421	
DACs, output level	V_O		0.3V		$V_{DD}-0.3$	V
DACs, differential nonlinearity	DNL		-0.95		+0.95	LSB
DACs, integral nonlinearity	INL		-2.0		+2.0	LSB
DACs, settling time*		Vdac ±1%			10	ms
DACs, load resistance*	R_L		30			kΩ
DACs, load capacitance*	C_L				80	pF
OP AMPs, load capacitance*	C_L				1	nF

* Guaranteed by design only.

ELECTRICAL CHARACTERISTICS

◆ Expander

(Ta=-40...85°C)

Parameter	Conditions	Min	Typ	Max	Unit
Expanding ratio*			1:2		
Operation range input*		-24		+10	dB
Operation range output*		-48		+20	dB
Gain step*			1.333		dB
Integral nonlinearity		-0.5		+0.5	dB
Attack time*		7.4	9.2	14.3	ms
Decay time*		9.5	11.9	14.3	ms

◆ Compressor

(Ta=-40...85°C)

Parameter	Conditions	Min	Typ	Max	Unit
Compressing ratio*			2:1		
Operation range input*		-39.4		+20	dB
Operation range output*		-19.7		+10	dB
Gain step*			1.333		dB
Integral nonlinearity		-0.5		+0.5	dB
Attack time*		2.9	3.9	4.6	ms
Decay time*		13	16.9	20	ms

◆ AC Characteristics

(Ta=-40...85°C)

Parameter	Conditions	Min	Typ	Max	Unit
RX S/N ratio	Psophometric weighting	48			dB
TX S/N ratio		50			dB
RX THD				34	dB
TX THD				34	dB
Crosstalk RX to TX*			50		dB
Crosstalk TX to RX*			50		dB
Mute attenuation		50			dB

* Guaranteed by design only.

mas
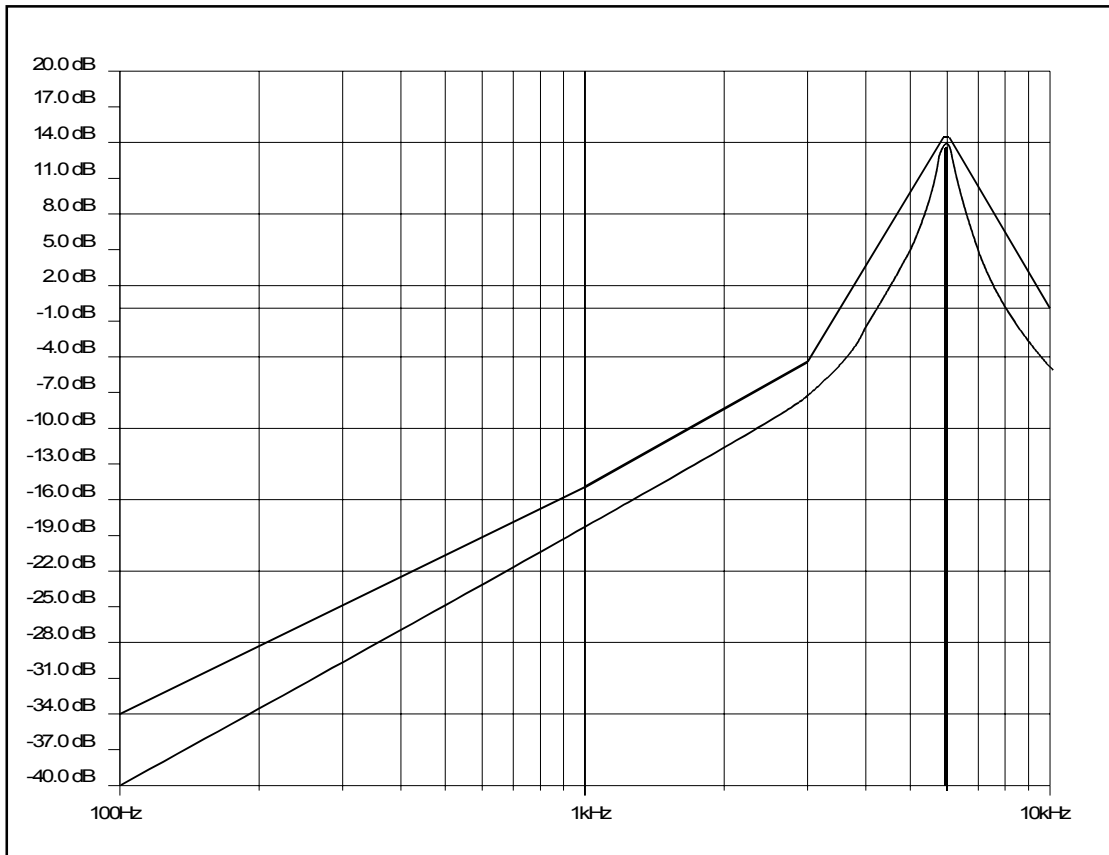MICRO ANALOG SYSTEMS

ELECTRICAL CHARACTERISTICS
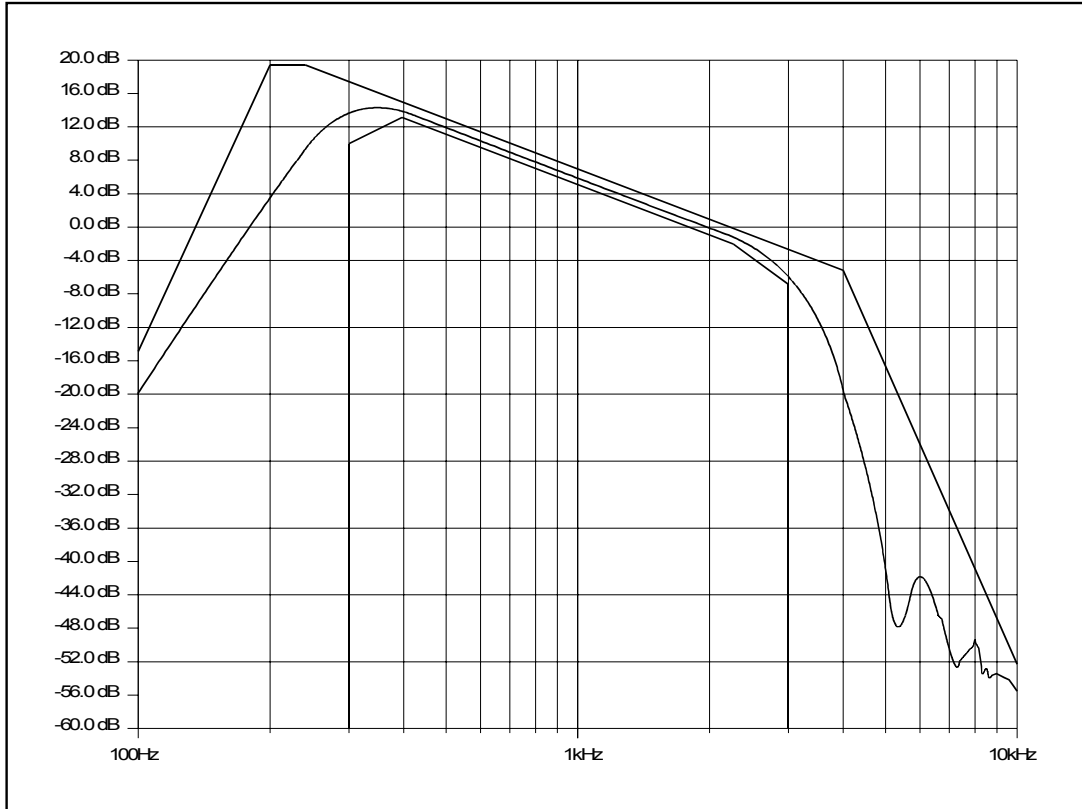
RX Total frequency response
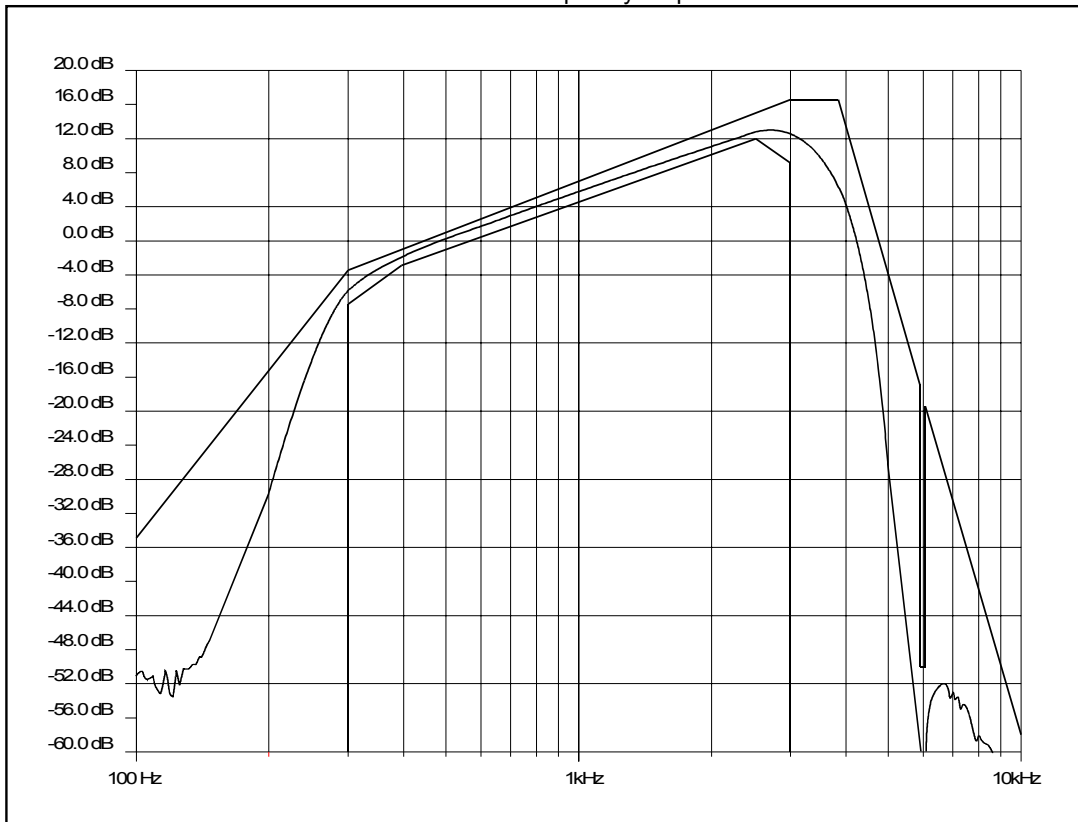
TX Total frequency response

# ELECTRICAL CHARACTERISTICS

Filter F2 frequency response

ELECTRICAL CHARACTERISTICS

◆ Timing

(Ta=-40...85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCL cycle	T1		0.5			us
Data setup time	T2		60			ns
Data hold time	T3		20			ns
STB rising edge after SCL falling edge	T4		10			ns
STB width	T5		5			us
MSB data bit valid after STB falling edge	T6	Register read			5	us
SCL rising edge after SCL falling edge	T7	Register read	5			us
Next data bit valid after SCL falling edge	T8	Register read	30			ns
Ready for next address	T9		7			us

◆ Timing Diagram

mas
MICRO ANALOG SYSTEMS
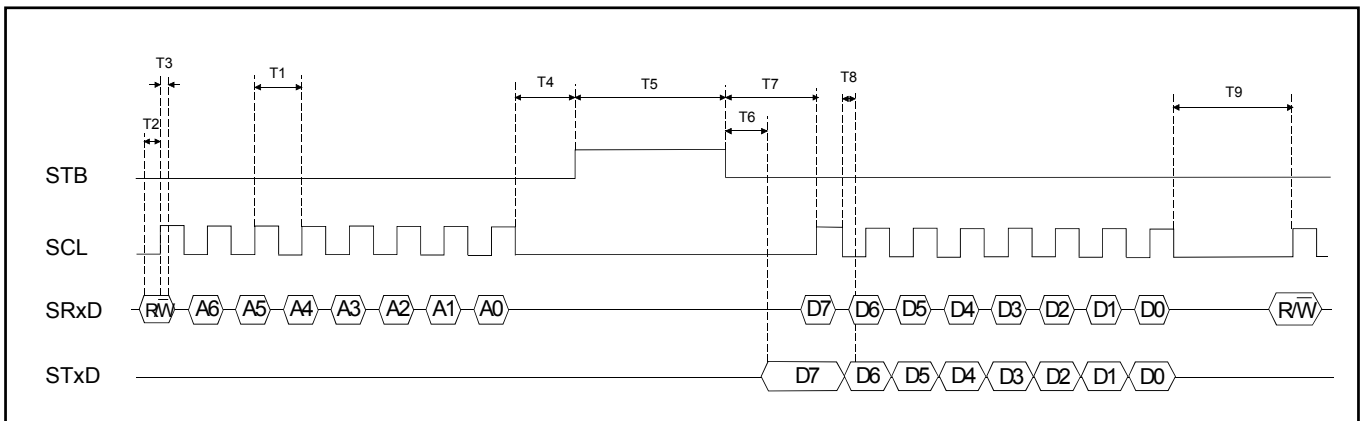
FUNCTIONS

◆ Schematic diagram

mas MICRO ANALOG SYSTEMS
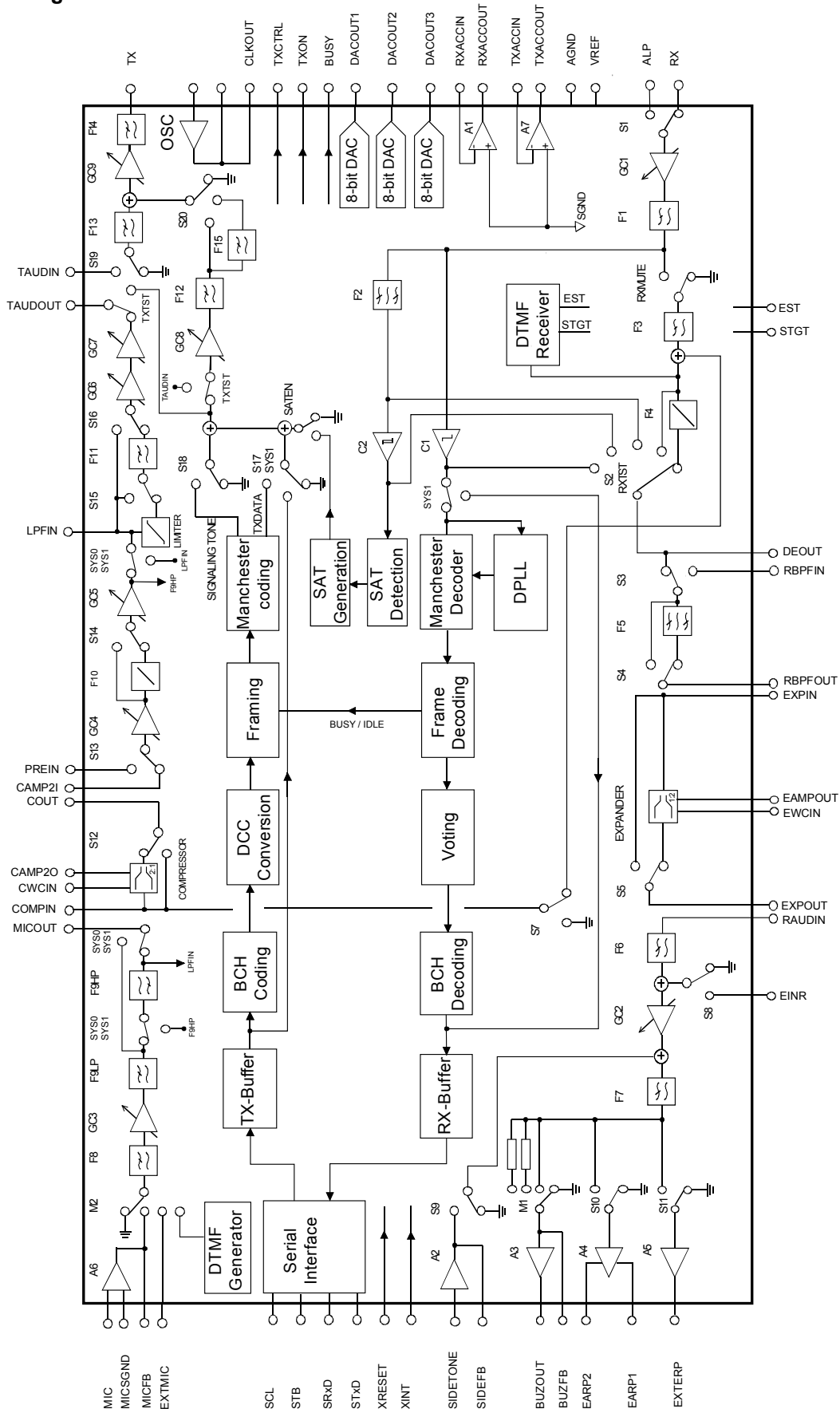
FUNCTIONS

◆ Data Reception

The data reception block is in the power down state after a reset. The power down mode of the block is controlled by the RXSIP bit in register 07_{HEX}. The Manchester encoded data is received through the RX pin. The data is amplified with GC1 and filtered with filter F1. The comparator C1 is used to convert data to a digital signal. The digital PLL circuit recovers the bit clock from the Manchester encoded data. The bit clock is 8kHz in the ETACS mode and 10kHz in the AMPS mode. The mode is set with the SYS0 bit of register 12_{HEX}. The recovered bit clock is used in the Manchester decoder and the data is then transmitted to the frame decoding block. The frame decoding block finds dotting sequences, busy/idle bits and word syncs from the data. To avoid data being generated by random noise, the frame decoding block enters the data reception mode only after it has received two consecutive word syncs (11100010010) separated by 463 bits in the forward control channel and 77 bits in the forward voice channel. In this case the voting and BCH block are activated. When the frame decoding block loses five consecutive synchronization patterns it rejects the data reception mode and sets the voting and BCH blocks in power down state. The voice and control channel modes are selected with the CTCV bit of register 12_{HEX}.

Forward control channel data format. The numbers under the frames show the number of bits in each section.

Busy/Idle	Bit Sync	Busy/Idle	Word Sync	Busy/Idle	Data	Busy/Idle	Data	Busy/Idle	Data	Busy/Idle	Data
1	10	1	11	1	10	1	10	1	10	1	10
				1. Repeat of word A							

Busy/Idle	Data	Busy/Idle	Data	Busy/Idle	Data	Busy/Idle	Data	Busy/Idle	Data	Busy/Idle	Data
1	10	1	10	1	10	1	10	1	10	1	10
1. Repeat of word B						2. Repeat of word A					

Busy/Idle	Data	Busy/Idle	Data	Busy/Idle	Data	Busy/Idle	Data	Busy/Idle	Bit Sync	Busy/Idle	
1	10	1	10	1	10	1	10	1	10	1	
5. Repeat of word B											

bit sync = 1010101010   word sync = 11100010010

The busy/idle bits are extracted from the data. Busy/idle bits are used to indicate the current status of the reverse control channel (RECC). The RECC is busy if the busy/idle bit is low and idle if the busy/idle bit is high. The state determination is made with 2-out-of-3 voting. The TX block uses the busy/idle indication for arbitration. The STR bit of register 12_{HEX} selects the words from stream A or stream B.

Forward voice channel data format.

Bit Sync	Word Sync	1.Word repeat	Bit Sync	Word Sync	2.Word repeat	Bit Sync	Word Sync	3.Word repeat
101	11	40	37	11	40	37	11	40
	Bit Sync	Word Sync	9.Word repeat	Bit Sync	Word Sync	10.Word repeat	Bit Sync	Word Sync	11.Word repeat
	37	11	40	37	11	40	37	11	40

On the forward voice channel after bit synchronization and word synchronization are received and the AUMUT bit in register 13_{HEX} is set to high, the RX audio block will be muted until the 920 bits are received. The repeated words are transferred to the voting block. The voting is done bit by bit, 3-out-of-5. If three consecutive words are identical, the receiver is powered down and no remaining words are read. After the voting block the data is transmitted to the BCH block. This block performs decoding of the received BCH coded data. The following polynomial is used:

$$G(x) = x^{12} + x^{10} + x^8 + x^5 + x^4 + x^3 + x^0$$

If only one error occurs in data the BCH block can correct it. If more than one error occurs the BCH block cannot correct them and the BCHER bit of register 11_{HEX} is set to high. The BCH block transfers the data to the RX buffer. When the buffer is full the RXWRD bit of register 10_{HEX} is set to high and this causes interrupt line XINT to go active. When register 10_{HEX} is read the interrupt is cleared. The data buffer can be read by reading register 15_{HEX} four times. If the next word is coming and the previous word has not been read from the buffer, the word is missed. The new and the old words are compared.

FUNCTIONS

◆ Data Transmission

After a reset the TX block is in power down. The power down mode is controlled by bit TXSIP (TX section in power down) in register 07_{HEX}. The TXRST bit located in register 12_{HEX} is used every time a TX collision occurs or for any other TX block reset causes. When the device is ready to receive data, the TXWRD bit of register 10_{HEX} is high. If five bytes are written into register 19_{HEX} the data transmission begins. The data is transferred from the serial interface to the TX buffer and the TXWRD bit is set high again, which causes XINT to become active.

When the block comes out of power down mode the XINT is active because the device is ready to receive data (TXWRD goes high). The lower nibble of the fifth byte is ignored. The 36 bits of data are coded by the BCH coder with following polynomial:

$$G(x) = x^{12} + x^{10} + x^8 + x^5 + x^4 + x^3 + x^0$$

The BCH coder adds 12 parity bits to the data and the data is transferred to the DCC coding block. The DCC coder adds a digital color code on the reverse control channel (RECC) according following table.

DCC(1:0)	Coded DCC
00	0000000
01	0011111
10	1100011
11	1111100

The framing block adds bit sync (101010...10) and word sync (11100010010) sequences to the frames and performs needed repeats depending on the mode.

Reverse control channel data format. The numbers under the frames show the number of bits in each section.

Bit sync	Word sync	Coded DCC	First word repeated 5 times	Second word repeated 5 times	
30	11	7	240	240	

Reverse voice channel data format.

	Bit Sync	Word Sync	1.Repeat of word 1	Bit Sync	Word Sync	2.Repeat of word 1	Bit Sync	Word Sync	
	101	11	48	37	11	48	37	11	
	Bit Sync	Word Sync	5.Repeat of word 1	Bit Sync	Word Sync	1.Repeat of word 2	Bit Sync	Word Sync	
	37	11	48	37	11	48	37	11	
	Bit Sync	Word Sync	5.Repeat of word 2						
	37	11	48						

The Manchester encoder block encodes the data into a Manchester coded format with bit clock. The bit clock is 8kHz in the ETACS mode and 10kHz in the AMPS mode. The mode can be controlled by bit SYS0 of register 12_{HEX}. The data polarity can be inverted with bit INVTX of register 13_{HEX}. If the BUSY bit does not go active between 56 and 104 bits of the transmitted message a transmission collision occurs. In this case the data which is in the TX block and the data that the user is writing to the device will not be transmitted. The TXCOL bit of register 10_{HEX} will go high in this case and cause an interrupt. The TXCOL will remain active until the TX block is reset with the TXRST bit of register 12_{HEX}. If the TXCTREN bit is active in register 12_{HEX} the TXCTRL output turns the transmitter off when a TX collision occurs. If the AUMUT bit in register 13_{HEX} is set to high the TX audio block is muted with switch S19 on the voice channel while data transmission is occurring.

FUNCTIONS

◆ Data Reception in Narrow Band mode

Forward voice channel data format for narrow band.

DSAT	Sync word	Data	DSAT
24	30	40	24

Sync word = 011001010110101001100110100110

DSAT = Digital Supervisory Audio Tone is one of seven 24-bit digital sequences added to the voice transmission. DSAT is transmitted at 200 NRZ bits/second. The following is a list of the seven DSAT sequences.

	DSAT sequence
0	2556CB$_{HEX}$
1	255B2B$_{HEX}$
2	256A9B$_{HEX}$
3	25AD4D$_{HEX}$
4	26AB2B$_{HEX}$
5	26B2AD$_{HEX}$
6	2669AB$_{HEX}$

The 40-bit long data sequence is generated at a 100 Manchester bits/second rate. The data sequence contains 28 bits of data and 12 parity bits.

The incoming data is captured by two 8-bit shift registers. When one shift register is full the RXWRD flag is set and an interrupt is generated. The captured data must be read by the micro controller within 20ms after the interrupt. Meanwhile, the other shift register is being filled and when it is full a new interrupt is generated. The shift registers are clocked in at 400 Hz. Two samples of each state of both the 200 NRZ bits/second data and the 100 Manchester bits/second data are loaded into the registers. Note that there are as many transitions in the 200 NRZ bits/second data as in the 100 Manchester bits/second data. The micro controller will then be used to filter the digital bit sequence and detect the DSAT, SYNC WORD and DATA out of the bit stream. The DATA must be checked with following algorithm:

$$G(x) = x^{12} + x^{10} + x^{8} + x^{5} + x^{4} + x^{3} + x^{0}$$
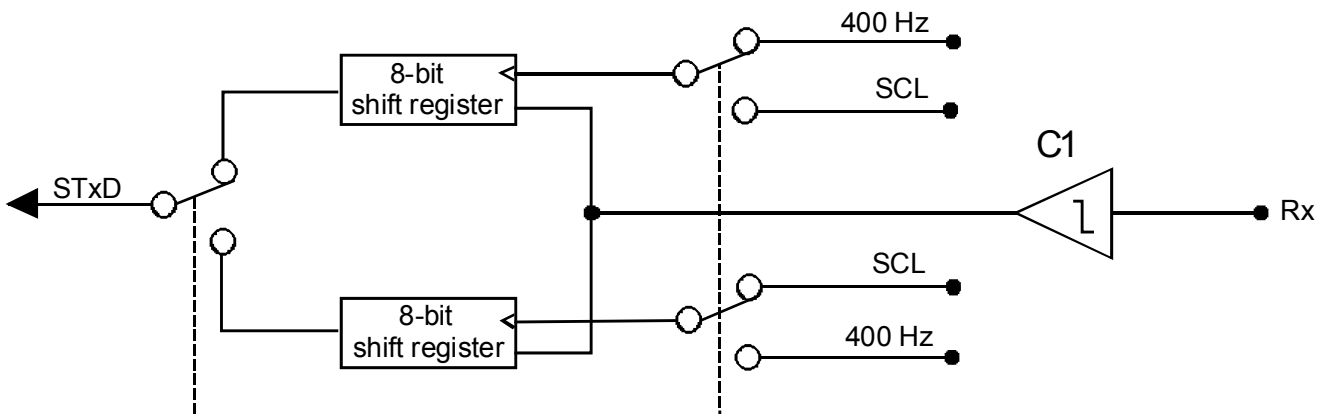
FUNCTIONS

◆ Data Transmission in Narrow Band mode

Reverse voice channel data format for narrow band.

DSAT/DST	Sync word	Data	DSAT/DST
24	30	40	24

Sync word = 011001010110101001100110100110

The data contains 36 data bits and 12 parity bits. The transmitted data is 100 bits/sec Manchester code. DSAT, DST and SYNC WORD are transmitted as 200 bits/sec NRZ code. The DSAT on the TX side is similar to the DSAT on RX side. However, under certain conditions the inverted DSAT, or DST (Digital Signaling Tone), must be transmitted. The DST is one of seven 24-bit digital sequences consisting of the logical inverse of the seven DSAT sequences. The conversions DSAT/ DST and DST/DSAT must be made without disturbing the phase of the DSAT. There is also a special 24-bit digital mask for each of the seven sequences. The mask defines the first bit to be inverted when converting from DSAT to DST or vice versa. Only when the bit in the mask is one can the polarity be changed.

	DSAT	DST	MASK
0	$2556CB_{HEX}$	$DAA934_{HEX}$	$FF003E_{HEX}$
1	$255B2B_{HEX}$	$DAA4D4_{HEX}$	$0BBF82_{HEX}$
2	$256A9B_{HEX}$	$DA9564_{HEX}$	$BD780F_{HEX}$
3	$25AD4D_{HEX}$	$DA52B2_{HEX}$	$3FF118_{HEX}$
4	$26AB2B_{HEX}$	$D954D4_{HEX}$	$0AE6F6_{HEX}$
5	$26B2AD_{HEX}$	$D94D52_{HEX}$	$8001FF_{HEX}$
6	$2669AB_{HEX}$	$D69654_{HEX}$	$1C0FCD_{HEX}$

MAS9191A does not include frame coding logic for narrow band operation. The DSAT, DST, SYNC WORD and DATA must be generated by micro controller. The BCH function must also be performed by the micro controller using the following algorithm:

$$G(x) = x^{12} + x^{10} + x^8 + x^5 + x^4 + x^3 + x^0$$

The generated bit sequence is written into shift register 19_{HEX} 8 bits at a time. While the next byte is written to one of the 8-bit shift registers the other is clocked out with a 200Hz clock. Each time the contents of a shift register transmitted, the TXWRD flag is set and an interrupt is generated. Note that 200 NRZ bits/second data has as many transitions as 100 Manchester bits/second data.
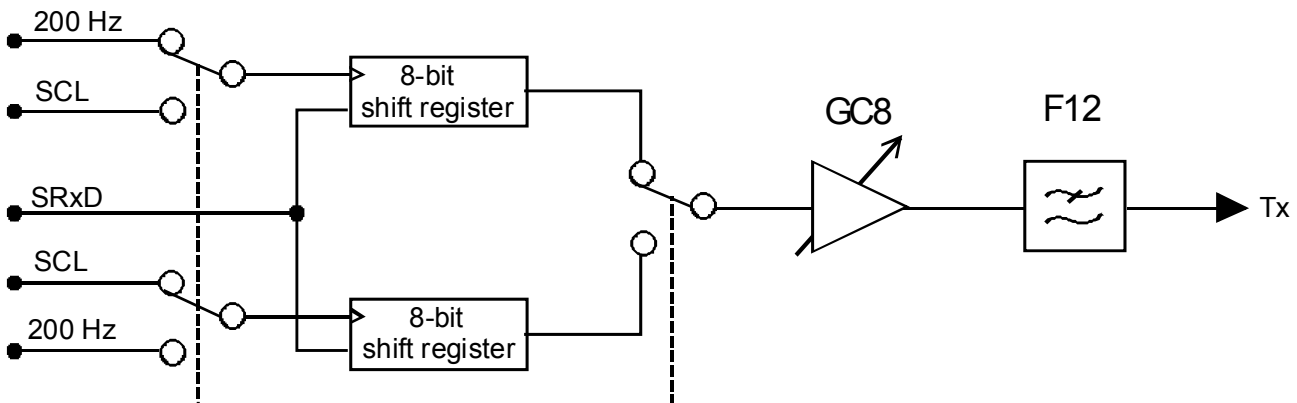
FUNCTIONS

◆ SAT detection & regeneration

SAT detection is active on voice channel in AMPS or TACS mode (SYS1=0). The supervisory audio tone is detected with a digital PLL. The detector compares the received SAT to the given SAT color code (SCC). When the given SAT is detected the SATDET bit of register 11_{HEX} is set to high. If SATINTEN bit of register 13_{HEX} is on the rising and falling edge of SATDET will cause the interrupt SATINT. On the voice channel the SAT regeneration can be enabled with bit SATEN of register 14_{HEX}. By setting bit NOMSAT of register 14_{HEX} nominal SAT frequency is generated. Otherwise, the SAT output frequency will follow received SAT frequency. The block is in power down mode when the TXSIP (transmit section in power down) bit is active in register 07_{HEX}. After a reset the block is in power down mode.

| SCC1	SCC0	SAT frequency
0	0	5970 Hz
0	1	6000 Hz
1	0	6030 Hz
1	1	invalid code

◆ SAT, ST or Data Transmission

The SAT and signaling tone (ST) are sent only on the voice channel in AMPS or TACS mode (SYS1=0). The SATEN and STON can be used to control the SAT and ST transmission. However, the device will automatically stop transmitting SAT and ST signals whenever data is being transmitted, even though SATEN or STON is high. The signaling tone is 8kHz in ETACS and 10kHz in AMPS. Also, switch S17 for TX data and switch S18 for ST can be used to disable the transmission. The switches must be on during transmission. The control bits for these switches are located in register $0D_{HEX}$. The SAT, TXDATA and the ST are summed and amplified with GC8. The gain of the amplifier is -3.75dB...+3.75dB with 16 steps. The adjustment is made with bits 0..3 of register $0D_{HEX}$. After being amplified the signal is filtered with 4th order SC filter F12. The cutoff frequency of the filter is 19kHz in AMPS, 15kHz in ETACS and 200Hz in NAMPS (SYS1=1). The gain of the filter at 1kHz is 0dB. In the NAMPS mode, the signal is then fed to low pass filter F15, which is a 2nd order RC type filter. After filtering the signal is summed to the TX audio signal depending on the state of switch S20. The switch is controlled by bit 6 of register 01_{HEX}. Register 07_{HEX} bit AUDIOP is used to set these blocks into power down mode.

◆ DTMF Receiver

For enabling answering machine functions, the chip has an internal DTMF receiver. The receiver is in power down mode after a reset. The DTMFRP bit of register 07_{HEX} controls the receiver power down mode. The receiver has two separate filters for separation of the low and high frequencies. The comparator and logic section measures the low and high frequency periods with an averaging algorithm. When the valid DTMF tone is detected the external steering logic output pin EST is set to high. With an external RC time constant the tone detect time and tone dropout times can be adjusted. The STGT input/output pin has an internal comparator and pull-up and pull-down transistors. When EST is active and STGT goes from below to above the Vref level (VDD/2) the STGT is pulled up with an internal transistor. This causes the STD signal to go high, which causes the XINT line to become active. At the same time the detected DTMF tone is stored in register 04_{HEX}. When the DTMF tone is not present the EST will go low, which causes the STGT to fall. When the STGT falls below the Vref level (VDD/2) the internal logic pulls the input down. The external RC circuit will filter out very short gaps in the received DTMF tone. The interrupt caused by the DTMF detector is cleared by reading status register 10_{HEX}. If the interrupt is cleared but register 04_{HEX} is not read until the next DTMF tone is received, then the previous tone will be lost. The formula below can be used to calculate tone present and tone absent times. By adding diodes to the external circuit the tone present and tone dropout times can be altered. If one of the diodes is removed, the absent and present times are calculated using the parallel combination of R1 and R2.


$$\text{Time} = R*C \ \ln(V_{DD}/V_{REF})$$
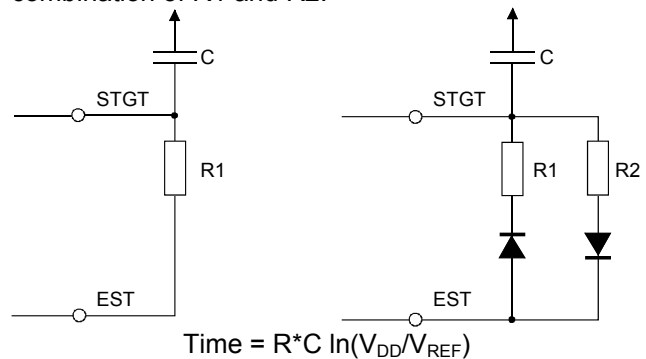
FUNCTIONS

◆ RX Audio

The RX audio block starts with switch S1. The switch is controlled by bit S1 of register $0E_{HEX}$. The input ALP is used for enabling the audio loopback mode. In normal operation RX is used. Behind the switch is amplifier GC1 with adjustable gain from -3dB to +3dB. The gain is controlled with bits 0..3 in register $0E_{HEX}$. The amplifier output is connected to the second order lowpass filter F1. The cutoff frequency of the filter is 50 kHz and the gain at 1kHz is 0dB. The filter output is connected to data comparator C1 and to the SAT bandpass filter F2 and to the rest of the RX audio block. The polarity of the received data can be inverted with bit INVRX, which is located in register 13_{HEX}. The data comparator output is connected to the DPLL and Manchester decoder blocks. The filter F2 is a 6kHz bandpass filter for supervisory audio tone. The filter is a second order SC filter. The filter output is connected to SAT comparator C2 and the SAT detection block.

The signal from F1 is connected to filter F3 through a switch which is used by the internal logic when the AUMUT bit of register 13_{HEX} is active. In this case if the data is received on the voice channel the lowpass filter F3 input is grounded automatically with this switch. With switches S6 and S7 the received audio and transmitted audio can be summed. The control bits of the switches are located in register 03_{HEX}. This signal is fed to F4 and to the DTMF receiver. The function of the DTMF receiver is described in the next section RX de-emphasis filter F4 has a -6dB/octave (±1dB) frequency response in the range 300Hz ... 3kHz. The filter can be bypassed with S2-RXTST0-RXTST1. Switch S2-RXTST0-RXTST1 is connected to the DEOUT pin. The performance of C1, C2 and F2 can be monitored with switch S2-RXTST0-RXTST1. Bits 5 and 6 in register 02_{HEX} and bit 5 in register $0E_{HEX}$ control this switch. An external capacitor is needed between DEOUT and RBPFIN. The RBPFIN input is connected to filter F5, which is a 6th order bandpass filter. The gain of this filter is 0dB at 1kHz. The filter can be bypassed with switch S4. After S4 the signal is connected to the RBPFOUT pin. An external capacitor is used to connect the signal to the EXPIN input.
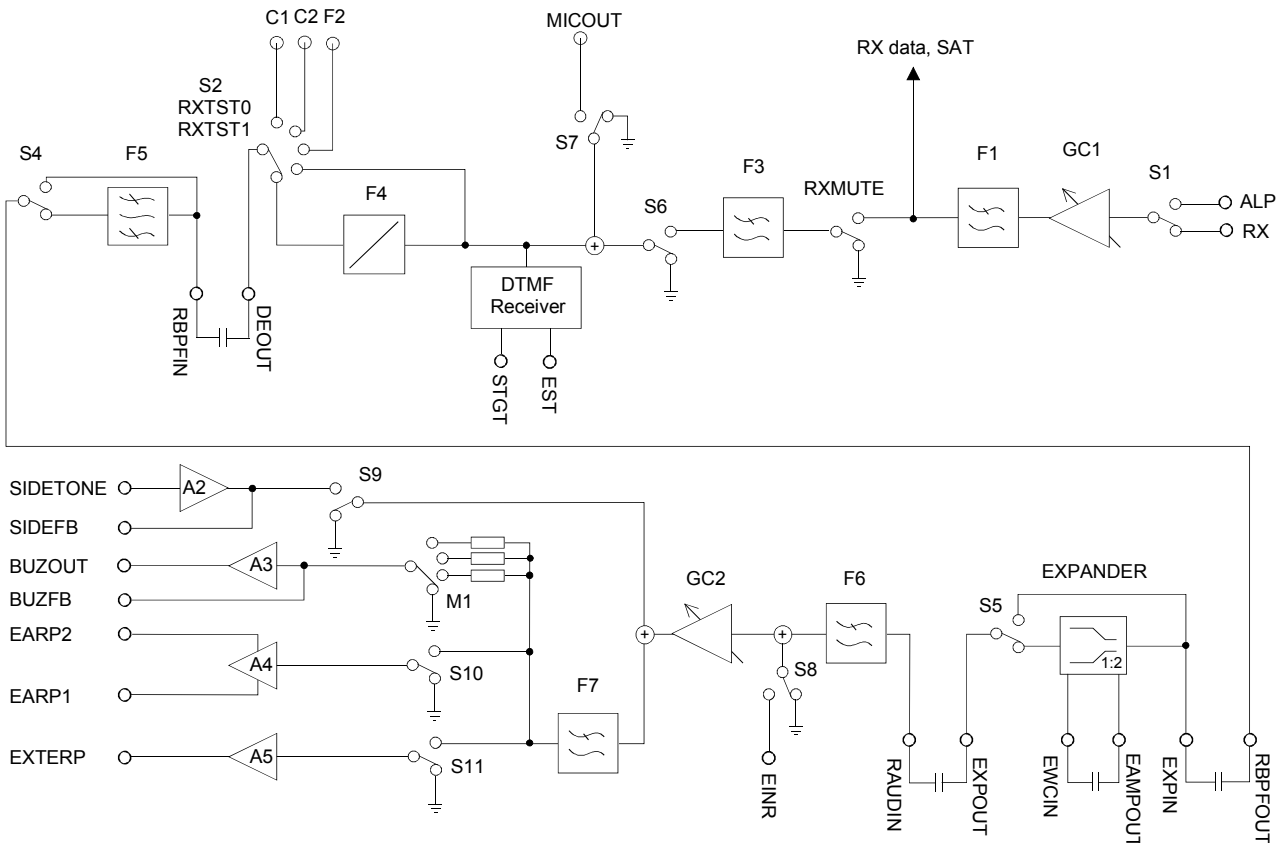
Audio Receive Path

FUNCTIONS

The signal is fed to the SC-type audio expander with expansion ratio 1:2. The expander can also be bypassed with switch S5. The switch is controlled with bit S5 in register 03_{HEX}. After switch S5 the signal goes to the EXPOUT output pin. An external capacitor is used to connect the signal to the RAUDIN input and to filter F6. Filter F6 is a 4th order SC-type lowpass filter. The gain at 1kHz is 0dB. After filtering the signal and the external accessory input EINR can be summed with switch S8. The control bit for the switch is in register 03_{HEX}. The summed signal is amplified with GC2, which has a -15dB...+15dB gain with 16 steps. The gain is controlled with bits 0..3 in register 03_{HEX}. The amplified signal can be summed with SIDETONE. The side tone can be switched on with S9, which has a control bit in register 02_{HEX}. The side tone input has an internal Op Amp with feedback signal SIDEFB. The gain of the Op Amp is controlled by external components. COMPIN is normally used as an input for the side tone amplifier circuit.

Filter F7 is a second order low pass filter. The cutoff frequency is 20kHz and the gain at 1kHz is 0dB.

After filtering the signal can be connected to three amplifiers with switches M1, S10 and S11. The control bits are located in registers 02_{HEX} and 03_{HEX}. A4 is the earphone amplifier, which is a single input differential output amplifier. Amplifier A5 is for external accessories and is capable of driving a capacitive load. The load capacitance is 1nF and the block has a 4.82dB gain. The third amplifier A3 is a buzzer driver. It drives the signal to the power transistor, which drives the buzzer. The buzzer represents a high inductive load of 1.2mH/25ohm. The block stabilizes the current flow through the external buzzer which depends on the current gain factor of the external bipolar transistor. The emitter resistor of the transistor must be 6.8 ohms. Three current values (peak values) can be chosen with switch M1:10mA, 66mA and 160mA. The tolerance of the external resistor will directly affect the buzzer current. The RX audio block can be set into power down mode together with the TX audio block. The AUDIOP bit in Register 07_{HEX} is used for this purpose. The blocks are in power down mode after a reset.
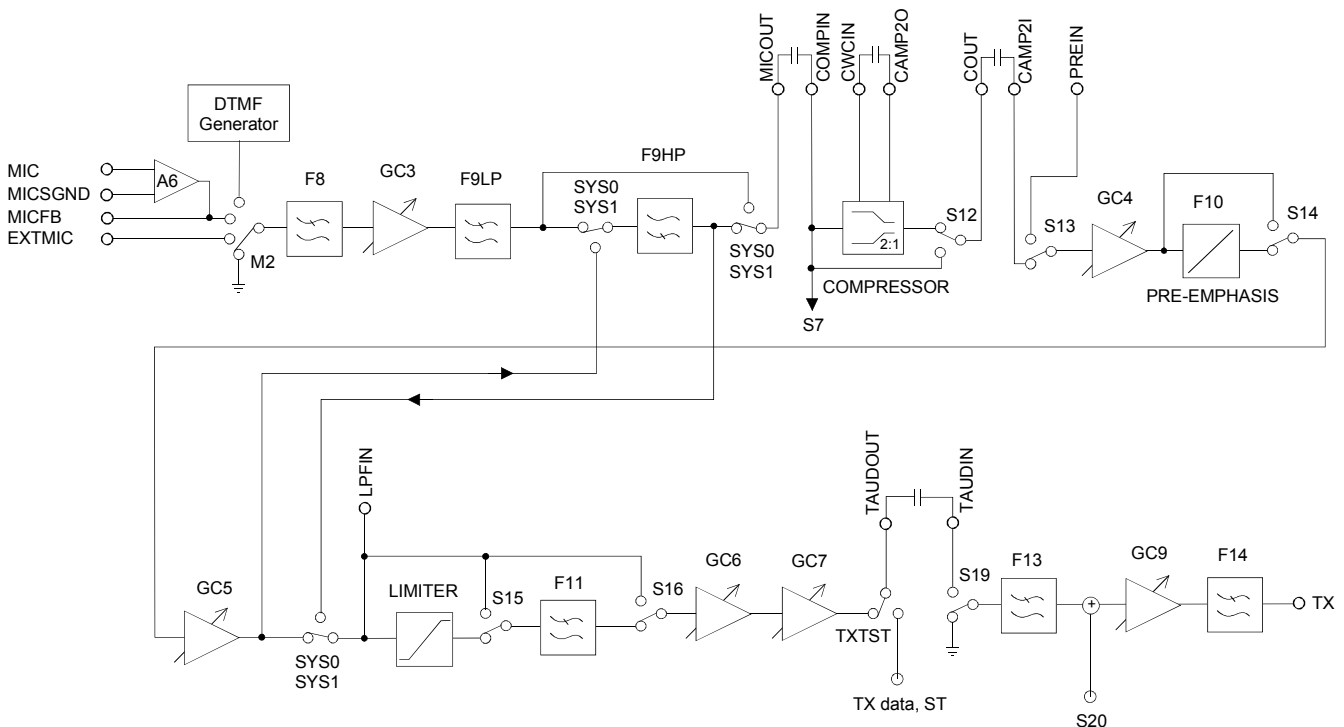
FUNCTION

◆ TX Audio

The TX audio block is in the power down mode after a reset. The block is set to the operation mode with the AUDIOP bit of register 07_{HEX}. The same bit also controls the RX audio block. The TX audio block starts with switch M2, which is controlled by bits 4 and 5 in register 00_{HEX}. Switch M2 connects one of the following blocks as an input source: 1) After a reset the input source is connected to signal ground. 2) In the second position the input is connected to the microphone amplifier A6. The gain of amplifier A6 is determined with external components. The maximum gain is 30 dB. 3) In the third position the input is connected to EXTMIC, which is for external accessories. 4) The fourth position selects the DTMF generator. The DTMF generator is controlled with registers 05_{HEX} and 06_{HEX}. Register 05_{HEX} controls the low frequencies and register 06_{HEX} controls the high frequencies. A detailed description of how to use these registers is in the REGISTERS section. The DTMF generator is in the power down mode after a reset and can be set up with the DTMFTP bit of register 07_{HEX}.

The signal is then filtered with anti-aliasing filter F8. The gain at 1kHz is 0dB and the cutoff frequency is 15kHz. After the filter the signal is amplified with GC3. The gain is -3dB...+3dB with 16 steps according to bits 0..3 in register 00_{HEX}. The amplified signal is then fed to lowpass filter F9LP and highpass filter F9HP, which are 4th order SC filters. During normal operation the output of filter F9HP is connected to output MICOUT. With switch SYS0-SYS1 the highpass filter can be transferred to the output of GC5 after the signal has been compressed and pre-emphasized. Bit 6 in register 12_{HEX} and bit 6 in register 14_{HEX} control switch SYS0-SYS1. Connect MICOUT through a 22nF capacitor to the compressor input COMPIN. The MICOUT can also be used as a source for the side tone amplifier and for detecting the audio level with the uncommitted Op Amp (See APPLICATIONS section). The compressor is an SC audio type with a 2:1 compressing ratio. The detailed values are found in the ELECTRICAL CHARACTERISTICS section under Compressor. The compressor can be bypassed internally with switch S12 or externally with S13. The bypass gain is 0dB (100 mV_{rms}). The compressor requires one external 22nF capacitor between pins CAMP2O and CWCIN. Another 22nF capacitor is needed between pins CAMP2IN and COUT. This capacitor also serves as an external DC blocking capacitor between the compressor output and gain control GC4 input.

Audio Transmit Path

FUNCTIONS

The gain of GC4 can be adjusted in the range -0.67..+5.33dB with bits 0..3 in register $0A_{HEX}$. After GC4 the signal is filtered with pre-emphasis filter F10, which has a +6dB/octave (±1dB) frequency response at the range 300Hz..3kHz. At 1kHz the gain is 0dB. The pre-emphasis filter can be bypassed with switch S14.The signal is then amplified with GC5. Gain control GC5 is an SC-type with a programmable gain adjustment. The range is 0dB..-20 dB with 16 steps according to bits 0..3 in register $0A_{HEX}$.

At the output of GC5 is output pin LPFIN (or highpass filter F9HP) and a SC-type limiter. The limiting level is $439mV_p$ and the tolerance is ±5%. The 0dB level is $370mV_p$. The limiter can be bypassed with switch S15. The lowpass filter F11 with a 6kHz notch follows the limiter. The gain of the filter is 2.94dB at 1kHz. The filter and the limiter can be bypassed with switch S16. GC6 and GC7 are continuous time programmable gain adjustment blocks. The gain of GC6 is -3dB ... +3dB with 16 step according to bits 0..3 in register $0B_{HEX}$. The gain of GC7 is adjustable within - 3dB ... +1dB with bits 0..3 in register $0B_{HEX}$ in 16 steps.

GC7 output is connected to pin TAUDOUT through switch TXTST. The data transmission signal can be examined at TAUDOUT with this switch. Also with switch TXTST, the performance of GC8, 3.75..3.75dB., F12 and F15 can be observed with an input at TAUDIN. An external capacitor between pins TADOUT and TAUDIN is required. The TAUDIN input is connected to switch S19. The switch can be used to mute the TX audio block. S19 is controlled with bit 5 in register 01_{HEX}. Switch S19 is also controlled by the TX framing block. During data transmission on the voice channel and with the AUMUT bit in register 13_{HEX} set to high the TX audio block is muted with S19. Following S19 is a second order lowpass filter F13 with 15kHz cutoff frequency. After filtering the signal is summed with the data signal and amplified with GC9. The gain of the amplifier GC9 is adjustable with bits 0..3 located in register $0C_{HEX}$. The adjustment is done in 16 steps in the range -3.0.. +3.0dB .The output of the amplifier GC9 is then filtered with F14. The filter is a third order lowpass filter with 54kHz cutoff frequency. The gain at 1kHz is 0dB.

DTX bit of the regiter $0D_{HEX}$ is used to set DATA, DSAT and DST deviation. When the device is not in DTX (Discontinous Transmission) the DTX = 0 and there is nominal level at TX, 93 mV_{rms}. If DTX is on, the level is increased to 373 mV_{rms}.

FUNCTIONS

◆ DACs

The device has three 8-bit DACs. The DACs can be set to the power down mode by using bits XPDDAC1, XPDDAC2 and XPDDAC3. The DACs are in power down mode after a reset. The Vref for the DACs is VDD/2. The output values of the DACs are entered in 8-bit two's complement form into registers 16_{HEX}, 17_{HEX} and 18_{HEX}. The typical step size is 13 mV and the DC output level is in the range 0.3V..VDD-0.3V. The differential nonlinearity is ±0.5 LSB and the integral ±2LSB. The settling time is 10ms (max). The minimum load resistance is 30k and the maximum load capacitance is 80pF.

◆ Op Amps

There are two uncommitted inverting operational amplifiers in the device. The input pins are RXACCIN and TXACCIN. The output pins are RXACCOUT and TXACCOUT. The Op Amps are capable of driving capacitive loads up to 1nF.

◆ Serial Interface

The serial interface has three inputs: SCL (serial clock), STB (strobe) and SRxD(received data). Output pin STxD is used for transmitting data. The data is latched with the rising edge of the SCL signal. The MSB is received first and the LSB last. Before the STB signal, eight address bits must first be shifted in. The STB signal sets the device into the data mode. The MSB of the address byte defines the read/write operation. If the MSB is high the data is read from the device. If the MSB is low, the data is written to the device. After the STB the written data is shifted in with the rising edge of the SCL. If the data is to be read from the device, the STxD output is in the state of MSB data bit after the STB signal. The falling edge of the SCL shifts the next data bit to the STxD output. Eight data bits must be shifted out at which time the device exits the data mode. Because the serial interface transmit buffer is dynamic, data will be valid on the buffer only 200 uS after the STB signal appears. This means that the SCL frequency must be at least 5kHz.
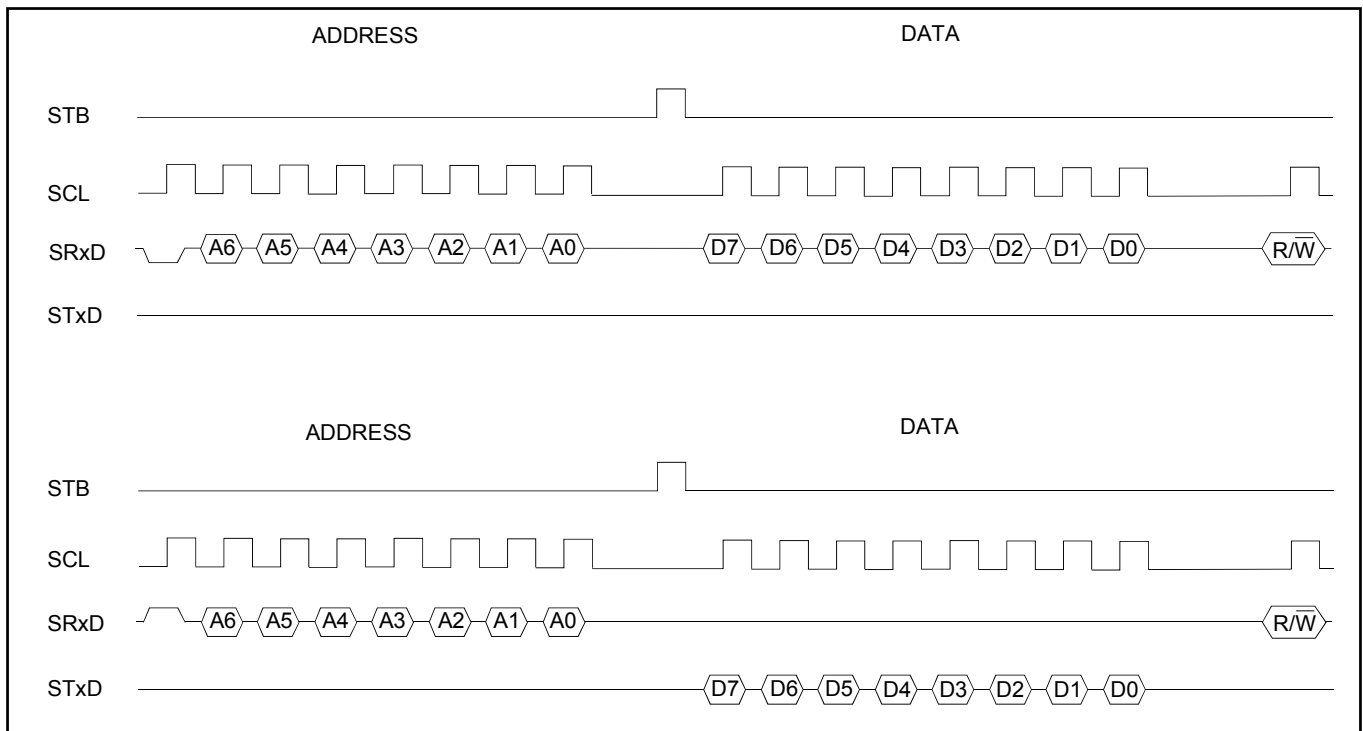
FUNCTIONS

◆ Registers

Address	I/O	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00$_{HEX}$	Write	0	0	M2[1:0]		GC3[3:0]			
01$_{HEX}$	Write	0	S20	S19	S16	S15	S14	S13	S12
02$_{HEX}$	Write	0	RXTST[1:0]		S9	S11	S10	M1[1:0]	
03$_{HEX}$	Write	S8	S7	S6	S5	GC2[3:0]			
04$_{HEX}$	Write	0	Vref[2:0]			0	0	0	0
(84$_{HEX}$)	Read	X	X	X	X	DTMF[3:0]			
05$_{HEX}$	Write	0	0	LOWF[5:0]					
06$_{HEX}$	Write	HIGHF[7:0]							
07$_{HEX}$	Write	XPDDAC3	XPDDAC2	XPDDAC1	RXSIP	TXSIP	AUDIOP	DTMFRP	DTMFTP
0A$_{HEX}$	Write	GC4[3:0]				GC5[3:0[			
0B$_{HEX}$	Write	GC7[3:0]				GC6[3:0]			
0C$_{HEX}$	Write	0	0	0	TXTST	GC9[3:0]			
0D$_{HEX}$	Write	0	S18	S17	DTX	GC8[3:0]			
0E$_{HEX}$	Write	S4	S3	S2	S1	GC1[3:0]			
10$_{HEX}$ (90$_{HEX}$)	Read	X	X		SATINT	TXCOL	TXWRD	RXWRD	STD
11$_{HEX}$ (11$_{HEX}$)	Read	X	BCHERR	BUSY	TXON	WSYNC	DOT	SATDET	X
12$_{HEX}$	Write	SATEN	SYS0	STR	RXRST	TXRST	TXCTRE	CTCV	STON
13$_{HEX}$	Write	SATINTE	STDE	RXINTE	AUMUT	INVRX	INVTX	DCC[1:0]	
14$_{HEX}$	Write	NOMSAT	SYS1	0	0	0	0	SCC[1:0]	
15$_{HEX}$ (95$_{HEX}$) AMPS	Read	1$_{ST}$ RX[0:7]							
		2$_{ND}$ RX[8:15]							
		3$_{RD}$ RX[16:23]							
		4$_{TH}$ RX[24:27]				0	0	0	0
15$_{HEX}$ (95$_{HEX}$) NAMPS	Read	8 bits of captured data after comparator with shift register clocked at 400Hz							
16$_{HEX}$	Write	DAC1[7:0]							
17$_{HEX}$	Write	DAC2[7:0]							
18$_{HEX}$	Write	DAC3[7:0]							
19$_{HEX}$ AMPS	Write	1$_{ST}$ TX[0:7]							
		2$_{ND}$ TX[8:15]							
		3$_{RD}$ TX[16:23]							
		4$_{TH}$ TX[24:31]							
		5$_{TH}$ TX[32:35]				0	0	0	0
19$_{HEX}$ NAMPS	Write	8 bit sequence to be transmitted with shift register clocked at 200Hz							

FUNCTIONS

Register 00_HEX (write only)				
Bit	**Name**	**State**	**Function**	
3-0	GC3[3:0]	0000-1111	Control range for GC3: -3.0dB … +3.0dB, 0.4dB/step	
		0000	-3.0dB	
		0001	-2.6dB	
		0010	-2.2dB	
		…….		
		1111	+3.0dB	
		1000	+0.2dB default value	
5-4	M2[1:0]	00	AGND	Connected to F8 input
		01	A6-OUT	
		10	EXTMIC	
		11	DTMFGEN	
6	reserved	0	reserved for future use, set to 0	
7	reserved	0	reserved for future use, set to 0	

Register 01_HEX (write only)				
Bit	**Name**	**State**	**Function**	
0	S12	0	Compressor output	connected to COUT
		1	Compressor input	
1	S13	0	COUT	connected to GC4 input
		1	PREIN	
2	S14	0	F10 output	connected to GC5 input
		1	F10 input	
3	S15	0	Limiter output	connected to F11 input
		1	Limiter input	
4	S16	0	F11 output	connected to GC6 input
		1	Limiter input	
5	S19	0	AGND	connected to F13 input
		1	TAUDIN	
6	S20	0 (SYS1 = 0)	AGND	summed to GC9 input
		1 (SYS1 = 1)	F12 output	
		0 (SYS1 = 0)	AGND	
		1 (SYS1 = 1)	F15 output	
7	reserved	0	reserved for future use, set to 0	

FUNCTIONS

Register 02$_{HEX}$ (write only)

Bit	Name	State	Function	
1-0	M1[1:0]	00	AGND	connected to amplifier A3 input
		01	10mA gain	
		10	66mA gain	
		11	160mA gain	
2	S10	0	AGND	connected to amplifier A4 input
		1	Filter F7 output	
3	S11	0	AGND	connected to amplifier A5 input
		1	Filter F7 output	
4	S9	0	AGND	summed to F7 input
		1	Amplifier A2 output	
6-5	RXTST0-RXTST1	00	determined by S2	connected to DEOUT
		01	C1	
		10	F2	
		11	C2	
7	reserved	0	reserved for future use, set to 0	

Register 03$_{HEX}$ (write only)

Bit	Name	State	Function	
3-0	GC2[3:0]	0000-1111	Control range for GC2: -15.0dB … +15.0dB, 2.0dB/step	
		0000	-15.0dB	
		0001	-13.0dB	
		0010	-11.0dB	
		…….		
		1111	+15.0dB	
		1000	+1.0dB default value	
4	S5	0	EXPOUT	connected to EXPOUT
		1	EXPIN	
5	S6	0	AGND	summed into F6 input
		1	RAUDIN	
6	S7	0	AGND	
		1	COMPIN	
7	S8	0	AGND	summed into GC2 input
		1	EINR	

FUNCTIONS

Register 04$_{HEX}$ (bits 7-4 write only, bits 3-0 read only)

Bit	Name	State	Function
3-0	DTMF[3:0]	0001	'1' Tone detected
		0010	'2' Tone detected
		0011	'3' Tone detected
		0100	'4' Tone detected
		0101	'5' Tone detected
		0110	'6' Tone detected
		0111	'7' Tone detected
		1000	'8' Tone detected
		1001	'9' Tone detected
		1010	'0' Tone detected
		1011	'*' Tone detected
		1100	'#' Tone detected
		1101	'A' Tone detected
		1110	'B' Tone detected
		1111	'C' Tone detected
		0000	'D' Tone detected
6-4	Vref[2:0]	Internal reference voltage adjustment	
		000	+0.75dB
		001	+0.50dB
		010	+0.25dB
		011	0.00dB default value
		100	-0.25dB
		101	-0.50dB
		110	-0.75dB
		111	-1.00dB
7	reserved	0	reserved for future use, set to 0

Register 05$_{HEX}$ (write only)

Bit	Name	State	Function	
5-0	LOWF[5:0]	00H-3FH	Transmitted low frequency DTMF tone	
			Nominal	Real frequency
		000000	No signal	No signal
		100110	697 Hz	695.8 Hz
		101010	770 Hz	769.0 Hz
		101111	852 Hz	860.6 Hz
		110011	941 Hz	933.8 Hz
7-6	reserved	00	reserved for future use, set to 0	

The register value for other frequencies may be calculated with the formula: $LG[5:0] = (f_{OUT} * 2^{17}) / 2.4MHz$.

FUNCTIONS

Register 06$_{HEX}$ (write only)

Bit	Name	State	Function	
7-0	HIGHF[7:0]	00H-FFH	Transmitted high frequency DTMF tone	
			Nominal	Real frequency
		00000000	No signal	No signal
		01000010	1209 Hz	1208.5 Hz
		01001001	1336 Hz	1336.7 Hz
		01010001	1477 Hz	1483.2 Hz
		01011001	1633 Hz	1629.6 Hz

The register value for other frequencies may be calculated with the formula: $HG[7:0] = (f_{OUT} * 2^{17}) / 2.4MHz$.

Register 07$_{HEX}$ (write only)

Bit	Name	State	Function
0	DTMFTP	0	DTMF transmitter in power down
		1	DTMF transmitter active
1	DTMFRP	0	DTMF receiver in power down
		1	DTMF receiver active
2	AUDIOP	0	AUDIO in power down
		1	AUDIO active
3	TXSIP	0	Digital TX section in power down
		1	Digital TX section active
4	RXSIP	0	Digital RX section in power down
		1	Digital RX section active
5	XPDDAC1	0	DAC1 in power down
		1	DAC1 active
6	XPDDAC2	0	DAC2 in power down
		1	DAC2 active
7	XPDDAC3	0	DAC3 in power down
		1	DAC3 active

FUNCTIONS

Register 0A_{HEX} (write only)			
Bit	**Name**	**State**	**Function**
3-0	GC5[3:0]	0000-1111	Control range for GC5: 0.0dB … -20.0dB, 1.33.0dB/step
		0000	0.0dB
		0001	-1.33dB
		0010	-2.67dB
		…….	
		1111	-20.0dB
		0000	0.0dB default value
7-4	GC4[3:0]	0000-1111	Control range for GC4: -0.67dB … +5.33dB, 0.4.0dB/step
		0000	-0.67dB
		0001	-0.27dB
		0010	+0.13dB
		…….	
		1111	+5.33dB
		1000	+2.53dB default value

Register 0B_{HEX} (write only)			
Bit	**Name**	**State**	**Function**
3-0	GC6[3:0]	0000-1111	Control range for GC6: -3.0dB … +3.0dB, 0.4dB/step
		0000	-3.0dB
		0001	-2.6dB
		0010	-2.2dB
		…….	
		1111	+3.0dB
		1000	+0.2dB default value
7-4	GC7[3:0]	0000-1111	Control range for GC7: -3.0dB … +1.0dB, 0.266.0dB/step
		0000	-3.0dB
		0001	-2.6dB
		0010	-2.2dB
		…….	
		1111	+1.0dB
		1011	-0.067dB default value

FUNCTIONS

Register 0C$_{HEX}$ (write only)			
Bit	Name	State	Function
3-0	GC9[3:0]	0000-1111	Control range for GC9: -3.0dB … +3.0dB, 0.4dB/step
		0000	-3.0dB
		0001	-2.6dB
		0010	-2.2dB
		…….	
		1111	+3.0dB
		1000	+0.2dB default value
4	TXTST	0	GC7 output connected to TAUDOUT ST, SAT and TXDATA connected to GC8 input
		1	ST, SAT and TXDATA connected to TAUDOUT TAUDIN connected to GC8 input
7-5	reserved	000	reserved for future use, set to 0

Register 0D$_{HEX}$ (write only)				
Bit	Name	State	Function	
3-0	GC8[3:0]	0000-1111	Control range for GC8: -3.75dB … +3.75dB, 0.5dB/step	
		0000	-3.75dB	
		0001	-3.25dB	
		0010	-2.75dB	
		…….		
		1111	+3.75dB	
		1000	+0.25dB default value	
4	DTX	0	Discontinuous transmission disabled	
		1	Discontinuous transmission enabled	
5	S17	0 (SYS1 = 0)	AGND	Summed into GC8 input
		1 (SYS1 = 0)	TXDATA signal	
		0 (SYS1 = 1)	AGND	
		1 (SYS1 = 1)	TX Buffer output signal	
6	S18	0	AGND	
		1	Signaling Tone	
7	reserved	0	reserved for future use, set to 0	

FUNCTIONS

Register 0E_HEX (write only)				
Bit	**Name**	**State**	**Function**	
3-0	GC1[3:0]	0000-1111	Control range for GC1: -3.0dB … +3.0dB, 0.4dB/step	
		0000	-3.0dB	
		0001	-2.6dB	
		0010	-2.2dB	
		…….		
		1111	+3.0dB	
		1000	+0.2dB default value	
4	S1	0	RX	connected to GC1 input
		1	ALP	
5	S2	0	F4 output	connected to DEOUT
		1	F4 input	
6	S3	0	signal from S2-RXTST0-RXTST1	connected to F5 input
		1	RBPFIN	
7	S4	0	F5 output	connected to RBPFOUT
		1	F5 input	

Register 10_HEX (read only)			
Bit	**Name**	**State**	**Function**
0	STD	0	DTMF tone not received
		1	DTMF tone received
1	RXWRD	0	RX buffer empty
		1	RX word received (SYS1 = 0) Next captured byte ready (SYS1 = 1)
2	TXWRD	0	Transmitting previous byte or word
		1	TX buffer empty
3	TXCOL	0	No TX collision detected
		1	TX collision detected
4	SATINT	0	SATDET signal stable
		1	rising or falling edge of SATDET detected
7-5	reserved	0,1	not in use

The rising edge of the signals STD, RXWRD, TXWRD, TXCOL and SATINT activates the interrupt line XINT. If the signal(s) changes when register 10_HEX or one of the other registers is read, the interrupt line will be activated right after the register read. Reading this register sets the interrupt line inactive. If a new interrupt is generated during register read , the interrupt line will be activated again right after register is read.

FUNCTIONS

Register 11$_{HEX}$ (read only)

Bit	Name	State	Function
0	reserved	0,1	not in use
1	SATDET	0	Invalid SAT frequency received
		1	Valid SAT frequency received. See SCC in register 14$_{HEX}$.
2	DOT	0	No dotting sequence detected
		1	Dotting sequence detected
3	WSYNC	0	No word sync detected
		1	Word sync detected
4	TXON	0	No transmission
		1	Word transmission on
5	BUSY	0	BUSY bit detected
		1	IDLE bit detected
6	BCHERR	0	No BCH error detected
		1	BCH error detected
7	reserved	0,1	not in use

Register 12$_{HEX}$ (write only)

Bit	Name	State	Function
0	STON	0	No signaling tone transmission
		1	Signaling transmission on
1	CTCV	0	Control channel
		1	Voice channel
2	TXCTREN	0	TX control disabled
		1	TX control active. TXCTRL output pin can be used to control transmitter
3	TXRST	0	Digital TX section operating
		1	Digital TX section reset
4	RXRST	0	Digital RX section operating
		1	Digital RX section reset
5	STR	0	Stream A
		1	Stream B
6	SYS0	0 (SYS1 = 0)	ETACS mode
		1 (SYS1 = 0)	AMPS mode
		0 (SYS1 = 1)	F9HP input connected to F9LP output. NAMPS mode
		1 (SYS1 = 1)	F9HP input connected to GC5 output. NAMPS mode
7	SATEN	0	SAT transmission disabled
		1	SAT transmission enabled

FUNCTIONS

Register 13_{HEX} **(write only)**			
Bit	**Name**	**State**	**Function**
1-0	DCC[1:0]	00-11	Digital color code
		00	0000000
		01	0011111
		10	1100011
		11	1111100
2	INVTX	0	TXDATA not inverted
		1	Invert TXDATA polarity
3	INVRX	0	RX input not inverted
		1	Invert RX input polarity
4	AUMUT	0	No automatic mute
		1	TX and RX audio muted automatically on the voice channel
5	RINTE	0	RX interrupts disabled
		1	RX interrupts enabled
6	STDE	0	STDE (DTMF receiver) interrupts disabled
		1	STDE (DTMF receiver) interrupts enabled
7	SATINTE	0	SAT detection interrupts disabled
		1	SAT detection interrupts enabled

Register 14_{HEX} **(write only)**			
Bit	**Name**	**State**	**Function**
1-0	SCC[1:0]	00	5958Hz-5982Hz SAT frequency expected
		01	5988Hz-6012Hz SAT frequency expected
		10	6018Hz-6042Hz SAT frequency expected
		11	Invalid state
5-2	reserved	0000	reserved for future use, set to 0
6	SYS1	0	Wide band mode (AMPS/ETACS)
		1	Narrow band mode (NAMPS)
7	NOMSAT	0	Transmitted SAT will follow received SAT
		1	Nominal SAT frequency transmitted

FUNCTIONS

Register 15$_{HEX}$ (read only)

Bit	Name	State	Function							
7-0	RX byte SYS1 = 0	00H-FFH	When RXWRD is high							
			1st byte	b0	b1	b2	b3	b4	b5	b6	b7
			2nd byte	b8	b9	b10	b11	b12	b13	b14	b15
			3rd byte	b16	b17	b18	b19	b20	b21	b22	b23
			4th byte	b24	b25	b26	b27	0	0	0	0
7-0	RX byte SYS1 = 1	00H-FFH	Captured byte with 400Hz after data comparator. MSB = first captured bit.							

The received word is read by reading register 15$_{HEX}$ four times.

Register 16$_{HEX}$ (write only)

Bit	Name	State	Function
7-0	DAC1[7:0]	00H-FFH	Control port for DAC1 output level
		80H	100mV$_{DC}$
		FFH	100mV$_{DC}$ + 7FH x 13mV$_{DC}$
		00H	100mV$_{DC}$ + 80H x 13mV$_{DC}$
		7FH	100mV$_{DC}$ + FFH x 13mV$_{DC}$

Register 17$_{HEX}$ (write only)

Bit	Name	State	Function
7-0	DAC2[7:0]	00H-FFH	Control port for DAC2 output level
		80H	100mV$_{DC}$
		FFH	100mV$_{DC}$ + 7FH x 13mV$_{DC}$
		00H	100mV$_{DC}$ + 80H x 13mV$_{DC}$
		7FH	100mV$_{DC}$ + FFH x 13mV$_{DC}$

Register 18$_{HEX}$ (write only)

Bit	Name	State	Function
7-0	DAC3[7:0]	00H-FFH	Control port for DAC3 output level
		80H	100mV$_{DC}$
		FFH	100mV$_{DC}$ + 7FH x 13mV$_{DC}$
		00H	100mV$_{DC}$ + 80H x 13mV$_{DC}$
		7FH	100mV$_{DC}$ + FFH x 13mV$_{DC}$

FUNCTIONS

| Register 19_{HEX} (write only)											
Bit	**Name**	**State**	**Function**								
7-0	TX byte SYS1 = 0	00H-FFH	When TXWRD is high								
			1st byte	b0	b1	b2	b3	b4	b5	b6	b7
			2nd byte	b8	b9	b10	b11	b12	b13	b14	b15
			3rd byte	b16	b17	b18	b19	b20	b21	b22	b23
			4th byte	b24	b25	b26	b27	b28	b29	b30	b31
			5th byte	b32	b33	b34	b35	0	0	0	0
7-0	TX byte SYS1 = 1	00H-FFH	Byte for transmitter. Byte is shifted out with 200Hz clock. MSB will be transmitted first.								

The transmitted word is written by writing to register 19_{HEX} five times.

APPLICATION INFORMATION
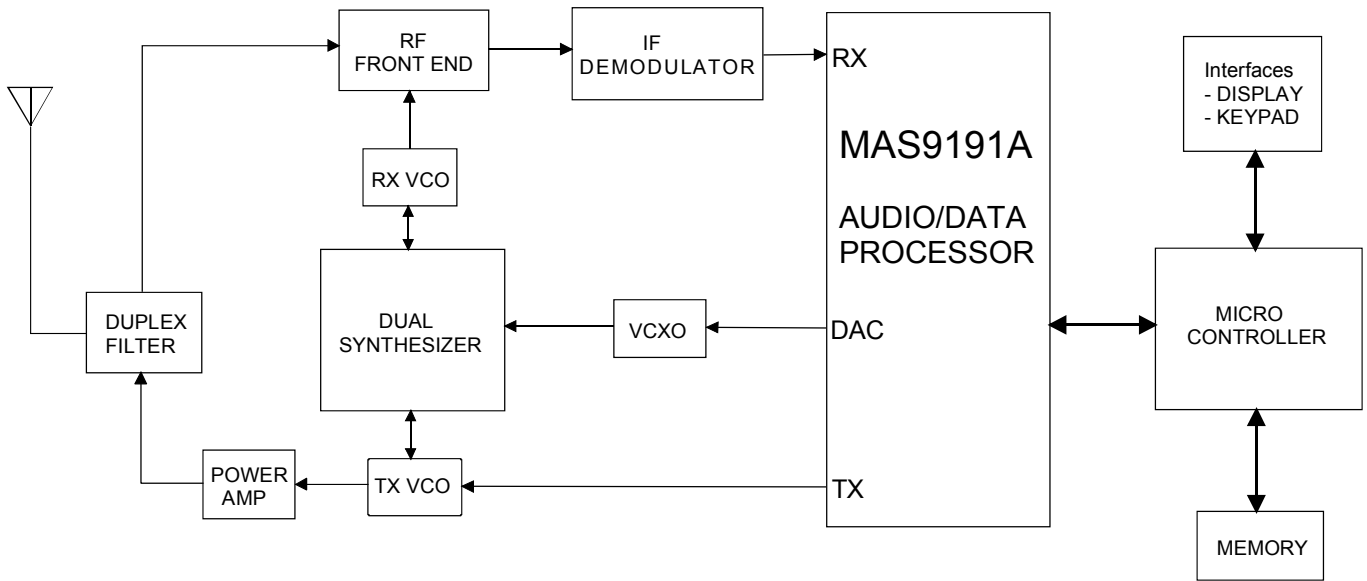
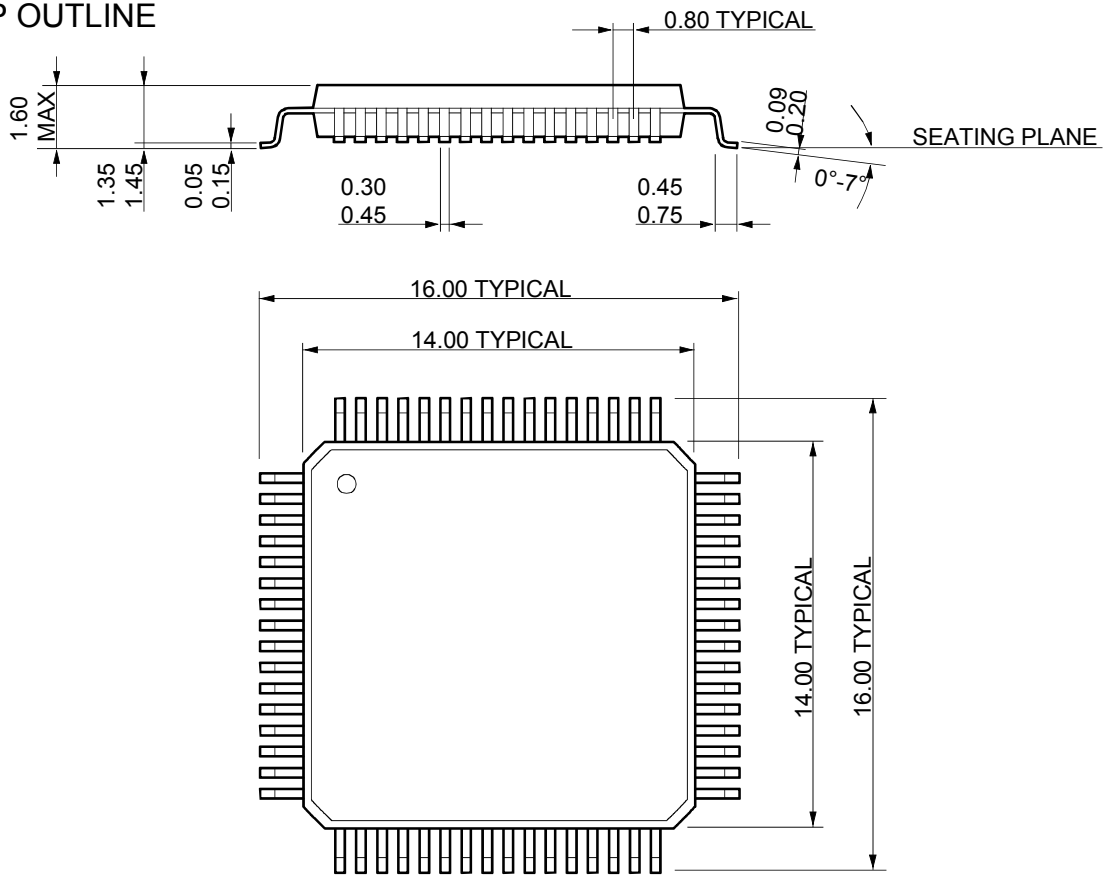Typical MAS9191A application in AMPS/ETACS cellular system.

TEST CIRCUIT
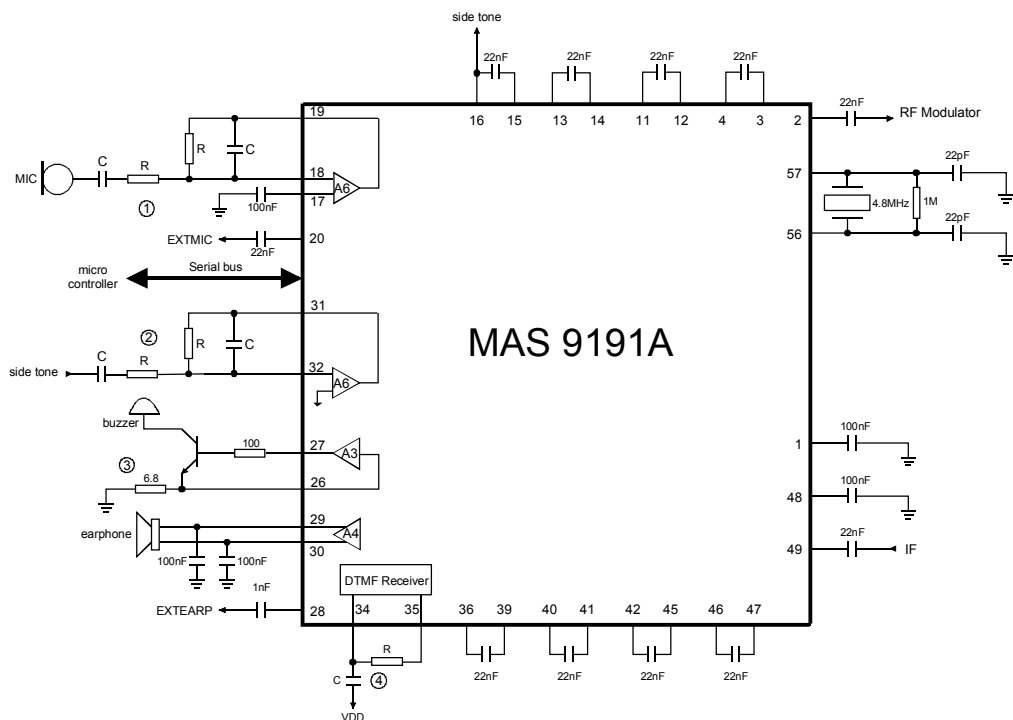
① components determine the gain of microphone amplifier A6

② components determine the gain of SIDETONE amplifier A2

③ NPN transistor for the buzzer

④ components determine RC time constant if DTMF receiver is used

MICRO ANALOG SYSTEMS

PACKAGE OUTLINES

64 LEAD TQFP OUTLINE

0.80 TYPICAL

1.60 MAX

1.35
1.45

0.05
0.15

0.30
0.45

0.45
0.75

0.09
0.20

SEATING PLANE

0°-7°

16.00 TYPICAL

14.00 TYPICAL

14.00 TYPICAL

16.00 TYPICAL

ALL MEASUREMENTS IN mm

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9191AJ	AMPS/ETACS single chip audio/data processor	TQFP64	
MAS9191AJ-T	AMPS/ETACS single chip audio/data processor	TQFP64	Tape and Reel

LOCAL DISTRIBUTOR

MICRO ANALOG SYSTEMS OY CONTACTS

Micro Analog Systems Oy Kamreerintie 2, P.O. Box 51 FIN-02771 Espoo, FINLAND	Tel. +358 9 80 521 Fax +358 9 805 3213 http://www.mas-oy.com

NOTICE

Micro Analog Systems Oy reserves the right to make changes to the products contained in this data sheet in order to improve the design or performance and to supply the best possible products. Micro Analog Systems Oy assumes no responsibility for the use of any circuits shown in this data sheet, conveys no license under any patent or other rights unless otherwise specified in this data sheet, and makes no claim that the circuits are free from patent infringement. Applications for any devices shown in this data sheet are for illustration only and Micro Analog Systems Oy makes no claim or warranty that such applications will be suitable for the use specified without further testing or modification.