

**Amplifier, Power, 14W
1.3-2.5 GHz**

MAAP-000076-PKG001

Rev A
Preliminary Datasheet

Features

- ◆ **14 Watt Saturated Output Power Level**
- ◆ **Variable Drain Voltage (6-10V) Operation**
- ◆ **MSAG Process**

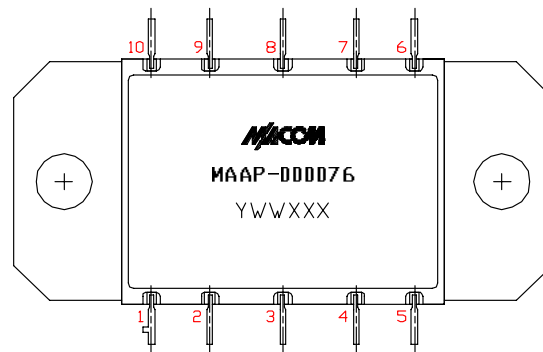
Primary Applications

- ◆ **Radio Communications**
- ◆ **SatCom**

Description

The MAAP-000076-PKG001 is a 2-stage 14W power amplifier with on-chip bias networks in a 10 lead flange-mount ceramic package, allowing easy assembly. The package is hermetic and provides an excellent thermal path. This product is fully matched to 50 ohms on both the input and output. External DC blocking capacitors are not required since they are incorporated into the MMIC design. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG™) Process, each device is 100% RF tested on wafer to ensure performance compliance.



Pin #	Description
1	VGG
2	N/C
3	RF IN
4	N/C
5	VGG
6	VDD
7	N/C
8	RF OUT
9	N/C
10	VDD

Also Available in:

Description	Die on Pedestal	Ceramic Pkg Sample Board	Die Sample Board	Mechanical Sample
Part Number	MAAP-000076-PED000	MAAP-000076-SMB001	MAAP-000076-SMB004	MAAP-000076-MCH000

Electrical Characteristics: $T_C = 45^\circ\text{C}^1$, $Z_0 = 50\ \Omega$, $V_{DD} = 10\text{V}$, $I_{DQ} = 3.8\text{A}^2$, $P_{in} = 22\text{ dBm}$, $R_G = 30\ \Omega$

Parameter	Symbol	Typical	Units
Bandwidth	f	1.3-2.5	GHz
Output Power	P_{OUT}	41.5	dBm
1-dB Compression Point	P_{1dB}	41	dBm
Small Signal Gain	G	25	dB
Power Added Efficiency	PAE	29	%
Input VSWR	VSWR	1.7:1	
Output VSWR	VSWR	1.8:1	
Gate Current, under large signal RF Drive	I_{GG}	<25	mA
Drain Current, under large signal RF Drive	I_{DD}	<5.9	A
Output Third Order Intercept	IP_3	46	dBm
Output Third Order Intermod, $P_{out} = 28\text{ dBm}$ (SCL)	IM_3	38	dBc

1. T_C = Case Temperature
2. Adjust V_{GG} between -2.6 and -1.2V to achieve specified I_{DQ} .

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Visit www.macom.com for additional data sheets and product information.

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Maximum Ratings³

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	27	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	6.1	A
Quiescent DC Power Dissipated (No RF)	P_{DISS}	61.0	W
Junction Temperature	T_J	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions⁴

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	6.0	10	10	V
Gate Voltage	V_{GG}	-2.6	-2.0	-1.2	V
Input Power	P_{IN}		22	25	dBm
Thermal Resistance	Θ_{JC}		2.2		°C/W
Case Temperature	T_C			Note 5	°C

4. Operation outside of these ranges may reduce product reliability.

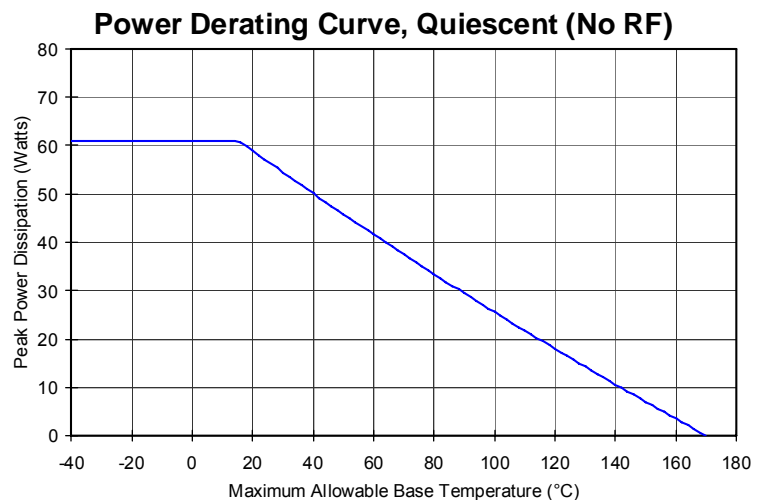
5. Case Temperature = 170°C — $\Theta_{JC} * V_{DD} * I_{DQ}$



Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply $V_{GG} = -2.7$ V, $V_{DD} = 0$ V.
2. Ramp V_{DD} to desired voltage, typically 10.0 V.
3. Adjust V_{GG} to set I_{DQ} , (approximately @ -2.0 V).
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.



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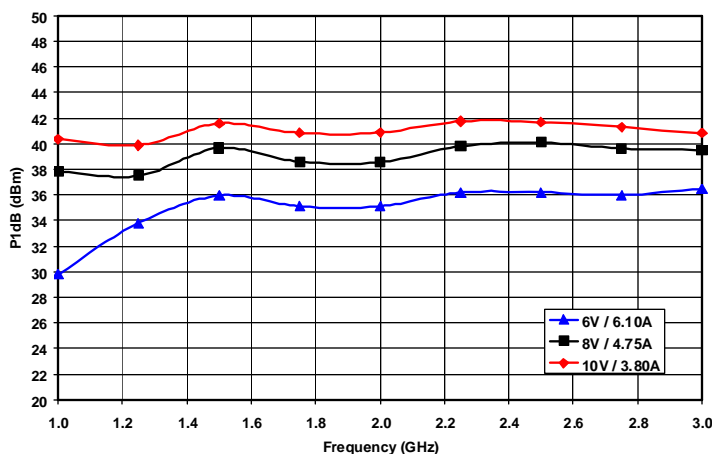


Figure 1. P1dB vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

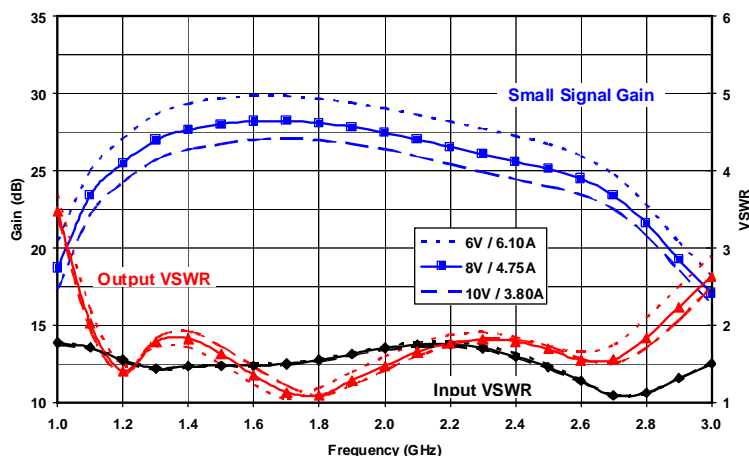


Figure 2. Small Signal Gain and Input & Output VSWR vs. Frequency and Quiescent Bias (Vdd / IDQ)

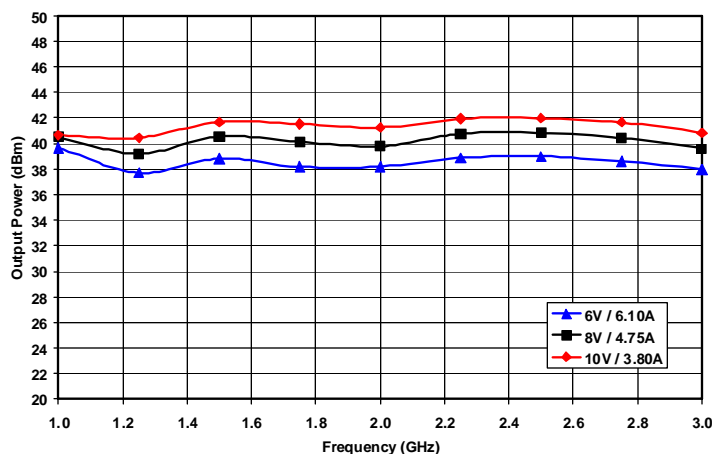


Figure 3. Saturated Output Power vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

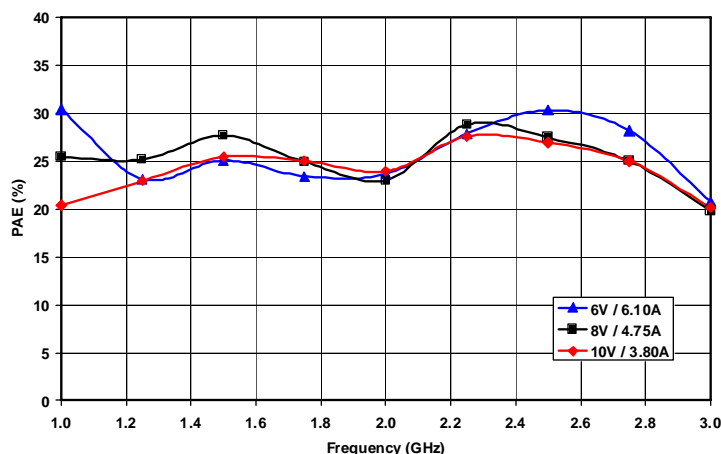


Figure 4. Saturated Power Added Efficiency vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

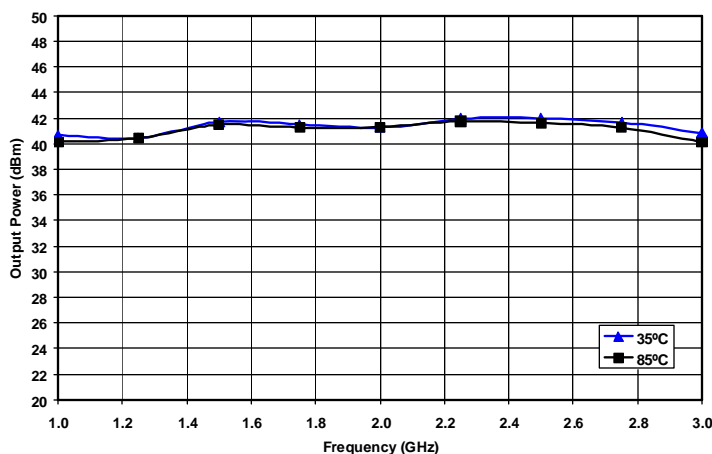


Figure 5. Saturated Output Power vs. Frequency and Case Temperature at VD = 10V and IDQ = 3.80A

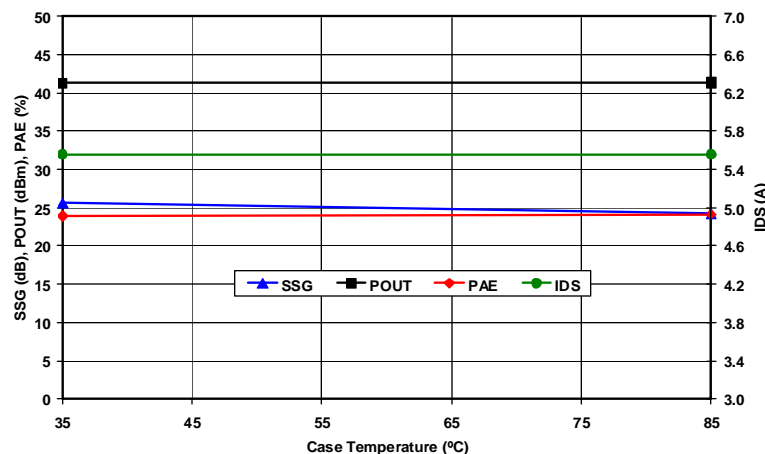


Figure 6. Small Signal Gain & Saturated Output Power, Power Added Efficiency and Drain Current vs. Case Temperature at 2.0 GHz, VD = 10V, and IDQ = 3.80A

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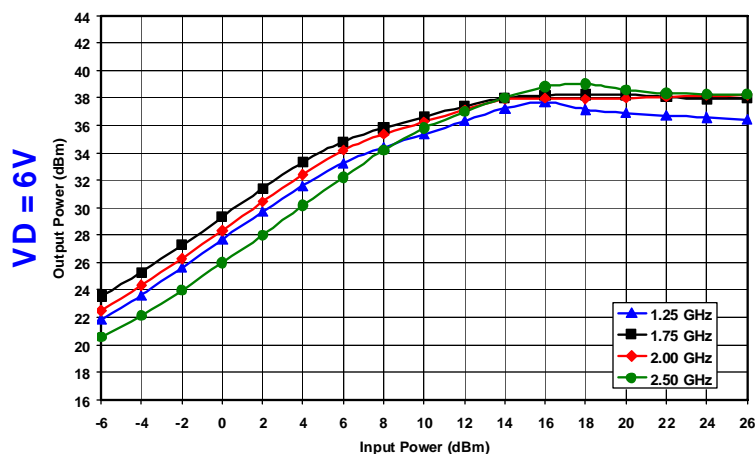


Figure 7. Output Power vs. Input Power and Frequency
at VD = 6V and IDQ = 6.10A

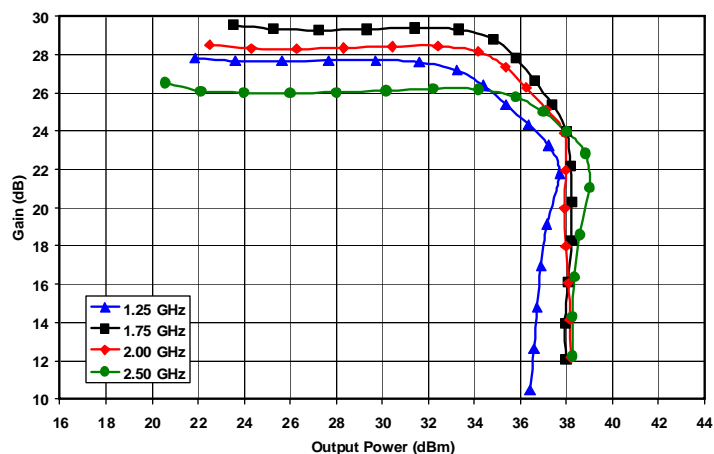


Figure 8. Gain vs. Output Power and Frequency
at VD = 6V and IDQ = 6.10A

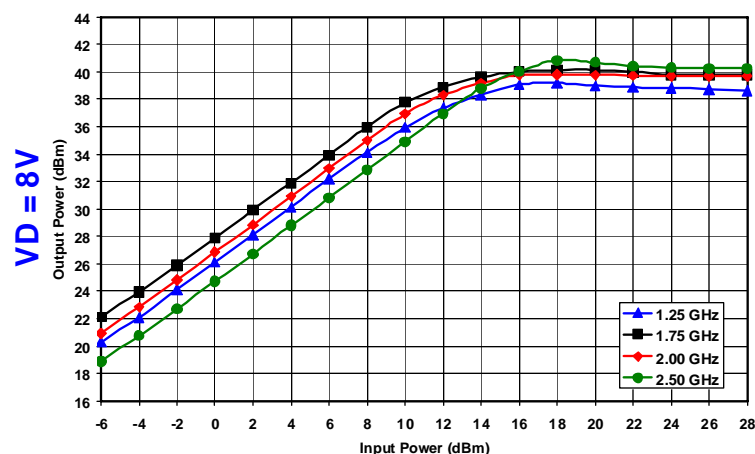


Figure 9. Output Power vs. Input Power and Frequency
at VD = 8V and IDQ = 4.75A

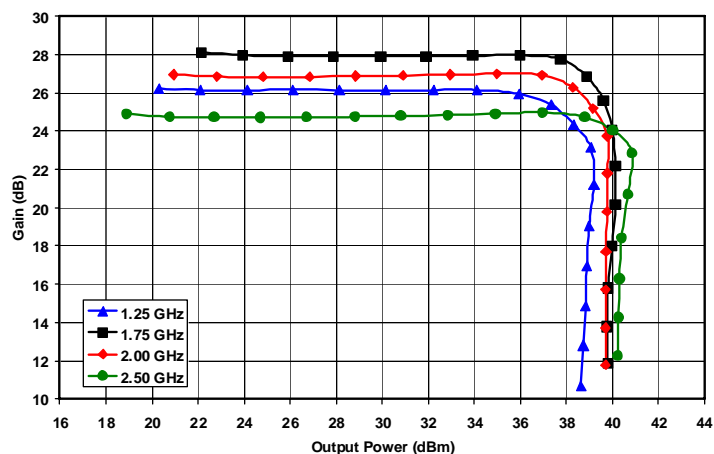


Figure 10. Gain vs. Output Power and Frequency
at VD = 8V and IDQ = 4.75A

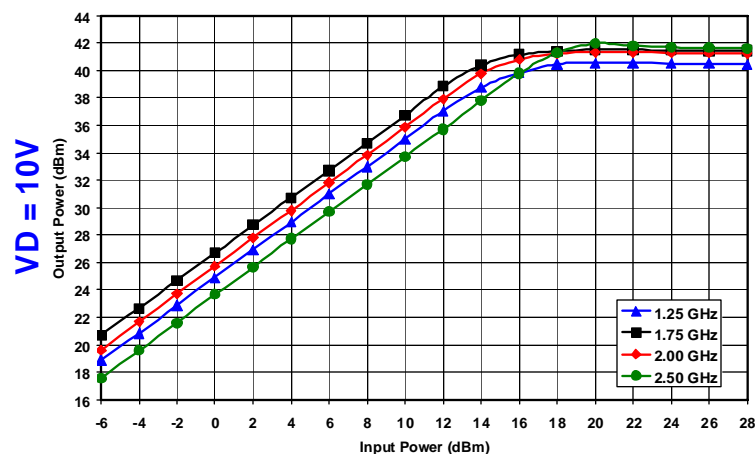


Figure 11. Output Power vs. Input Power and Frequency
at VD = 10V and IDQ = 3.80A

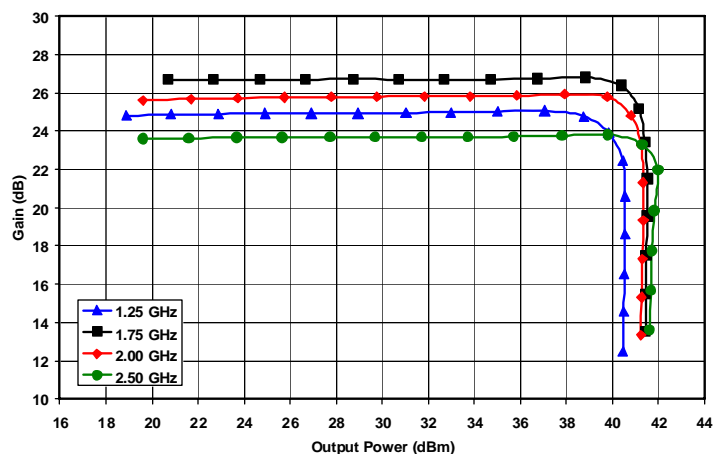


Figure 12. Gain vs. Output Power and Frequency
at VD = 10V and IDQ = 3.80A

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VD = 6V

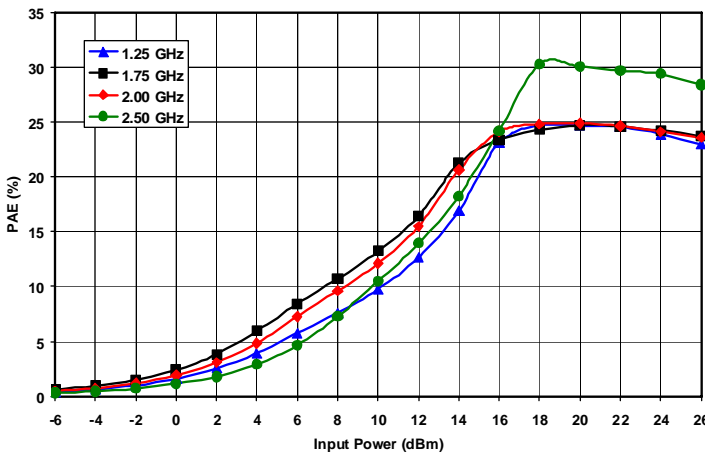


Figure 13. Power Added Efficiency vs. Input Power and Frequency at VD = 6V and IDQ = 6.10A

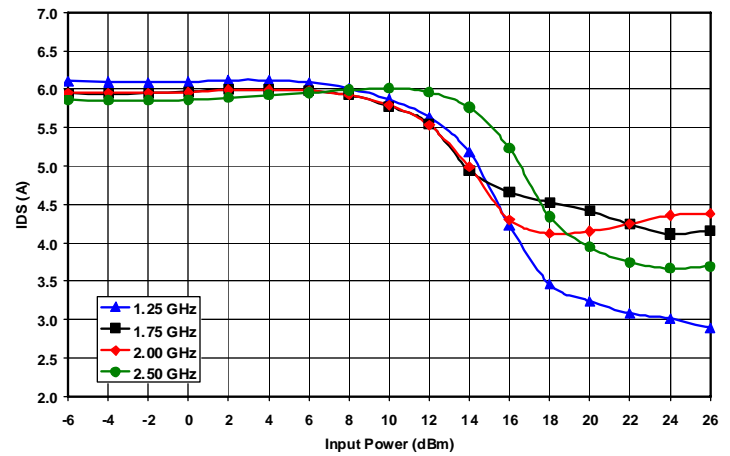


Figure 14. Drain Current vs. Input Power and Frequency at VD = 6V and IDQ = 6.10A

VD = 8V

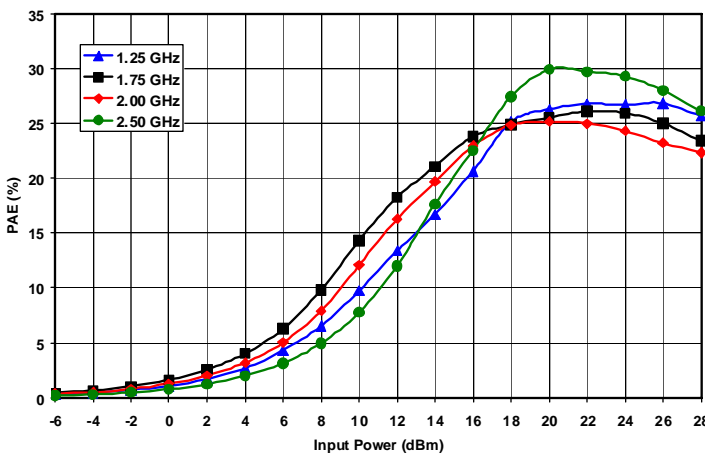


Figure 15. Power Added Efficiency vs. Input Power and Frequency at VD = 8V and IDQ = 4.75A

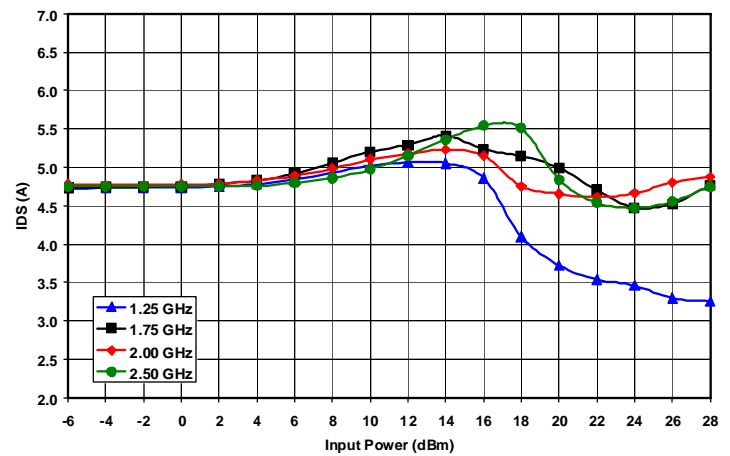


Figure 16. Drain Current vs. Input Power and Frequency at VD = 8V and IDQ = 4.75A

VD = 10V

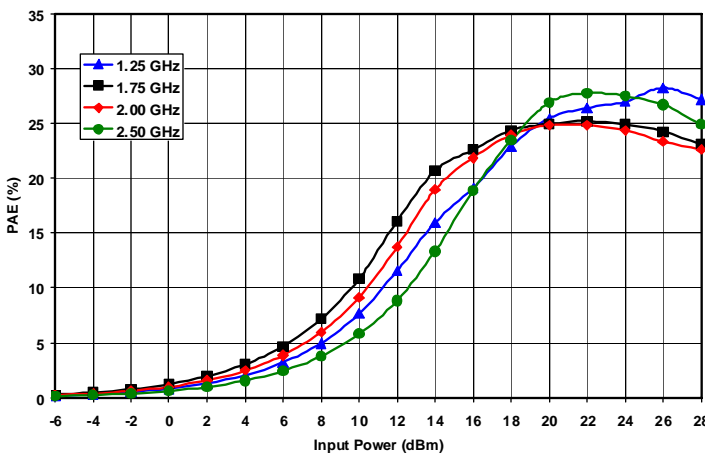


Figure 17. Power Added Efficiency vs. Input Power and Frequency at VD = 10V and IDQ = 3.80A

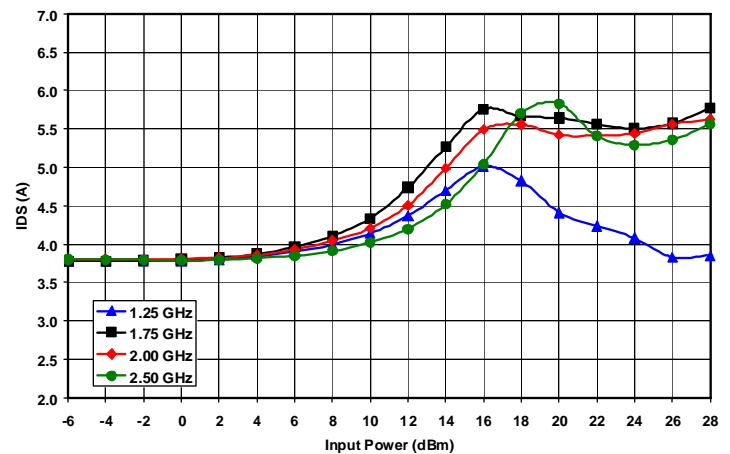


Figure 18. Drain Current vs. Input Power and Frequency at VD = 10V and IDQ = 3.80A

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VD = 6V

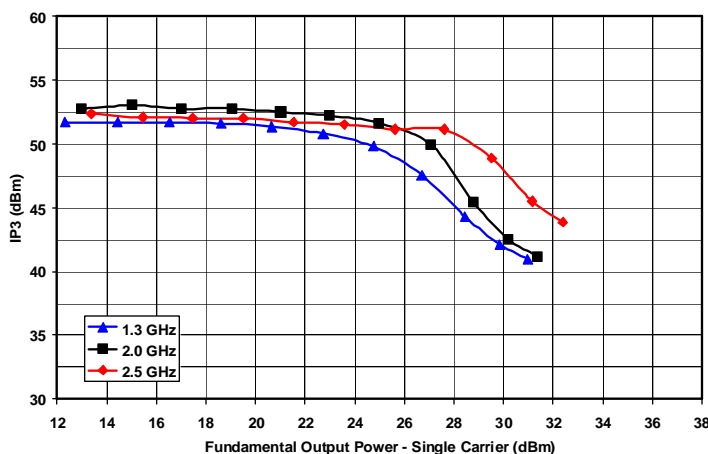


Figure 19. Third Order Intercept vs. Output Power and Frequency at VD = 6V and IDQ = 6.10A

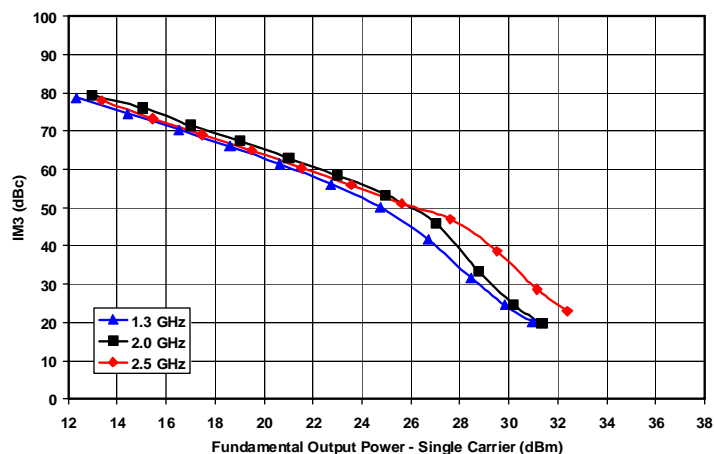


Figure 20. Third Order Intermod vs. Output Power and Frequency at VD = 6V and IDQ = 6.10A

VD = 8V

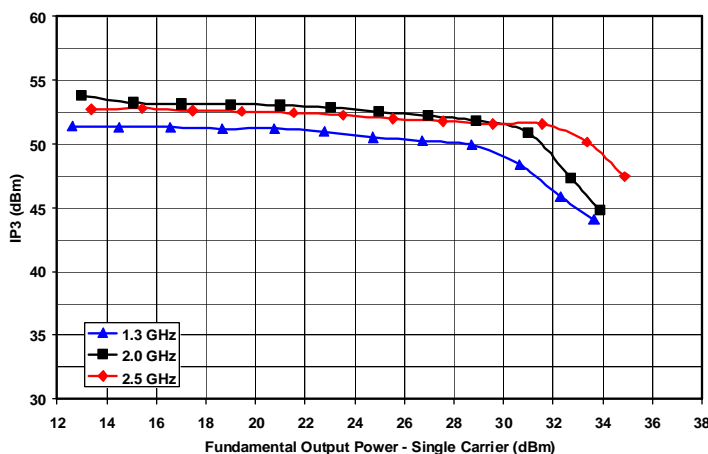


Figure 21. Third Order Intercept vs. Output Power and Frequency at VD = 8V and IDQ = 4.75A

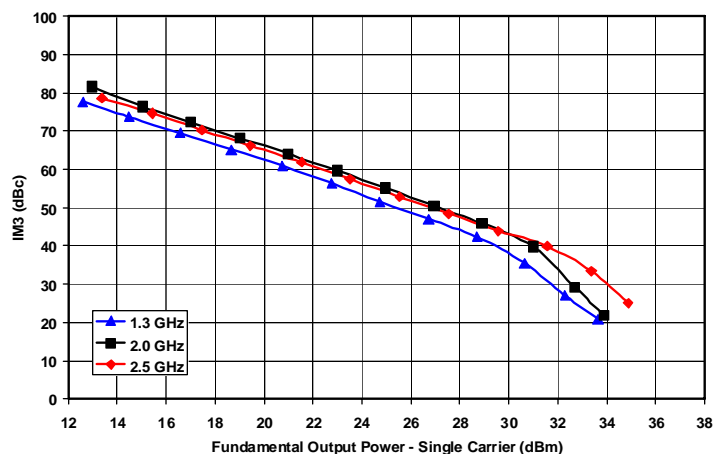


Figure 22. Third Order Intermod vs. Output Power and Frequency at VD = 8V and IDQ = 4.75A

VD = 10V

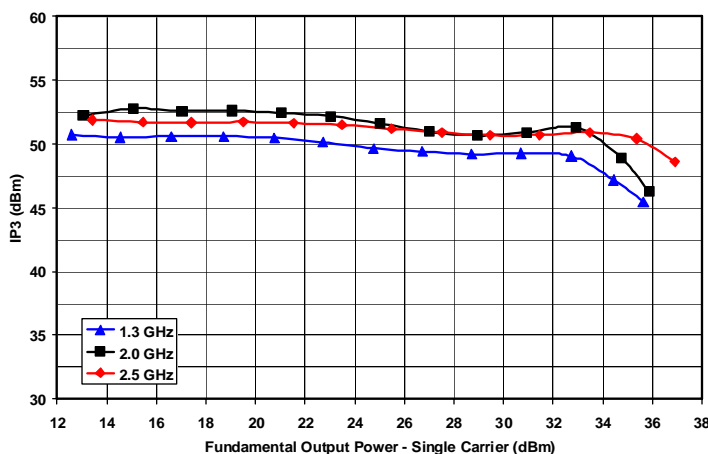


Figure 23. Third Order Intercept vs. Output Power and Frequency at VD = 10V and IDQ = 3.80A

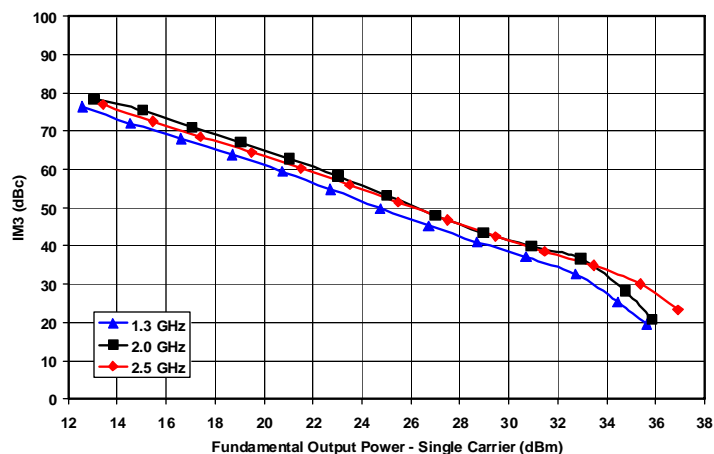


Figure 24. Third Order Intermod vs. Output Power and Frequency at VD = 10V and IDQ = 3.80A

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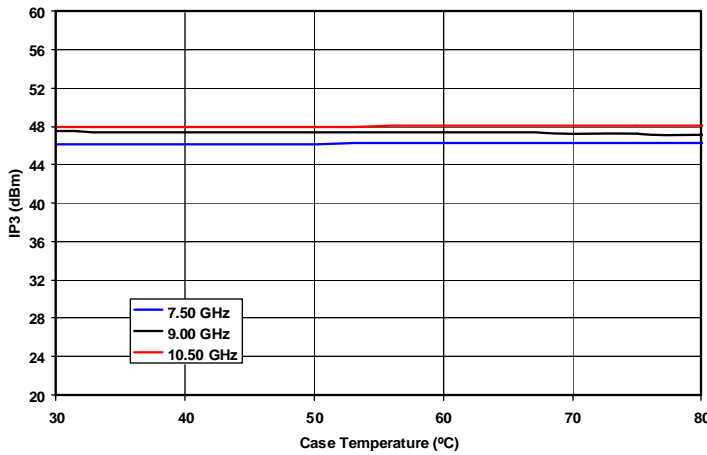


Figure 25. Third Order Intercept vs. Case Temperature and Frequency at Single Carrier Output Power Level = 28dBm, VD = 10V and IDQ = 3.20A

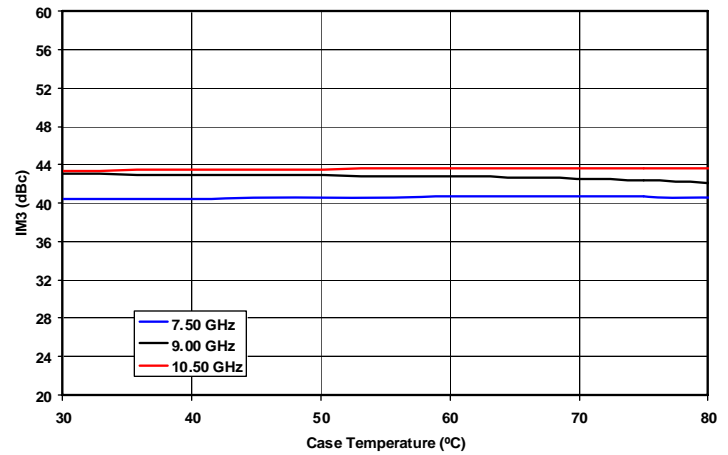


Figure 26. Third Order Intermod vs. Case Temperature and Frequency at Single Carrier Output Power Level = 28dBm, VD = 10V and IDQ = 3.20A

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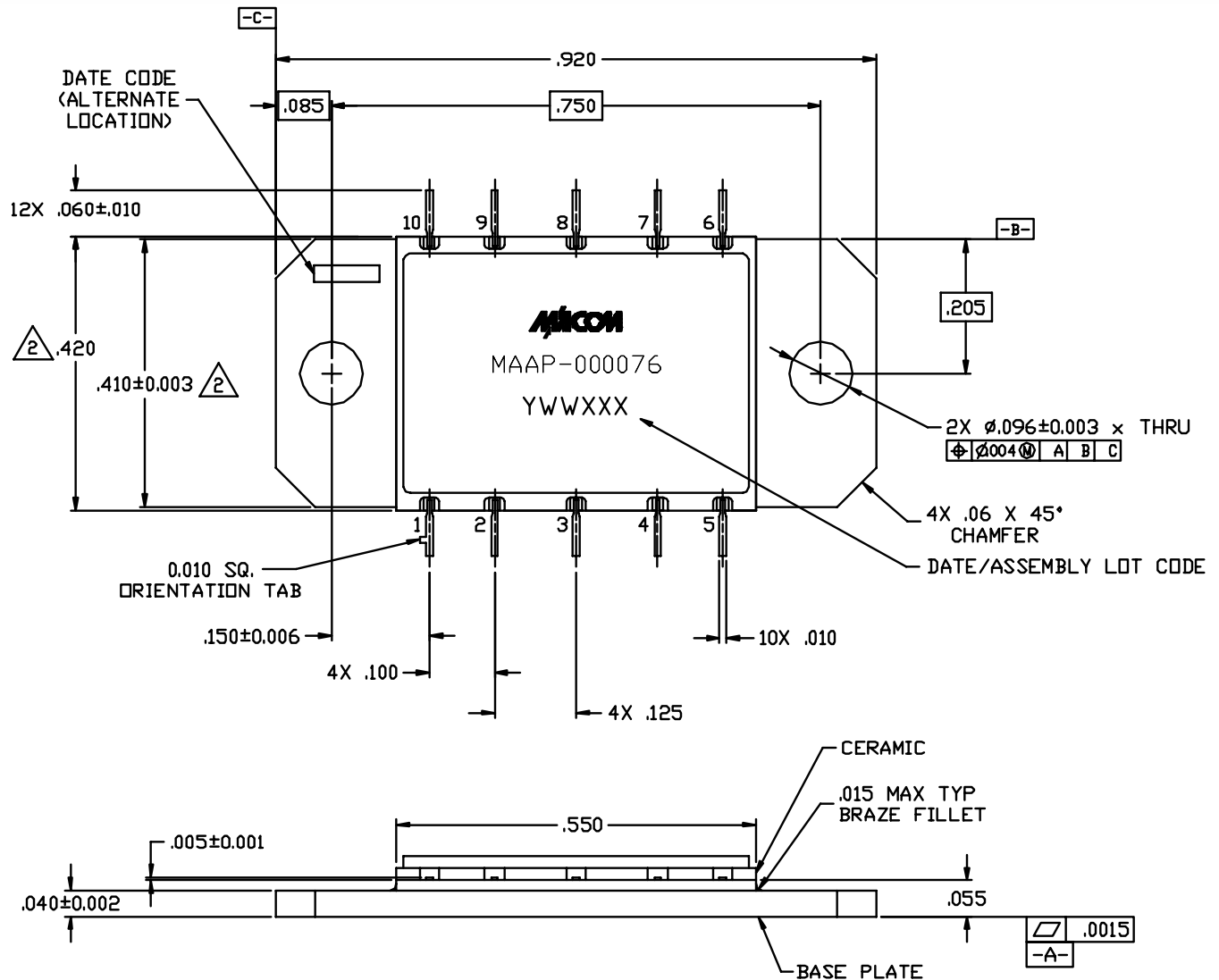
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Figure 27. Package Dimensions

This is a high frequency, low thermal resistance package. The package consists of a cofired ceramic construction with a copper-tungsten base and iron-nickel-cobalt leads. The finish consists of electrolytic gold over nickel plate.

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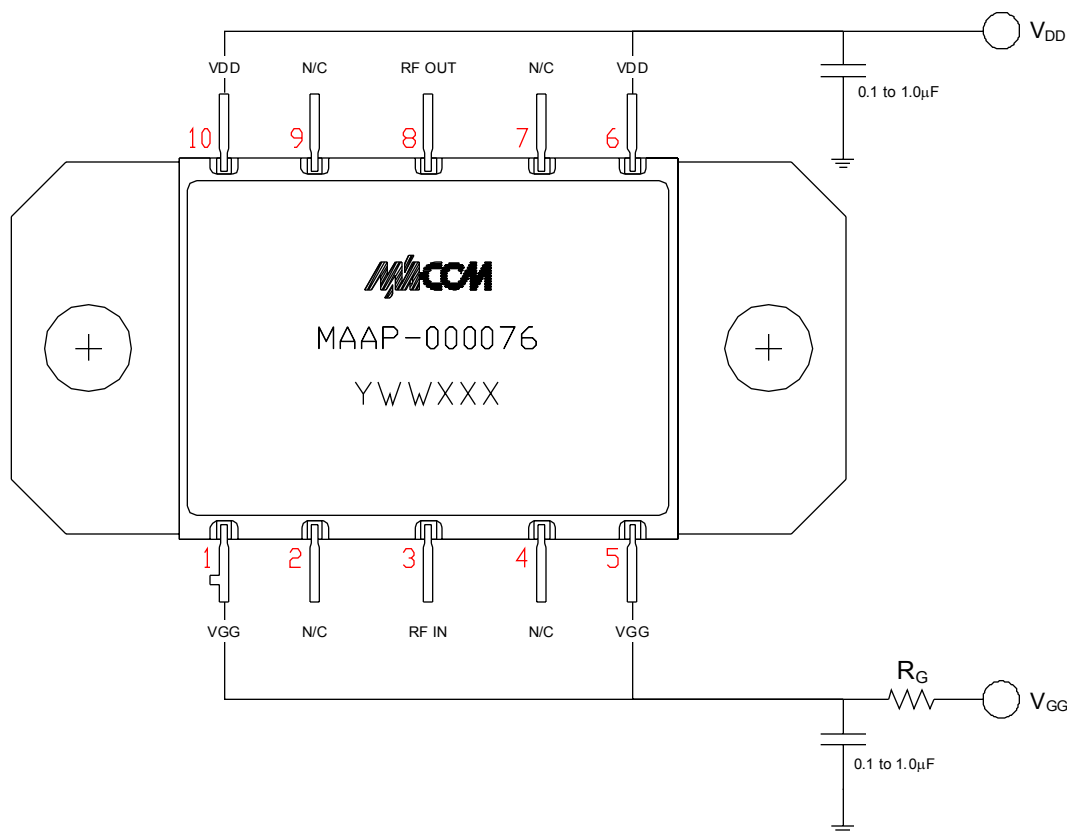


Figure 28. Recommended Bias Configuration

Assembly Instructions:

This flange mount style package provides a robust interface between a highly integrated GaAs MMIC device and a circuit board which may be assembled using conventional surface mount techniques. A thin shim made of a thermally and electrically conductive, ductile material must be used prior to installation of the ceramic package for proper thermal and electrical performance. Refer to **M/A-COM Application Note #M567*** for more information regarding shim material and mounting screw torque requirements.

For applications where surface mount components are to be installed after the ceramic package installation, this package will not be damaged when subjected to typical convection or IR oven reflow profiles. Refer to **M/A-COM Application Note #M538*** for maximum allowable reflow time and temperature. Alternatively, the package leads may be individually soldered. Whether an iron or hot gas soldering equipment is used, care should be taken to insure that the temperature is well controlled and electric static discharge (ESD) safe.

* Application Notes are available upon request.

Biasing Notes:

- ◆ A negative bias must be applied to V_{GG} before applying a positive bias to V_{DD} to prevent damage to the amplifier.

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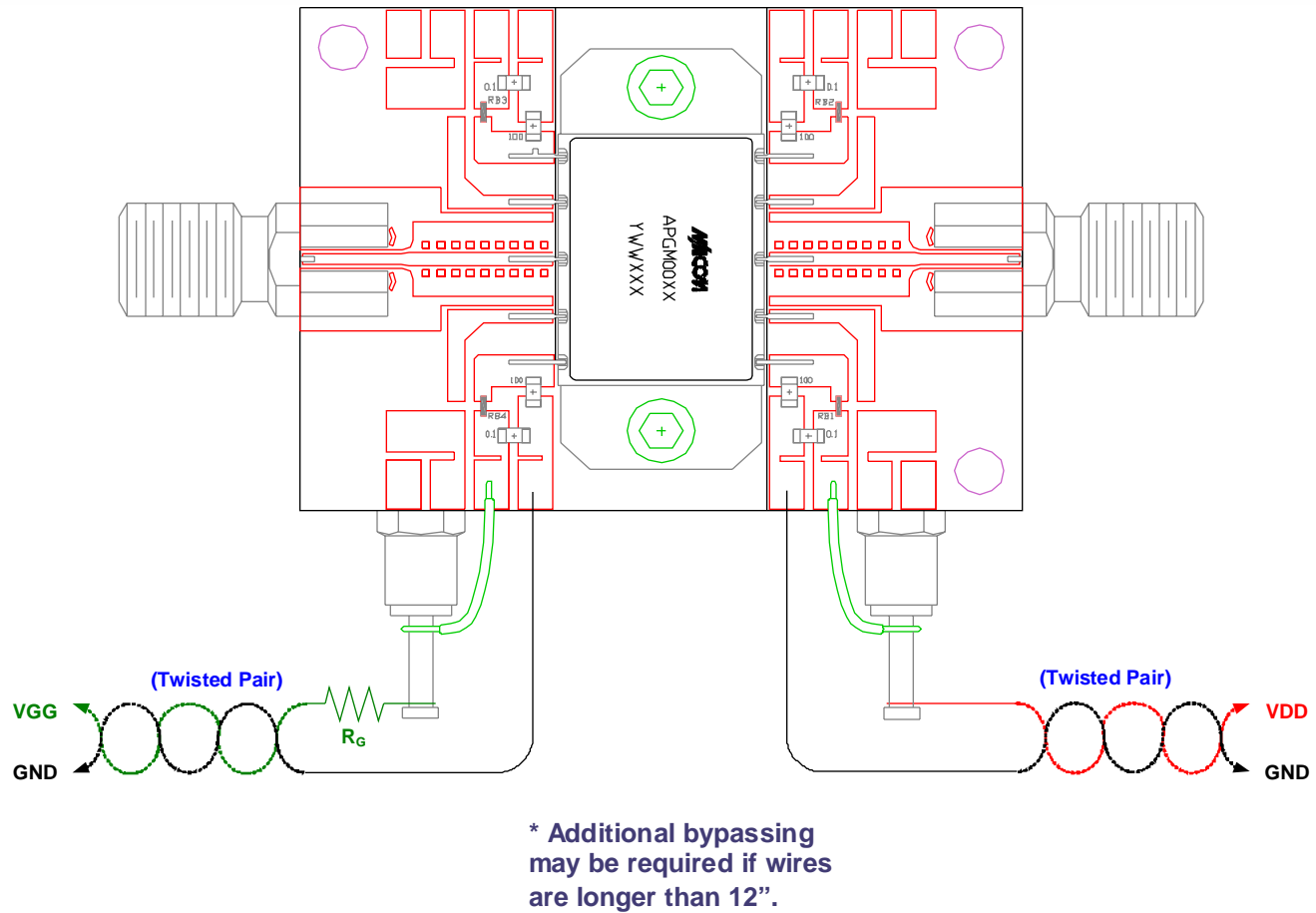


Figure 29. MAAP-000076-PKG001 Evaluation Board