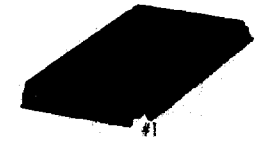
INTRODUCTION

The KS0107B is an LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems.
This device provides 64 shift registers and 64 output drivers. It generates the timing signal to control the KS0108B (64 channel segment driver).
The KS0107B is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display system in combination with the KS0108B (64 channel segment driver).

100 QFP-1420C



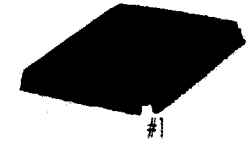
FEATURES

- Dot matrix LCD common driver with 64 channel output
- 64-bit shift register at internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode
- Applicable LCD duty : 1/48, 1/64, 1/96, 1/128
- Power supply voltage: + 5V ± 10%
- LCD driving voltage : 8V~17V (V_{DD}-V_{EE})
- Interface

Driver		Controller
COMMON	SEGMENT	
Other KS0107B	KS0108B	MPU

- High voltage CMOS process
- 100QFP / 100TQFP and bare chip available

100 TQFP-1414



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SAMSUNG ELECTRONICS

BLOCK DIAGRAM

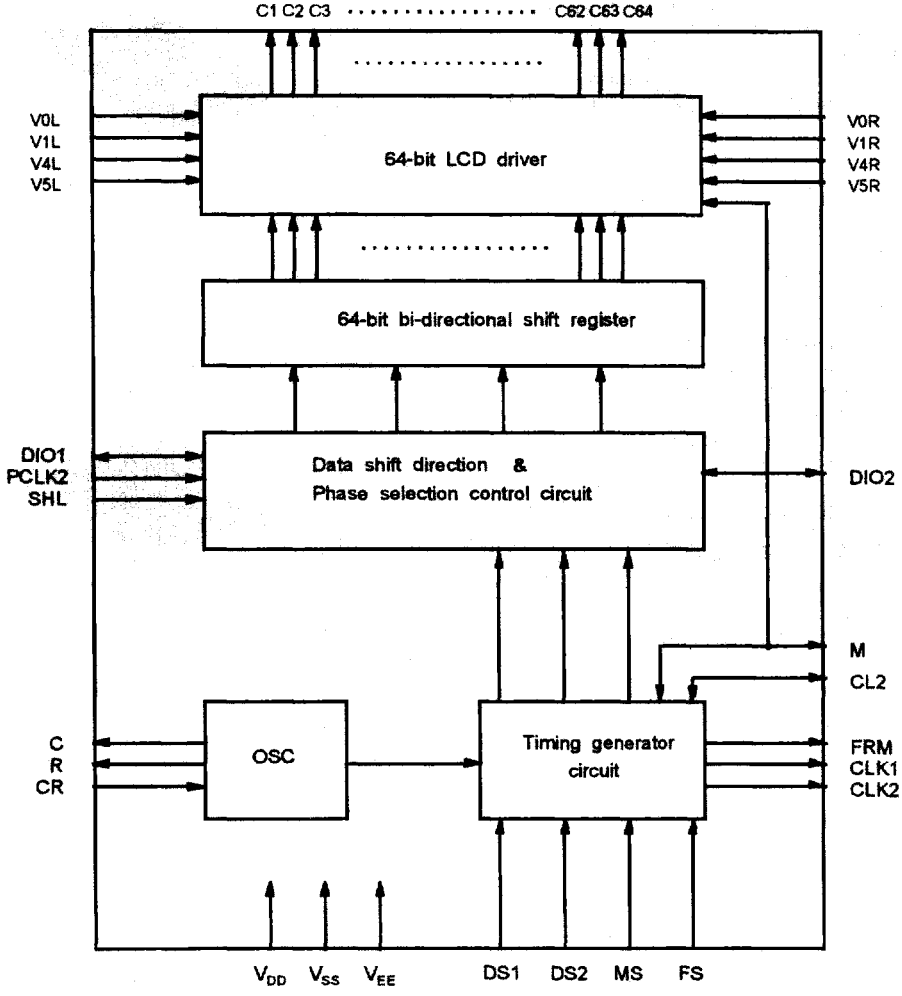


Fig 1. KS0107B Functional block diagram

PIN CONFIGURATION

1. 100QFP

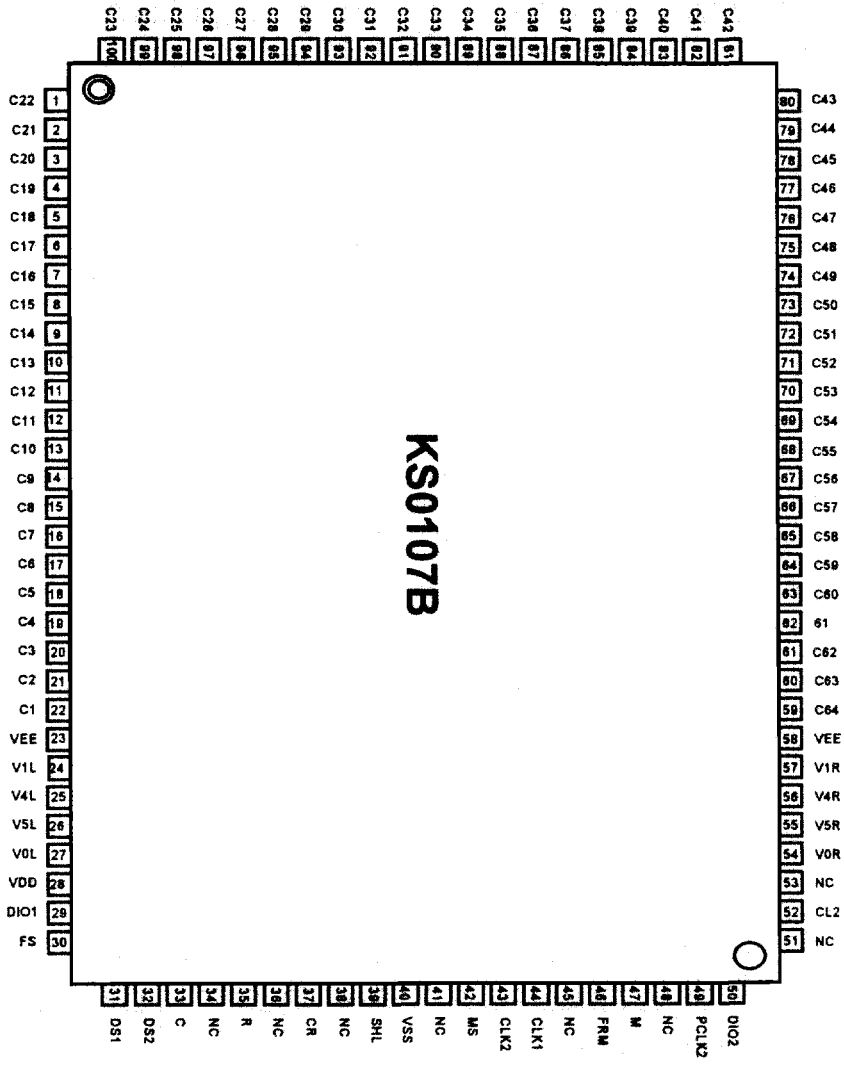
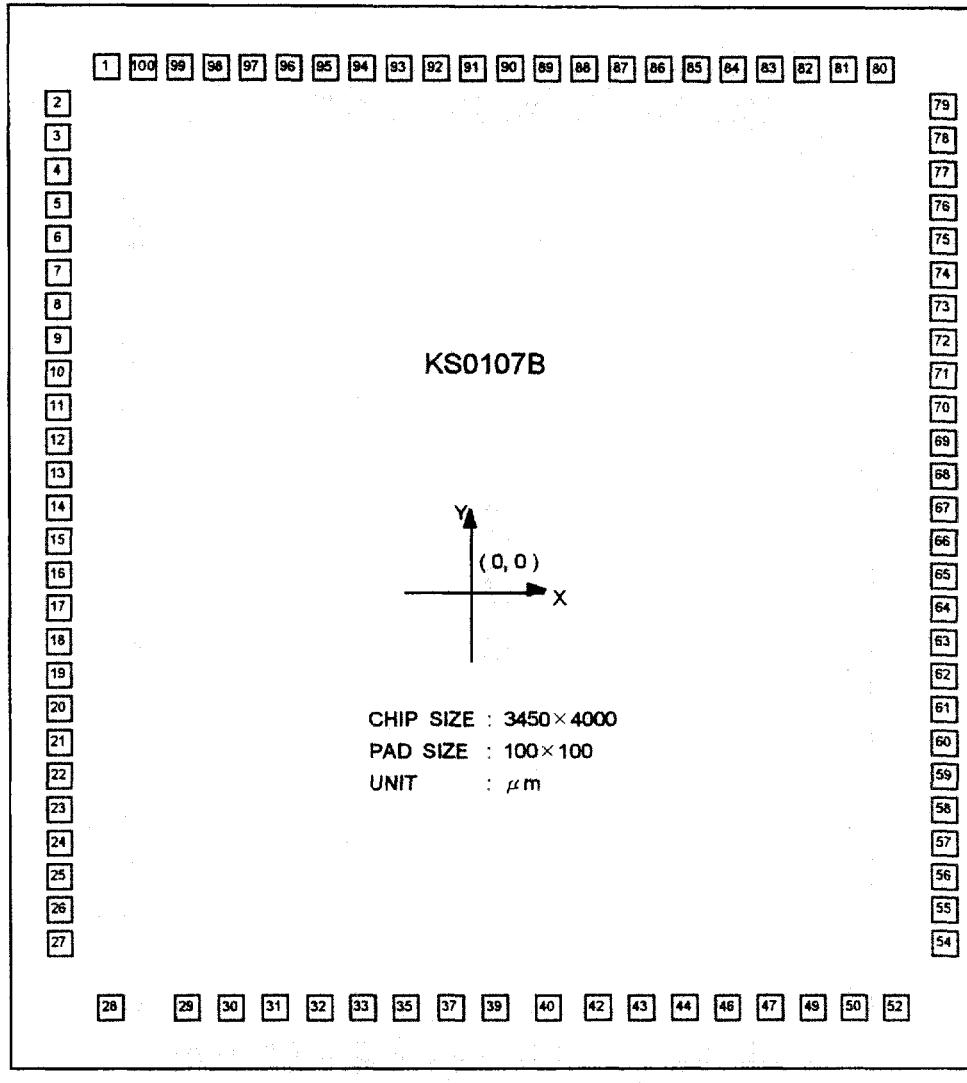


Fig2. 100 QFP Top View

PAD DIAGRAM (Chip layout for the 100QFP)



* There is the mark KS0107B on the center of the chip

SAMSUNG ELECTRONICS

PAD LOCATION (100QFP)

UNIT (um)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1	C22	-1314.5	1775.4	37	CR	-227.6	-1775	77	C46	1500.9	1380
2	C21	-1499.9	1630	39	SHL	-77.6	-1775	78	C45	1500.9	1505
3	C20	-1499.9	1505	40	VSS	113.8	-1775	79	C44	1500.9	1630
4	C19	-1499.9	1380	42	MS	308.7	-1775	80	C43	1310.5	1775.4
5	C18	-1499.9	1255	43	CLK2	458.7	-1775	81	C42	1185.5	1775.4
6	C17	-1499.9	1130	44	CLK1	608.7	-1775	82	C41	1060.5	1775.4
7	C16	-1499.9	1005	46	FRM	758.7	-1775	83	C40	935.5	1775.4
8	C15	-1499.9	880	47	M	908.7	-1775	84	C39	810.5	1775.4
9	C14	-1499.9	775	49	PCLK2	1058.7	-1775	85	C38	685.5	1775.4
10	C13	-1499.9	630	50	DIO2	1208.7	-1775	86	C37	560.5	1775.4
11	C12	-1499.9	505	52	CL2	1358.7	-1775	87	C36	435.5	1775.4
12	C11	-1499.9	380	54	V0R	1500.9	-1495	88	C35	310.5	1775.4
13	C10	-1499.9	255	55	V5R	1500.9	-1370	89	C34	185.5	1775.4
14	C9	-1499.9	130	56	V4R	1500.9	-1245	90	C33	60.5	1775.4
15	C8	-1499.9	5	57	V1R	1500.9	-1120	91	C32	-64.5	1775.4
16	C7	-1499.9	-120	58	VEE	1500.9	-995	92	C31	-189.5	1775.4
17	C6	-1499.9	-245	59	C64	1500.9	-870	93	C30	-314.5	1775.4
18	C5	-1499.9	-370	60	C63	1500.9	-745	94	C29	-439.5	1775.4
19	C4	-1499.9	-495	61	C62	1500.9	-620	95	C28	-564.5	1775.4
20	C3	-1499.9	-620	62	C61	1500.9	-495	96	C27	-689.5	1775.4
21	C2	-1499.9	-745	63	C60	1500.9	-370	97	C26	-814.5	1775.4
22	C1	-1499.9	-870	64	C59	1500.9	-245	98	C25	-939.5	1775.4
23	VEE	-1499.9	-995	65	C58	1500.9	-120	99	C24	-1064.5	1775.4
24	V1L	-1499.9	-1120	66	C57	1500.9	5	100	C23	-1189.5	1775.4
25	V4L	-1499.9	-1245	67	C56	1500.9	130				
26	V5L	-1499.9	-1370	68	C55	1500.9	255				
27	V0L	-1499.9	-1495	69	C54	1500.9	380				
28	VDD	-1345.6	-1775	70	C53	1500.9	505				
29	DIO1	-1127.6	-1775	71	C52	1500.9	630				
30	FS	-979.6	-1775	72	C51	1500.9	755				
31	DS1	-827.6	-1775	73	C50	1500.9	880				
32	DS2	-677.6	-1775	74	C49	1500.9	1005				
33	C	-527.6	-1775	75	C48	1500.9	1130				
35	R	-377.6	-1775	76	C47	1500.9	1255				

2. 100TQFP

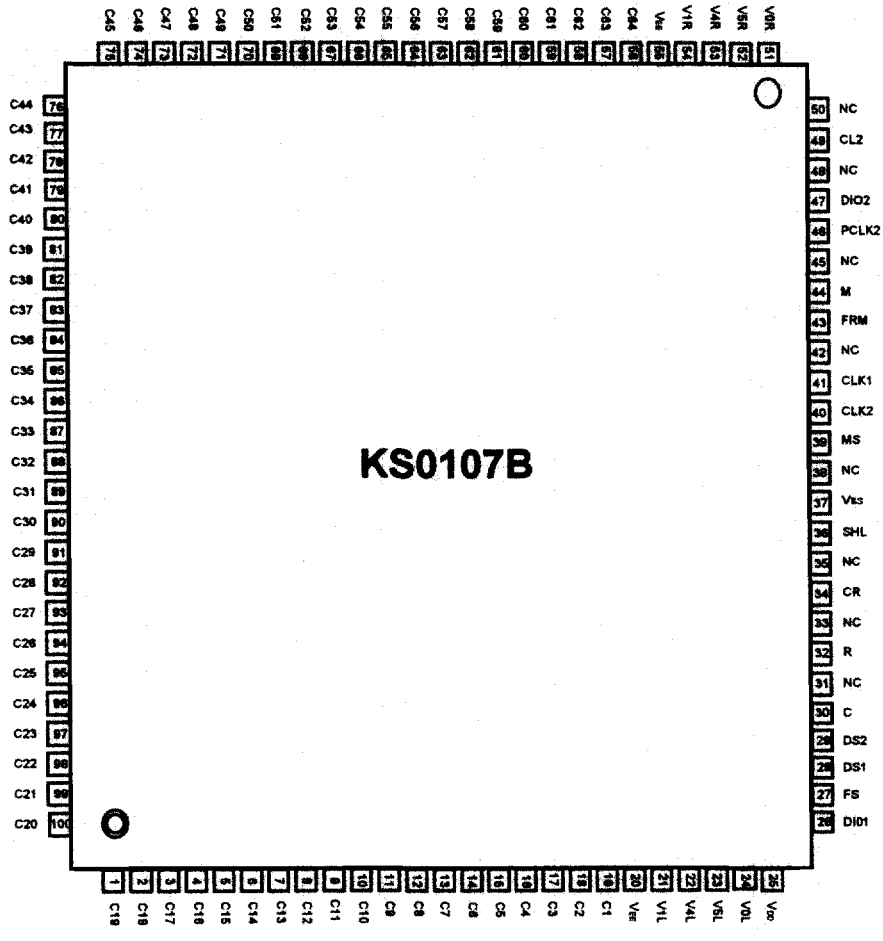
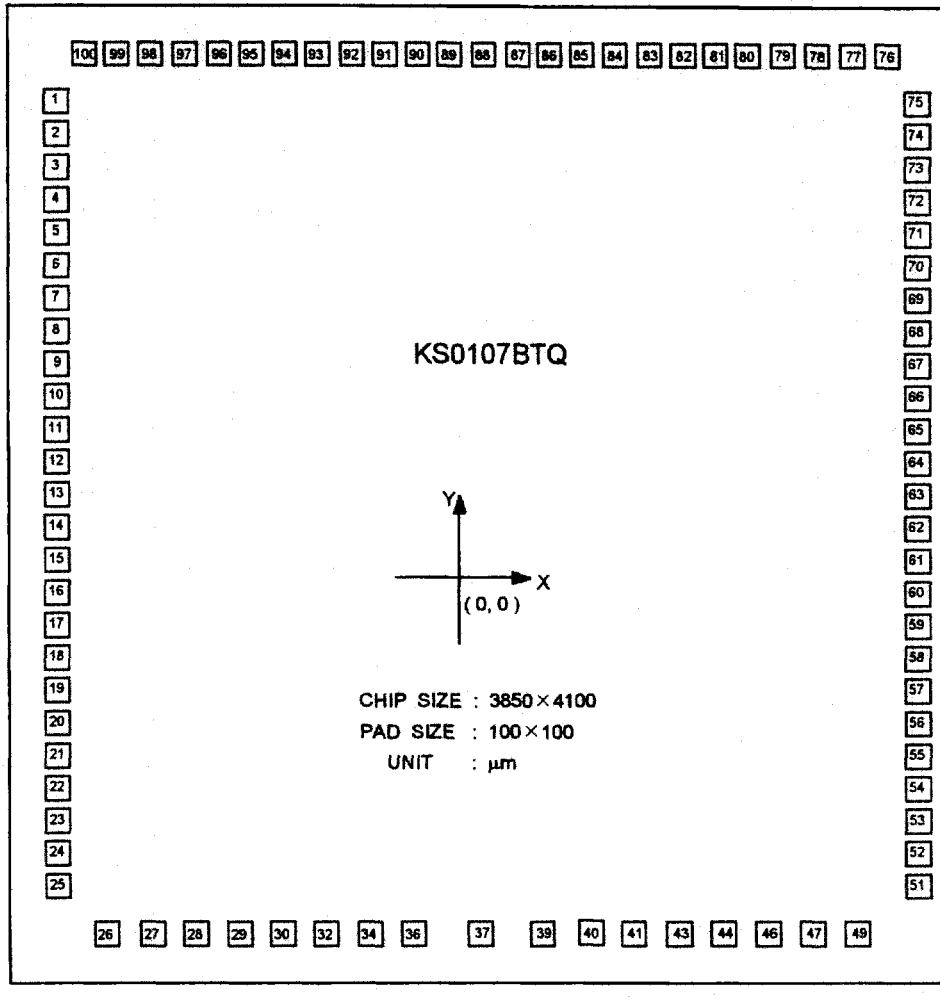


Fig3. 100 TQFP Top View

PAD DIAGRAM (Chip layout for the 100TQFP)



* There is the mark KS0107BTQ on the center of the chip.

PAD LOCATION (100TQFP)

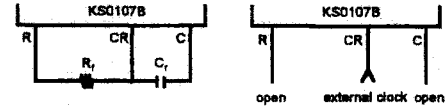
UNIT (um)

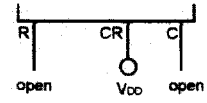
PAD NUM	PAD NAME	COORDINATE		PAD NUM	PAD NAME	COORDINATE		PAD NUM	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1	C19	-1697	1534	47	DIO2	1095	-1821	93	C27	-625	1822
2	C18	-1697	1409	48	NC			94	C26	-750	1822
3	C17	-1697	1284	49	CL2	1245	-1821	95	C25	-875	1822
4	C16	-1697	1159	50	NC			96	C24	-1000	1822
5	C15	-1697	1034	51	V0R	1697	-1466	97	C23	-1125	1822
6	C14	-1697	909	52	V5R	1697	-1341	98	C22	-1250	1822
7	C13	-1697	784	53	V4R	1697	-1216	99	C21	-1375	1822
8	C12	-1697	659	54	V1R	1697	-1091	100	C20	-1500	1822
9	C11	-1697	534	55	VEE	1697	-966				
10	C10	-1697	409	56	C64	1697	-841				
11	C9	-1697	284	57	C63	1697	-716				
12	C8	-1697	159	58	C62	1697	-591				
13	C7	-1697	34	59	C61	1697	-466				
14	C6	-1697	-91	60	C60	1697	-341				
15	C5	-1697	-216	61	C59	1697	-216				
16	C4	-1697	-341	62	C58	1697	-91				
17	C3	-1697	-466	63	C57	1697	34				
18	C2	-1697	-591	64	C56	1697	159				
19	C1	-1697	-716	65	C55	1697	284				
20	VEE	-1697	-841	66	C54	1697	409				
21	V1L	-1697	-966	67	C53	1697	534				
22	V4L	-1697	-1091	68	C52	1697	659				
23	V5L	-1697	-1216	69	C51	1697	784				
24	V0L	-1697	-1341	70	C50	1697	909				
25	VDD	-1697	-1466	71	C49	1697	1034				
26	DIO1	-1245	-1821	72	C48	1697	1159				
27	FS	-1095	-1821	73	C47	1697	1284				
28	DS1	-945	-1821	74	C46	1697	1409				
29	DS2	-795	-1821	75	C45	1697	1534				
30	C	-645	-1821	76	C44	1500	1822				
31	NC			77	C43	1375	1822				
32	R	-495	-1821	78	C42	1250	1822				
33	NC			79	C41	1125	1822				
34	CR	-345	-1821	80	C40	1000	1822				
35	NC			81	C39	875	1822				
36	SHL	-195	-1821	82	C38	750	1822				
37	VSS	0	-1821	83	C37	625	1822				
38	NC			84	C36	500	1822				
39	MS	195	-1821	85	C35	375	1822				
40	CLK2	345	-1821	86	C34	250	1822				
41	CLK1	495	-1821	87	C33	125	1822				
42	NC			88	C32	0	1822				
43	FRM	645	-1821	89	C31	-125	1822				
44	M	795	-1821	90	C30	-250	1822				
45	NC			91	C29	-375	1822				
46	PCLK2	945	-1821	92	C28	-500	1822				

PIN DESCRIPTION

<table>
<tr><th>PIN NUM
QFP(TQFP)</th><th>SYMBOL</th><th>INPUT/OUTPUT</th><th>DESCRIPTION</th></tr>
<tr><td>28(25)
40(37)
23(20),58(55)</td><td>V_{DD}
V_{SS}
V_{EE}</td><td>Power</td><td>For internal logic circuit (+5V ± 10%)
GND (= 0 V)
For LCD driver circuit</td></tr>
<tr><td>27(24), 54(51)
24(21), 57(54)
25(22), 56(53)
26(23), 55(52)</td><td>V0L, V0R
V1L, V1R
V4L, V4R
V5L, V5R</td><td>Power</td><td>Bias supply voltage terminals to drive LCD.
<table><tr><th>Select Level</th><th>Non-Select Level</th></tr><tr><td>V0L(R), V5L(R)</td><td>V1L(R), V4L(R)</td></tr></table>
V0L and V0R (V1L & V1R, V4L & V4R, V5L & V5R) should be connected by the same voltage.</td></tr>
<tr><td>42(39)</td><td>MS</td><td>Input</td><td>Selection of master/slave mode
i) Master mode (MS=1)
DIO1, DIO2, CL2 and M is output state.
ii) Slave mode (MS=0)
SHL=1 → DIO1 is input state (DIO2 is output state)
SHL=0 → DIO2 is input state (DIO1 is output state)
CL2 and M are input state.</td></tr>
<tr><td>39(36)</td><td>SHL</td><td>Input</td><td>Selection of data shift direction.
<table><tr><th>SHL</th><th>Data shift direction</th></tr><tr><td>H</td><td>DIO1 → C1 → ..... → C64 → DIO2</td></tr><tr><td>L</td><td>DIO2 → C64 → ..... → C1 → DIO1</td></tr></table></td></tr>
<tr><td>49(46)</td><td>PCLK2</td><td>Input</td><td>Selection of shift clock (CL2) phase.
<table><tr><th>PCLK2</th><th>Shift clock (CL2) phase</th></tr><tr><td>H</td><td>data shift at the rising edge of CL2</td></tr><tr><td>L</td><td>data shift at the falling edge of CL2</td></tr></table></td></tr>
<tr><td>30(27)</td><td>FS</td><td>Input</td><td>Selection of oscillation frequency.
i) Master mode
When the frame frequency is 70 Hz, the oscillation frequency should be
fosc=430 kHz at FS=1 (V_{DD})
fosc=215 kHz at FS=0 (V_{SS})
ii) Slave mode
Connect to V_{DD}.</td></tr>
<tr><td>31(28)
32(29)</td><td>DS1
DS2</td><td>Input</td><td>Selection of display duty.
i) Master mode
<table><tr><th>DS1</th><th>DS2</th><th>Duty</th></tr><tr><td>L</td><td>L</td><td>1/48</td></tr><tr><td>L</td><td>H</td><td>1/64</td></tr><tr><td>H</td><td>L</td><td>1/96</td></tr><tr><td>H</td><td>H</td><td>1/128</td></tr></table>
ii) Slave mode
Connect to V_{DD}.</td></tr>
</table>

PIN DESCRIPTION (continued)

<table>
<tr><th>PIN NUM
QFP(TQFP)</th><th>SYMBOL</th><th>INPUT/OUTPUT</th><th>DESCRIPTION</th></tr>
<tr><td>33(30)
35(32)
37(34)</td><td>C
R
CR</td><td></td><td>RC Oscillator
i) Master mode : use these terminals as shown below.
 

ii) Slave mode : stop the oscillator as shown below.
 
</td></tr>
<tr><td>44(41), 43(40)</td><td>CLK1
CLK2</td><td>Output</td><td>Operating clock output for the KS0108B
i) Master mode : connection to CLK1 and CLK2 of the KS0108B
ii) Slave mode : open</td></tr>
<tr><td>46(43)</td><td>FRM</td><td>Output</td><td>Synchronous frame signal.
i) Master mode : connection to FRM of the KS0108B
ii) Slave mode : open</td></tr>
<tr><td>47(44)</td><td>M</td><td>Input / Output</td><td>Alternating signal input for LCD driving.
i) Master mode : output state
Connection to M of the KS0108B
ii) Slave mode : input state
Connection to the controller</td></tr>
<tr><td>52(49)</td><td>CL2</td><td>Input / Output</td><td>Data shift clock
i) Master mode : output state
Connection to CL of the KS0108B
ii) Slave mode : input state
Connection to shift clock terminal of the controller.</td></tr>
<tr><td>29(26)

50(47)</td><td>DIO1

DIO2</td><td>Input / Output</td><td>Data input/output pin of internal shift register.
<table>
<tr><th>MS</th><th>SHL</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>22~1
(19~1)
100~59
(100~56)</td><td>C1~C64</td><td>Output</td><td>Common signal output for LCD driving.
<table>
<tr><th>DATA</th><th>M</th><th>OUT</th></tr>
<tr><td>L</td><td>L</td><td>V_1</td></tr>
<tr><td>L</td><td>H</td><td>V_4</td></tr>
<tr><td>H</td><td>L</td><td>V_5</td></tr>
<tr><td>H</td><td>H</td><td>V_0</td></tr>
</table></td></tr>
<tr><td>34(31),36(33)
38(35),41(38)
45(42),48(45)
51(48),53(50)</td><td>NC</td><td></td><td>No Connection</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating Voltage	V_{DD}	-0.3~+7.0	V	*1
Supply Voltage	V_{EE}	V_{DD}-19.0~V_{DD}+0.3	V	*4
Driver Supply Voltage	V_8	-0.3~V_{DD}+0.3	V	*1,2
	V_{LCD}	V_{EE}-0.3~V_{DD}+0.3	V	*3,4
Operating Temperature	T_{OPR}	-30~+85	℃	-
Storage Temperature	T_{STG}	-55~+125	℃	-

*1. Based on V_{SS}=0 V
*2. Applies to input terminals and I/O terminals at high impedance.
(Except V0L(R), V1L(R), V4L(R) and V5L(R))
*3. Applies to V0L(R), V1L(R), V4L(R) and V5L(R).
*4. Voltage level: $V_{DD} \geq$ V0L=V0R $\geq$ V1L=V1R $\geq$ V4L=V4R $\geq$ V5L=V5R $\geq V_{EE}$.

ELECTRICAL CHARACTERISTICS

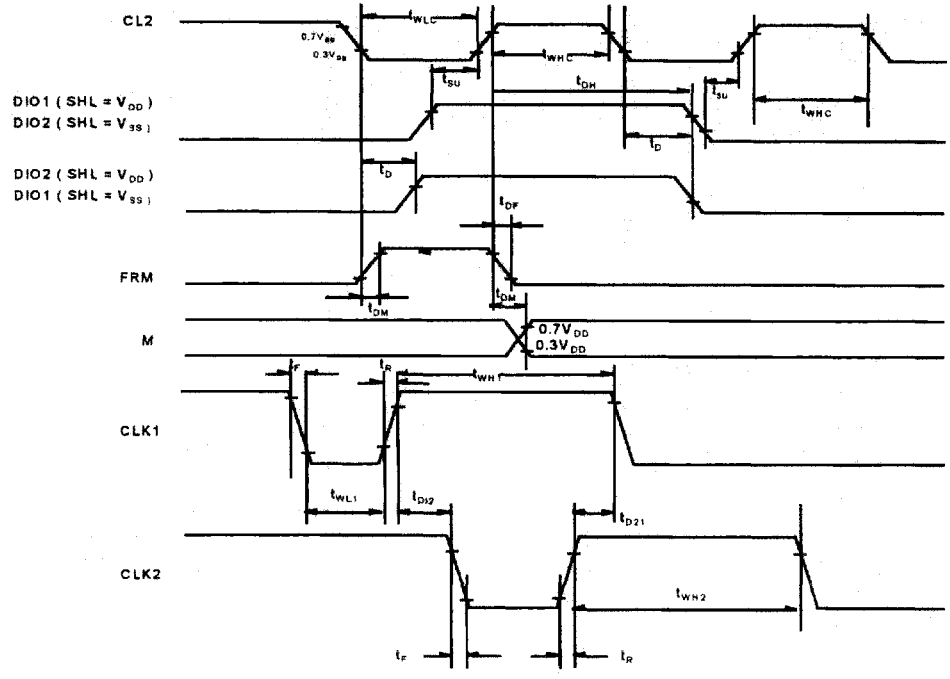
DC Characteristics (V_{DD}=+5V ± 10%, V_{SS}=0V, $|V_{DD}-V_{EE}|$=8~17V, T_a= -30 ~ +85 ℃)

Characteristic		Symbol	condition	Min	Typ	Max	Unit	Note
Input Voltage	High	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V	*1
	Low	V_{IL}		V_{SS}	-	0.3V_{DD}		
Output Voltage	High	V_{OH}	I_{OH}=-0.4 mA	V_{DD}-0.4	-	-	V	*2
	Low	V_{OL}	I_{OL}=0.4 mA	-	-	0.4		
Input Leakage Current		I_{LKG}	V_{IN}=V_{DD}~V_{SS}	-1.0	-	1.0	μA	*1
OSC Frequency		f_{OSC}	Rf=47K Ω ± 2% Cf=20pf ± 5%	315	450	585	KHz	
On Resistance (Vdiv-Ci)		R_{ON}	V_{DD}-V_{EE}=17V Load current = ± 150 μA	-	-	1.5	K Ω	
Operating Current		I_{DD1}	Master mode 1/128 Duty	-	-	1.0	mA	*3
		I_{DD2}	Slave mode 1/128 Duty	-	-	200	μA	*4
Supply Current		I_{EE}	Master mode 1/128 Duty	-	-	100		*5
Operating Frequency		f_{op1}	Master mode External clock	50	-	600	KHz	
		f_{op2}	Slave mode	0.5	-	1500		

*1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
*2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the output state.
*3. This value is specified at about the current flowing through V_{SS}.
Internal oscillation circuit: Rf=47 k Ω, Cf=20 pF
Each terminal of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.
*4. This value is specified at about the current flowing through V_{SS}.
Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is connected to V_{DD}, and MS is connected to V_{SS}. CL2, M, DIO1 is external clock.
*5. This value is specified at about the current flowing through V_{EE}.
Don't connect to V_{LCD} (V1~V5).

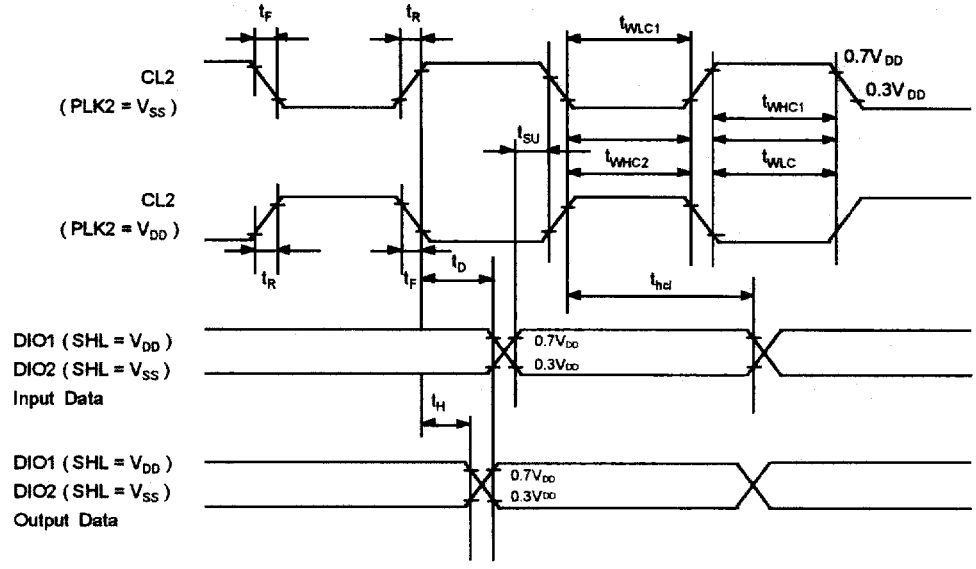
AC Characteristics (VDD=5V ± 10%, Ta=-30 ℃~+85 ℃)

1. Master mode (MS=V_{DD}, PCLK2=V_{DD}, Cf=20 pF, Rf=47 K Ω)



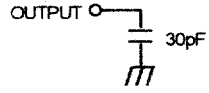
Characteristic	Symbol	Min	Typ	Max	Unit
Data Setup Time	t_{SU}	20	-	-	μs
Data Hold Time	t_{DH}	40	-	-	
Data Delay Time	t_D	5	-	-	
FRM Delay Time	t_{DF}	-2	-	2	
M Delay Time	t_{DM}	-2	-	2	
CL2 Low Level Width	t_{WLC}	35	-	-	
CL2 High Level Width	t_{WHC}	35	-	-	
CLK1 Low Level Width	t_{WL1}	700	-	-	ns
CLK2 Low Level Width	t_{WL2}	700	-	-	
CLK1 High Level Width	t_{WH1}	2100	-	-	
CLK2 High Level Width	t_{WH2}	2100	-	-	
CLK1-CLK2 Phase Difference	t_{D12}	700	-	-	
CLK2-CLK1 Phase Difference	t_{D21}	700	-	-	
CLK1, CLK2 Rise/Fall Time	t_R/t_F	-	-	150	

2. Slave mode (MS=V_{SS})



Characteristics	Symbol	Min	Typ	Max	Unit	Note
CL2 Low Level Width	t_{WLC1}	450	-	-	ns	PCLK2=V_{SS}
CL2 High Level Width	t_{WHC1}	150	-	-	ns	PCLK2=V_{SS}
CL2 Low Level Width	t_{WLC2}	150	-	-	ns	PCLK2=V_{DD}
CL2 High Level Width	t_{WHL}	450	-	-	ns	PCLK2=V_{DD}
Data Setup Time	t_{SU}	100	-	-	ns	
Data Hold Time	t_{DH}	100	-	-	ns	
Data Delay Time	t_D	-	-	200	ns	*1
Output Data Hold Time	t_H	10	-	-	ns	
CL2 Rise/Fall Time	t_R/t_F	-	-	30	ns	

*1; Connect load CL=30 pF



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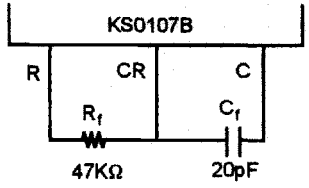
FUNCTIONAL DESCRIPTION

1. RC Oscillator

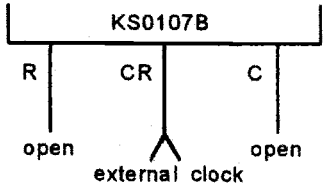
The RC Oscillator generates CL2, M, FRM of the KS0107B, and CLK1 and CLK2 of the KS0108B by the oscillation resister R and capacitor C.

When selecting the master/slave mode, the oscillation circuit is as following:

1) Master Mode : in the master mode, use these terminals as shown below.

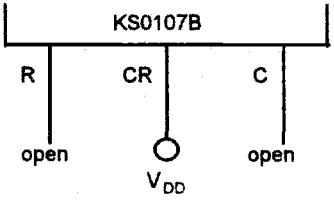


Internal Oscillation



External Clock

2) Slave Mode : in the slave mode, stop the oscillator as shown below.



2. Timing Generation Circuit

It generates CL2, M, FRM, CLK1 and CLK2 by the frequency from the oscillation circuit.

1) Selection of Master/Slave (M/S) Mode

When M/S is "H", it generates CL2, M, FRM, CLK1 and CLK2 internally.

When M/S is "L", it operates by receiving M and CL2 from the master device.

2) Frequency Selection (FS)

To adjust FRM frequency by 70 Hz, the oscillation frequency should be as follows:

FS	Oscillation Frequency
H	f_{osc}=430 kHz
L	f_{osc}=215 kHz

In the slave mode, it is connected to V_{DD}.

3) Duty Selection (DS1, DS2)

It provides various duty selections according to DS1 and DS2.

DS1	DS2	DUTY
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

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3. Data Shift & Phase Select Control

1) Phase Selection

It is a circuit to shift data on synchronization or rising edge, or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

2) Data Shift Direction Selection

When M/S is connected to V_{DD}, DIO1 and DIO2 terminal is only output.

When M/S is connected to V_{SS}, it depends on the SHL.

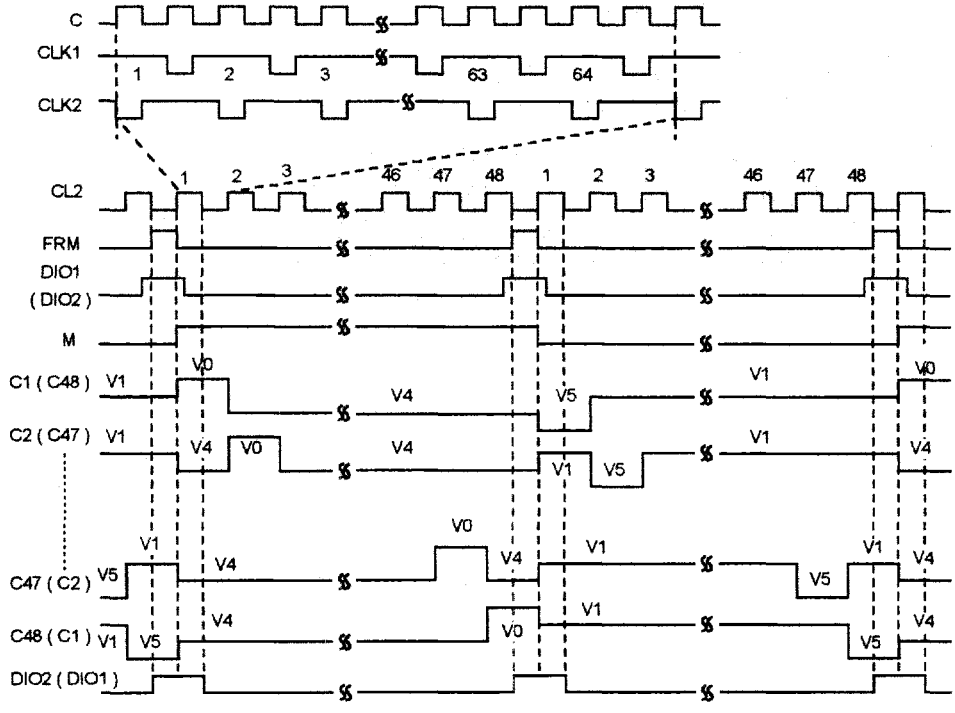
MS	SHL	DIO1	DIO2	Direction of Data
H	H	Output	Output	C1 → C64
	L	Output	Output	C64 → C1
L	H	Input	Output	DIO1 → C1 → C64 → DIO2
	L	Output	Input	DIO2 → C64 → C1 → DIO1

4

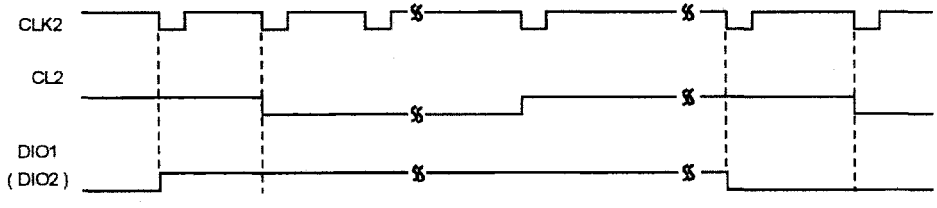
TIMING DIAGRAM

1. 1/48 Duty Timing (Master Mode)

Condition: DS1=L, DS2=L, SHL=H(L), PCLK2=H



- relation of CL2 & DIO1 (DIO2)



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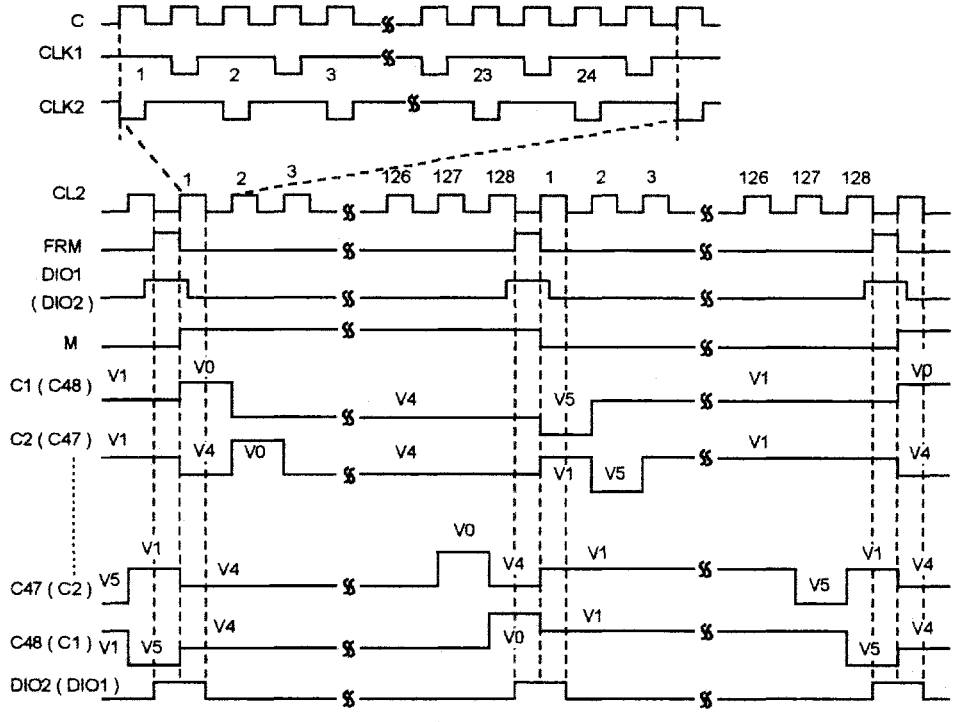
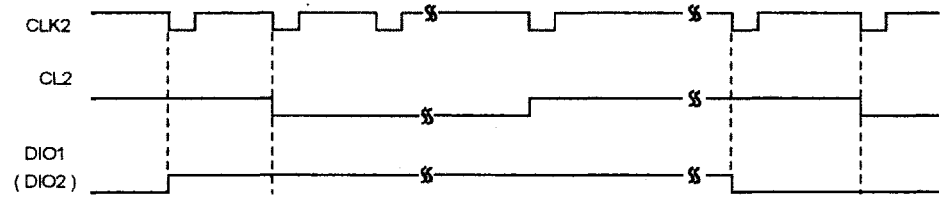
2. 1/128 duty timing (Master mode)
Condition: DS1=H, DS2=H, SHL=H(L), PCLK2=H



- relation of CL2 & DIO1 (DIO2)



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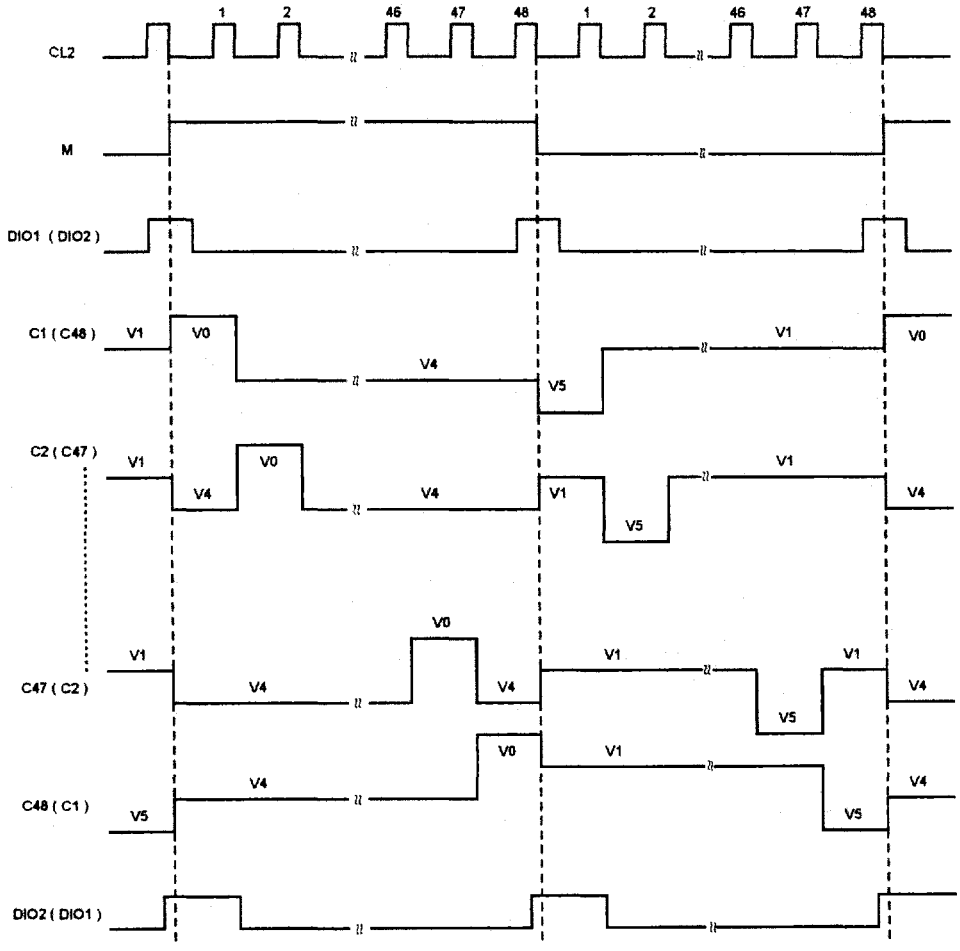
3. 1/48 Duty Timing (Slave Mode)

Condition: PCLK2=L, SHL=H(L)



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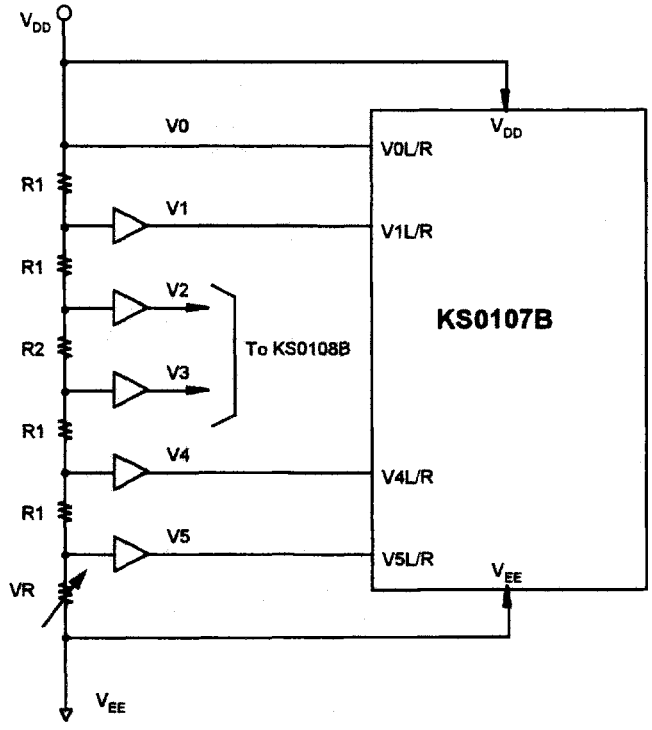
4. Power Driver Circuit



Relation of duty & bias

DUTY	BIAS	Rdiv
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

*When duty factor is 1/48, the value of R1 & R2 should satisfy.
R1/(4R1+R2)=1/8
R1=3 KΩ, R2=12 KΩ

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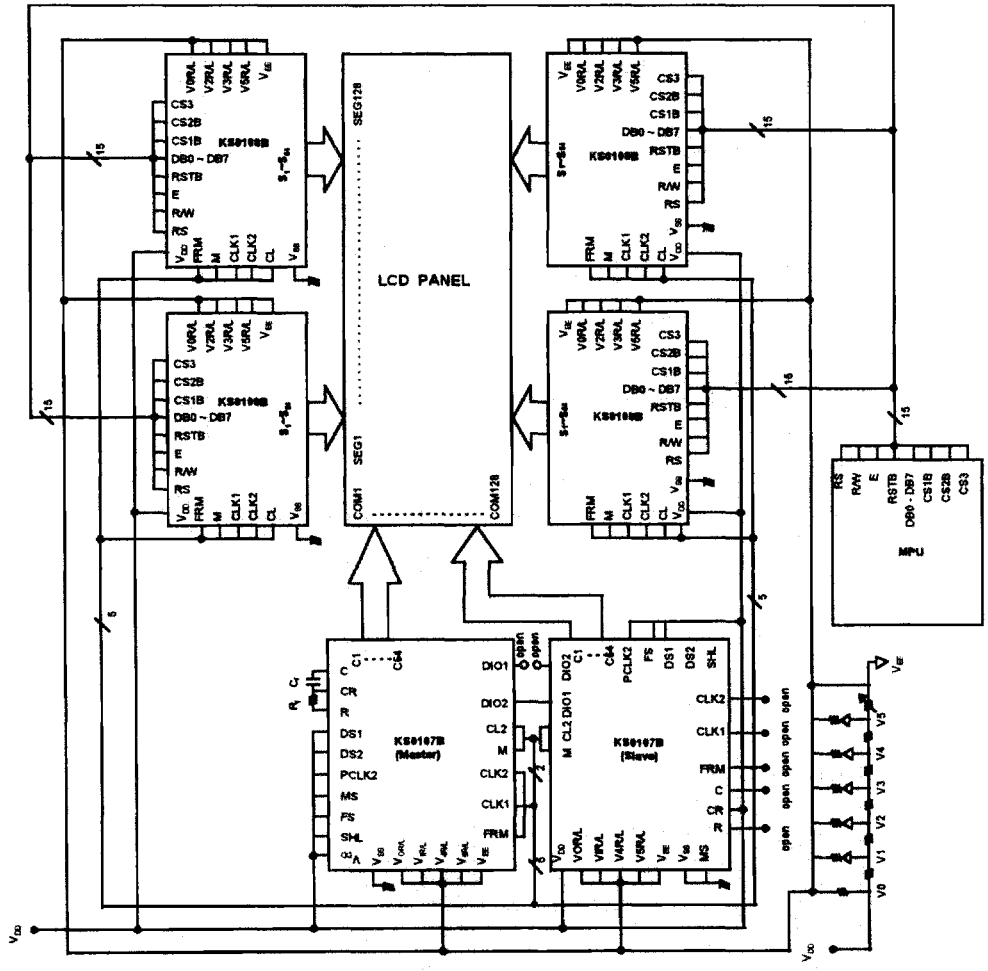
APPLICATION CIRCUIT

1/128 Duty Segment Drive(KS0108B) Interface Circuit



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