# 82C85/883

June 1989

## CMOS Static Clock Controller/Generator

#### Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Generates the System Clock For CMOS or NMOS Microprocessors and Peripherals
- Complete Control Over System Operation for Very Low System Power
  - ► Stop-Oscillator
  - ► Low Frequency
  - ► Stop-Clock
  - ► Full Speed Operation
- DC to 25MHz Operation (DC to 8MHz System Clock)
- Generates 50% and 33% Duty Cycle Clocks (Synchronized)
- Uses a Parallel Mode Crystal Circuit or External Frequency Source
- TTL Compatible Inputs/Outputs
- 24 Pin Slimline Dual-In-Line or 28 Pad Square LCC Package Options
- . Single 5V Power Supply
- Military Operating Temperature Range ...... -55°C to +125°C

### Description

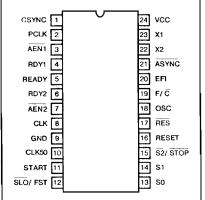
The Harris 82C85/883 Static CMOS Clock Controller/Generator provides complete control of static CMOS system operating modes and supports full speed, slow, stop-clock and stop-oscillator operation. While directly compatible with the Harris 80C86 and 80C88 16-bit Static CMOS Microprocessor Family, the 82C85/883 can also be used for general system clock control.

For static system designs, separate signals are provided on the 82C85/883 for stop (S0, S1, \$\overline{S2}/\overline{STOP}\$) and start (START) control of the crystal oscillator and system clocks. A single control line (\$\overline{SLO}/FST\$) determines 82C85 fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. Automatic maximum mode 80C86 and 80C88 software HALT instruction decode logic in the 82C85/883 enables software-based clock control. Restart logic insures valid clock start-up and complete synchronization of system clocks.

The 82C85/883 is manufactured using the Harris advanced Scaled SAJI IV CMOS process. In addition to clock control circuitry, the 82C85/883 also contains a crystal controlled oscillator (up to 25MHz), clock generation logic, complete "Ready" synchronization and reset logic. This permits the designer to tailor the system power-performance product to provide optimum performance at low power levels.

## **Pinouts**

82C85/883 (CERAMIC DIP) TOP VIEW



82C85/883 (CERAMIC LCC) TOP VIEW

