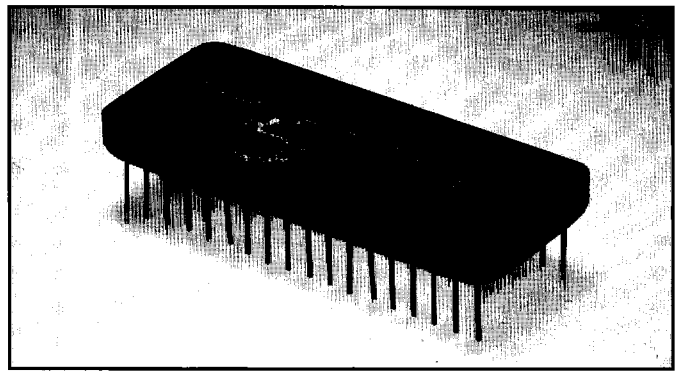
MIL-STD-1553 SINGLE & DUAL CHANNEL 5-VOLT TRANSCEIVERS FC1553 9 SERIES

The CMAC FC15539 is a complete data bus transmitter and receiver hybrid, driven from a single 5V supply. The device conforms to MIL-STD-1553B, and is screened to the requirements of MIL-STD-883 and BS9450 (CECC 63000).



- SINGLE RAIL OPERATION
- LOW POWER DISSIPATION
- RECEIVER OUTPUT LOGIC OPTIONS FOR ENCODER/DECODER COMPATIBILITY
- THIRD-ORDER BALANCED RECEIVER INPUT FILTERING
- ENHANCED INPUT LOGIC TRACKING AND FAULT PROTECTION
- SHORT CIRCUIT PROTECTION OF TRANSMITTER OUTPUTS

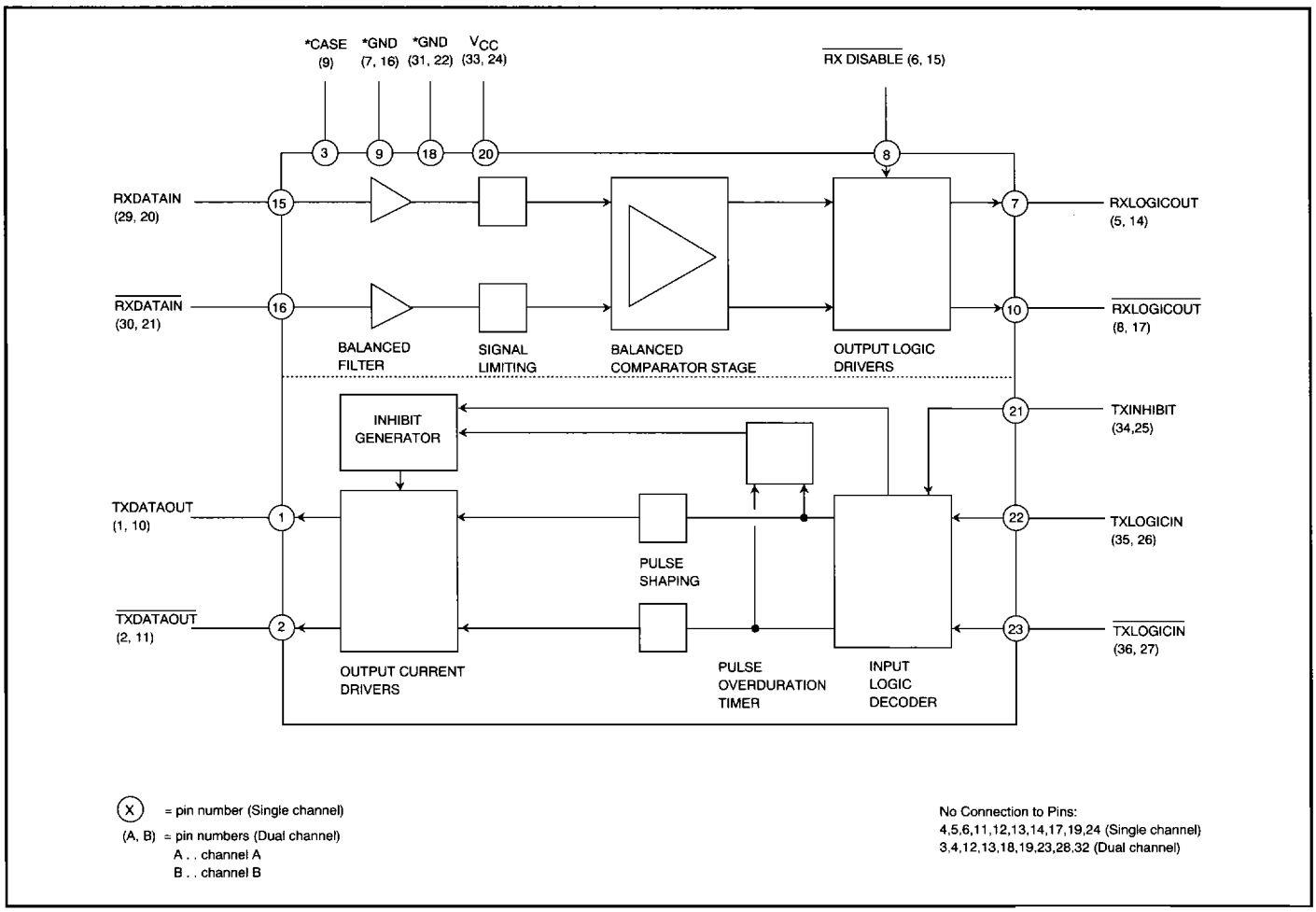


Fig. 1 Block Schematic

* All 'GND' and 'CASE' pins must be connected together externally.

GENERAL DESCRIPTION

(a) Receiver

The Receiver Input accepts Manchester II encoded bipolar data as differential signals 'RXDATAIN' and 'RXDATAIN'. taken from the 0 Volt Centre-tapped transformer.

The Receiver Outputs, 'RXLOGICOUT' and 'RXLOGICOUT' represent excursions of the differential-mode input signal beyond balanced positive and negative thresholds, and are compatible with standard TTL logic levels.

(b) Transmitter

The Transmitter Input accepts Biphase Manchester II encoded signals – 'TXLOGICIN' and 'TXLOGICIN' – and an inhibit signal 'TXINHIBIT' at standard TTL logic levels. In conjunction with the fault isolation resistors, termination resistors and bus transformers specified in fig. 4, a nominal 7.5V Bipolar Manchester II signal is produced on the bus (point 'a').

NOTE:

The transceiver channels of the dual-channel device are isolated, and have separate Vcc and ground pins.

RECEIVER DETAIL

- **Filtering and Differential Processing**

  'RXDATAIN' and 'RXDATAIN' pass through a balanced third-order low-pass filter to reduce the effects of line-reflections and to improve the signal-to-noise ratio: the signals are limited to acceptable voltage levels. Common-mode performance is enhanced by fully balanced processing of 'RXDATAIN' and 'RXDATAIN'.

- **RXDISABLE Pin (Receiver Strobe)**

  LOGIC '0' applied to 'RXDISABLE' disables the receiver and returns 'RXLOGICOUT' and 'RXLOGICOUT' to their quiescent state.

  The receiver is enabled by disconnecting, or applying logic '1' to 'RXDISABLE'.

- **Encoder-Decoder Compatibility Options**

  Transceivers are available with quiescent low or quiescent high versions of 'RXLOGICOUT' and 'RXLOGICOUT'.

TRANSMITTER DETAIL

- **Input Logic Tracking**

  To optimise transmitter operation, the input logic decoder tracks the crossover points of 'TXLOGICIN' and 'TXLOGICIN' A small deadband ensures transmission is inhibited if the inputs are 'shorted' together by a logic or interconnect fault.

- **Inhibit Generation and Transmitter Driver Protection**

  With 'TXINHIBIT' disconnected, or connected to Logic '1', transmission is inhibited regardless of the condition of 'TXLOGICIN' or 'TXLOGICIN'.

  Logic '0' applied to 'TXINHIBIT' results in transmission being inhibited under the following conditions only:

  –'TXLOGICIN' and 'TXLOGICIN' are at the same logic level

  –'TXLOGICIN' and 'TXLOGICIN' are shorted together

  –Supply voltage falls below approximately 4V

  –Case temperature exceeds approximately 175°C: (optional feature)

Symbol.	Parameter	Min	Typ	Max	Unit
	GENERAL				
V_{CC}	Supply Voltage Range	+4.5		+5.5	V
T_{CO}	Operating Case Temperature Range	–55		+125	°C
T_{CS}	Storage Temperature Range	–55		+150	°C
	LOGIC INPUTS				
V_{IH}	High Level Input Voltage	+2		+7	V
V_{IL}	Low Level Input Voltage	0		+1	V
	LOGIC OUTPUTS				
I_{OH}	High Level Output Current			+0.2	mA
I_{OL}	Low Level Output Current	–8			mA

Table 1 Recommended Operating Conditions

	LOGIC INPUTS				
I_{IH}	High Level Input Current			+0.02	mA
I_{IL}	Low Level Input Current	–1			mA
	LOGIC OUTPUTS				
V_{OH}	High Level Output Voltage	+2.4			V
V_{OL}	Low Level Output Voltage			+0.5	V

Table 2 Resulting Electrical Characteristics

Symbol.	Parameter	Min	Typ	Max	Unit
	INPUT SPECIFICATIONS - see fig. 4 for references • used with specified transformer (grounded centre tap) • measurements at: point 'c' (transformer coupled) point 'a' (direct coupled) unless otherwise stated.				
V_{ID}	Differential Voltage (line to line measured at point 'd')			± 8	V_{pk}
V_{IC}	*Common-Mode Voltage up to 2MHz (line to ground)	± 10			V_{pk}
CMRR	Common-Mode Rejection Ratio	40			dB
Z_{IN}	Differential Input Impedance f = 1MHz (not including transformer - measured at point 'd')	2.5			kΩ
V_{THD}	Differential Threshold Voltage, (sinewave input, referred to point 'a') f = 1MHz f = 2MHz f = 4MHz	0.84	1.0 2.5 14.0	1.15	V_{p-p} V_{p-p} V_{p-p}
	PROPAGATION DELAYS				
t_{dr}	Delay between differential zero crossing on 'RXDATAIN' and 50% point on 'RXLOGICOUT'		375		ns
t_{ds}	Delay between 50% point on '$\overline{\text{RXDISABLE}}$' and receiver turnon/turnoff		160		ns

Table 3 Receiver Specifications
*DC isolation voltage 50V for FC1553TI (5V) transformer

Symbol	Parameter	Min	Typ	Max	Unit
	OUTPUT SPECIFICATIONS see figs 2, 4				
V_{OP}	Line-Line output voltage, point 'X'	18	22	27	V_{p-p}
V_{OS}	Output offset, point 'X', measured 2.5 µs after zero crossing of last parity bit. transmission duty cycle = 25%		± 50	± 250	mV
t_r	Rise and Fall Times	100	180	300	ns
	PROPAGATION DELAYS				
t_{INP}	Delay from rising edge on 'TXINHIBIT' to quiescent outputs		250		ns
t_{INN}	Delay from falling edge on 'TXINHIBIT' to active outputs		250		ns
t_{DT}	Delay between 50% point on 'TXLOGICIN' or '$\overline{\text{TXLOGICIN}}$' and corresponding output zero-crossing		150		ns

Table 4 Transmitter Specifications

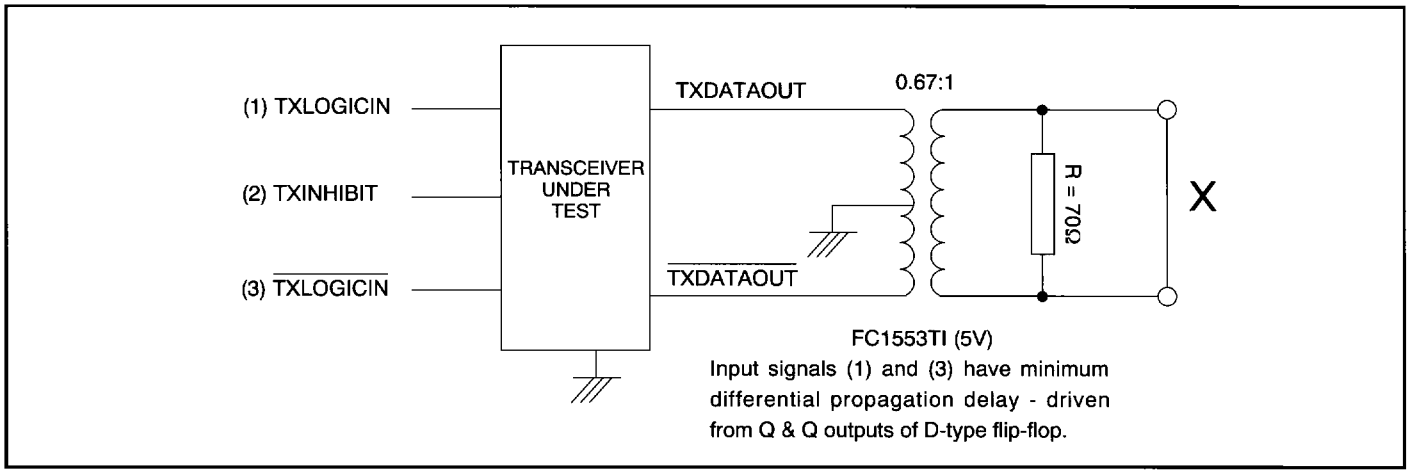


Fig. 2 Test Circuit for Transmit Amplitude and Offset

POWER, THERMAL AND SUPPLY DATA

Symbol	Parameter	Duty Cycle	Min	Typ	Max	Unit	Notes
I_{CC}	Supply Current ($4.5V<V_{CC}<5.5V$)						
	• Receiver active or quiescent Transmitter quiescent			30	45	mA	
	• Receiver active or quiescent	25%		160	220	mA	
	Transmitter active	100%		550	650	mA	
	THERMAL DATA						
P_{CR}	Power dissipation of most critical device on hybrid	100%		200	300	mW	
θ_{JC}	Junction-case thermal resistance of most critical device on hybrid			85	100	°C/W	
θ_{CA}	Case-ambient thermal resistance (temperature rise of case above ambient, per Watt internal dissipation - Fig. 3)			30		°C/W	
δ_{125}	Maximum allowable transmission duty cycle at case temperature 125°C				100	%	

Table 5 Power, Thermal and Supply Current Data

NOTE: The above data corresponds to one transceiver channel only and does not include the standby current or power dissipation of the idle channel circuitry in the dual channel device.

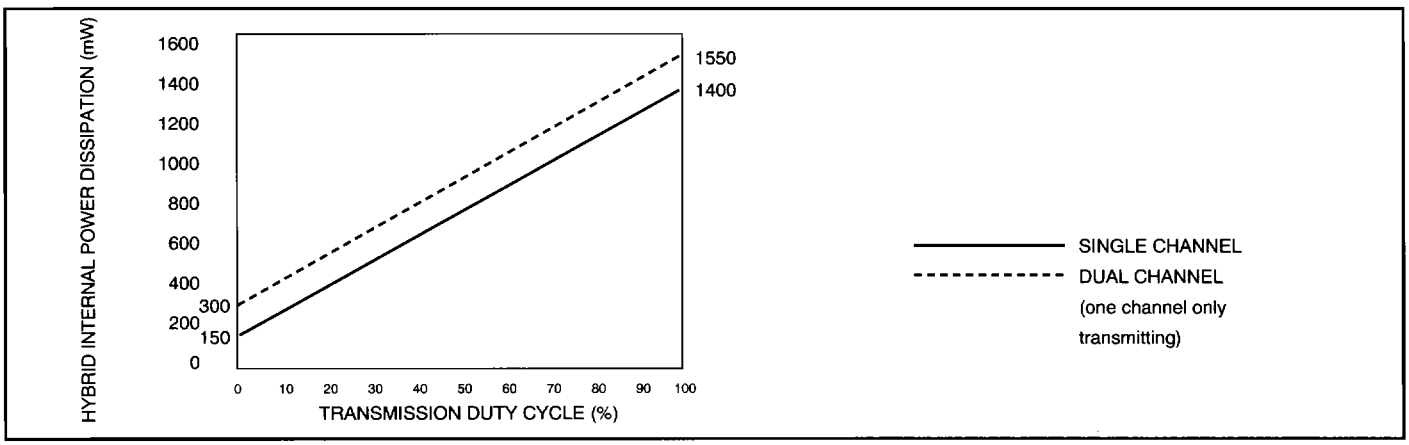


Fig. 3 Hybrid Internal Power Dissipation (Typical) for V_{CC} = 5.0V

RECOMMENDED APPLICATION PRECAUTIONS

(a) DECOUPLING

Decouple Vcc to ground, close to the hybrid, with a >10μF tantalum capacitor in parallel with a 100nF ceramic bypass capacitor.

NOTE: Peak transmission current drawn from Vcc is 550mA.

(b) PCB LAYOUT

- Full PCB ground-planing is recommended.
- It is good practice to ensure connections from encoder/decoder to 'TXLOGICIN', 'TXLOGICIN' and 'TXINHIBIT' are as short as possible and of balanced length, shape and area. Optimum results are obtained when these signals have minimum rise/fall times and minimum differential delays.
- Connections between 'TXDATAOUT' and the centre tapped transformer should be designed to:

(i) Withstand peak transmission currents at required operating duty cycles

(ii) Minimise added series inductance

(iii) Ensure tracking capacitance in conjunction with transceiver and transformer impedances does not reduce overall input impedance below the value stated in MIL-STD-1553B.

These connections should also be balanced in terms of length, shape and area.

PIN CONFIGURATION

Single Channel

Pin number	Function
1	TXDATAOUT
2	TXDATAOUT
3	CASE
4	n.c.
5	n.c.
6	n.c.
7	RXLOGICOUT
8	RXDISABLE
9	GND
10	RXLOGICOUT
11	n.c.
12	n.c.
13	n.c.
14	n.c.
15	RXDATAIN
16	RXDATAIN
17	n.c.
18	GND
19	n.c.
20	V_{CC}(+5V)
21	TXINHIBIT
22	TXLOGICIN
23	TXLOGICIN
24	n.c.

Dual Channel

Pin number	Channel	Function	Pin number	Channel	Function
1	1	TXDATAOUT	19	2	n.c.
2	1	TXDATAOUT	20	2	RXDATAIN
3	1	n.c.	21	2	RXDATAIN
4	1	n.c.	22	2	GND
5	1	RXLOGICOUT	23	2	n.c.
6	1	RXDISABLE	24	2	V_{CC}(+5V)
7	1	GND	25	2	TXINHIBIT
8	1	RXLOGICOUT	26	2	TXLOGICIN
9	1	CASE	27	2	TXLOGICIN
10	2	TXDATAOUT	28	1	n.c.
11	2	TXDATAOUT	29	1	RXDATAIN
12	2	n.c.	30	1	RXDATAIN
13	2	n.c.	31	1	GND
14	2	RXLOGICOUT	32	1	n.c.
15	2	RXDISABLE	33	1	V_{CC}(+5V)
16	2	GND	34	1	TXINHIBIT
17	2	RXLOGICOUT	35	1	TXLOGICIN
18	2	n.c.	36	1	TXLOGICIN

Table 6 Pin Configurations

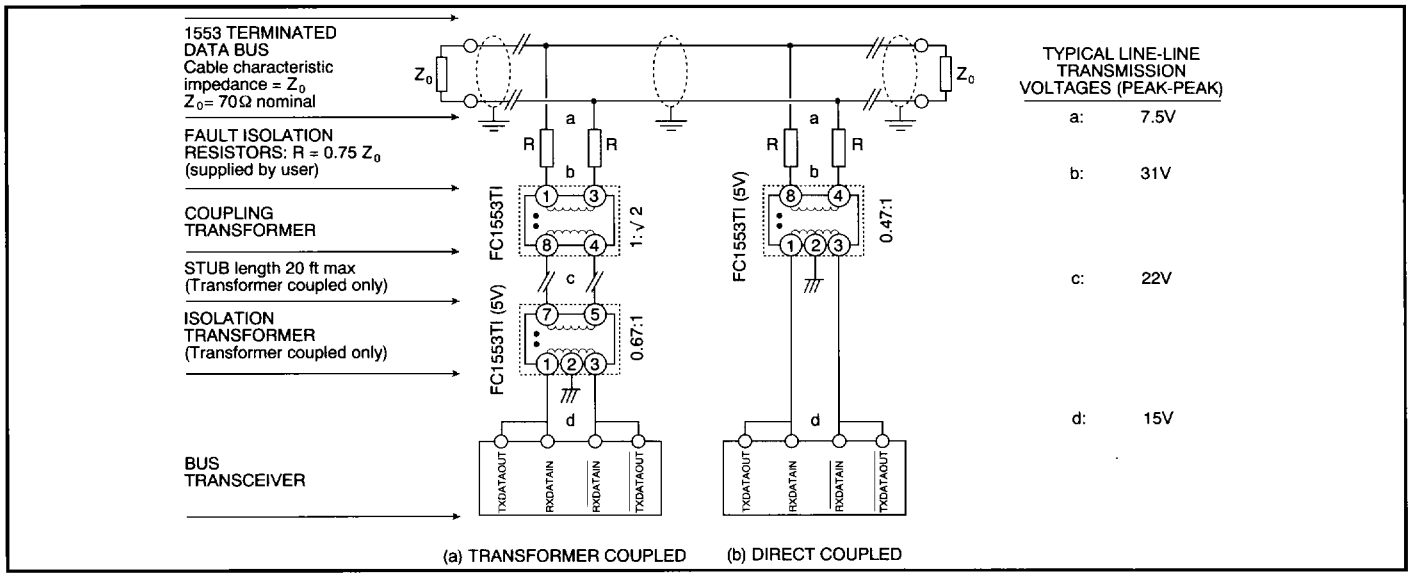


Fig. 4 Transceiver to bus connection diagram

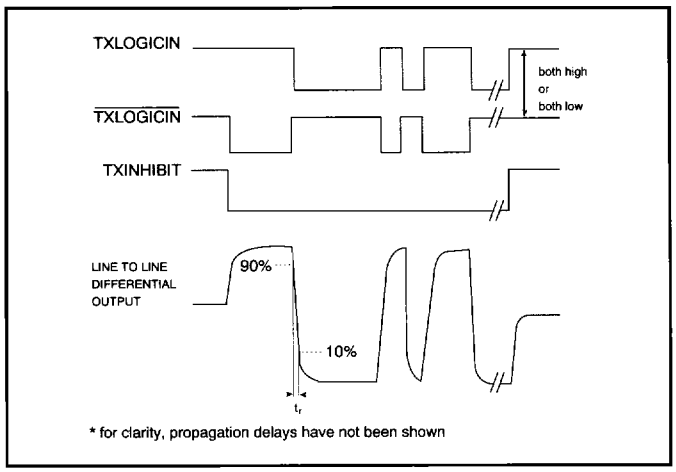


Fig. 5 Typical transmitter waveforms

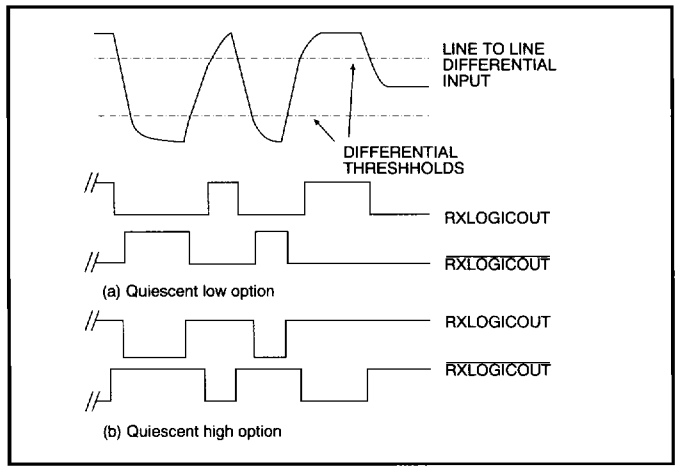


Fig. 6 Typical receiver waveforms

Product Number†	Options							
	Power Rails	Single Channel	Dual Channel	Receiver Output options		Transformation Ratio (transceiver side : stub side)		Transformer Part Number
	+5V only			Quiescent Low	Quiescent High	Isolation Transformer	Direct Coupling Transformer	
FC155391	•	•		•		0.67:1	0.47:1	FC1553TI (5V)
FC155392	•	•			•	0.67:1	0.47:1	FC1553TI (5V)
FC1553921	•		•	•		0.67:1	0.47:1	FC1553TI (5V)
FC1553922	•		•		•	0.67:1	0.47:1	FC1553TI (5V)
FC155393	•	•		•		0.57:1	0.40:1	FC1553TI (5VX)
FC155394	•	•			•	0.57:1	0.40:1	FC1553TI (5VX)
FC1553923	•		•	•		0.57:1	0.40:1	FC1553TI (5VX)
FC1553924	•		•		•	0.57:1	0.40:1	FC1553TI (5VX)

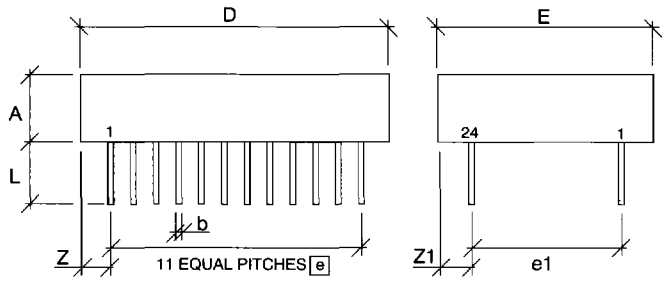
Table 7 Selection Guide

† Add 'FP' suffix to Product Number for 'Flatpack' package
Note: For MIL-STD-1553A Applications, refer to Supplier.

24-PIN SOLID SIDEWALL PACKAGE

REF	MIN	NOM	MAX
D			33.00 (1.300)
E			20.00 (0.790)
A			5.00 (0.190)
L	6.09 (0.240)		6.61 (0.260)
Øb	0.41 (0.016)		0.51 (0.020)
e		2.54 (0.100)	
e1		15.24 (0.600)	
Z			2.20 (0.087)
Z1			2.23 (0.088)

1 index mark indicates position of terminal No. 1



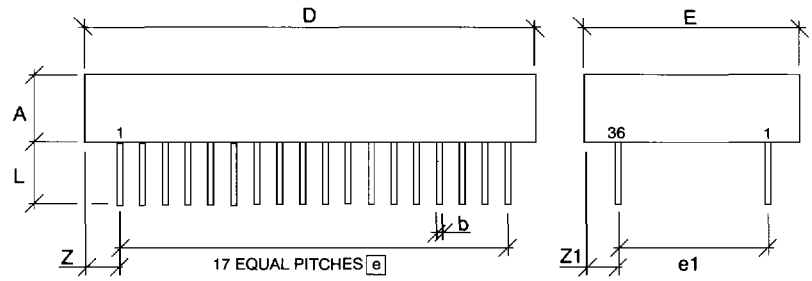
All dimensions in mm (inches) First Angle Projection

Fig. 8 Mechanical Outline (Single Channel)

36-PIN SOLID SIDEWALL PACKAGE

REF	MIN	NOM	MAX
D			48.26 (1.900)
E			19.95 (0.785
A			5.08 (0.200)
L	6.09 (0.240)		6.61 (0.260)
Øb	0.38 (0.015)		0.51 (0.020)
e		2.54 (0.100)	
e1		15.24 (0.600)	
Z			2.80 (0.110)
Z1			2.48 (0.097)

1 index mark indicates position of terminal No. 1



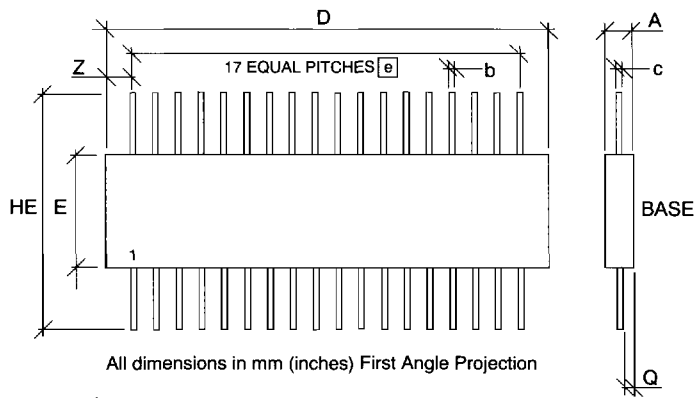
All dimensions in mm (inches) First Angle Projection

Fig. 9(a) Mechanical Outline (Dual Channel) – DIP

36-PIN FLATPACK

REF	MIN	NOM	MAX
e		2.54 (0.10)	
E		19.68 (0.775)	19.94 (0.785)
D	47.88 (1.885)	48.13 (1.895)	48.40 (1.905)
A		3.43 (0.135)	
Z		2.48 (0.098)	
b	0.304 (0.012)		0.456 (0.018)
c	0.20 (0.008)	0.25 (0.010)	0.30 (0.012)
Q		1.525 (0.060)	
HE	45.0 (1.77)		

1 index mark indicates position of terminal No. 1



All dimensions in mm (inches) First Angle Projection

Fig. 9(b) Mechanical Outline (Dual Channel) – Flatpack

The product assurance programme defines manufacturing procedures, establishes quality standards, in line inspection controls and 100% screening tests.
The standard 100% screening performed prior to product shipment is shown in the flow chart.
Manufactured in accordance with procedures laid down within MIL-STD-883 and BS9450 (CECC 63000).

Title	Factory Procedure	BS9450 Requirement	MIL-STD-883 Requirement
Internal Visual	FCES 6360	1.2.10	2017
Lid Seal	Welded	1.2.6.14	none
Stabilization Bake	FCES 6551	1.2.6.3.4	1008
Temperature Cycling	FCES 6552	1.2.6.13	1010
Constant Acceleration	FCES 6380	1.2.6.9	2001
Fine Leak	FCES 6370	1.2.6.14.1	1014
Gross Leak	FCES 6370	1.2.6.14.2	1014
Burn In	FCES 6390	1.2.9.2	1015
Final QC	FCES 6560	1.2.2	2009
	FCES 6376		
	FCES 6377		
	FCES 6370		

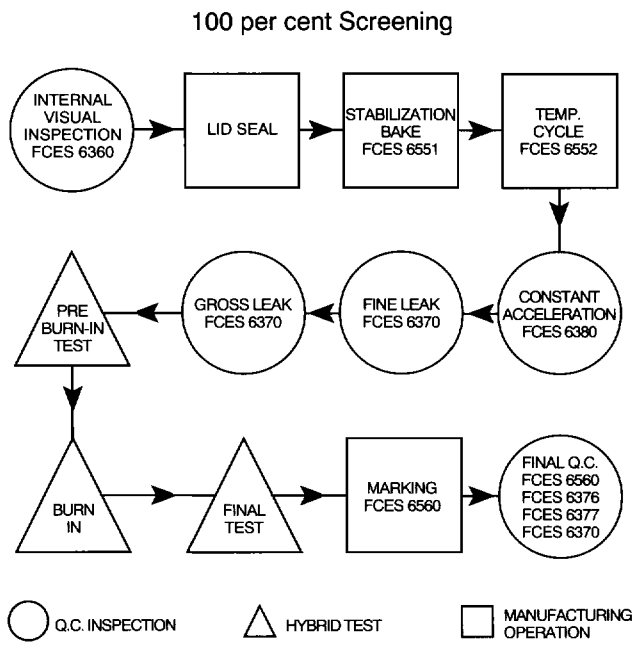


Fig. 8 Quality Conformance

All information contained herein is given in good faith, but unless we have given the user written confirmation of product suitability we can accept no liability regarding the particular application for which the product is intended.	C-MAC reserves the right to make changes to the product described in this data sheet to improve performance, reliability or manufacturability.	**Product Safety** Operation outside the stated ratings may result in premature failure or safety hazard. Product safety information is available on request.

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