XC3300A/L HardWire™ Array Family

Preliminary

Product Specification

Features

- Mask-programmed versions of Xilinx Programmable Logic Cell Arrays XC3000, XC3000A, XC3000L, XC3100, XC3100A
  - Cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - IEEE 1149.1-compatible boundry scan logic support
  - On-chip scan path test latches
  - High performance submicron CMOS process
- Easy conversion from Programmable FPGA
  - Architecturally identical to Programmable FPGA
  - Fully pin and performance compatible
  - Same specifications as Programmable FPGA
  - Supports daisy-chained configuration modes
  - Test program automatically generated
  - Emulates Programmable Configuration Signals
- Advanced Second Generation Architecture
  - Compatible arrays up to 9000 gate complexity
  - Extensive register, combinational and I/O capabilities
  - High fan-out signal distribution, low-slew clock
  - Internal 3-state bus capabilities
  - On-chip crystal oscillator amplifier

Description

The Xilinx XC3300A/L family of HardWire Arrays are mask programmed versions of the Xilinx XC3000A/L/XC3100A FPGAs. In high-volume applications where the design is stable, the programmable FPGAs used for prototyping and initial production can be replaced by their HardWire Array equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In a Programmable FPGA the logic functions and interconnections are determined by the configuration program data loaded and stored in internal static memory cells. The HardWire Array has architecture identical to the Programmable FPGA it replaces. All CLBs, IOBs, interconnect topology, power distribution and other elements are the same. In the HardWire Array the memory cells and the logic they control are replaced by metal connections. Thus the HardWire Array is a semicustom device manufactured to provide a customer specific function, yet is completely compatible with the FPGA it replaces.

Table 1. Summary of HardWire Product Availability For Each Member of the XC3000/XC3100 Families

HardWire Device	Replacement for Pin-Compatible Programmable Device	Maximum Speed Grade for HardWire Conversion*	Packages												
				PLCC			TQFP/VQFP				PQFP			PPGA	
			Number of Pins	44	68	84	64	100	144	176	100	160	208	132	175
XC3330A	XC3020A, XC3030A	-6	Number of I/Os	34	58	74	54	80	-	-	80	-	-	-	-
	XC3120, XC3130	-3		34	58	74	54	80	-	-	-	-	-	-	-
	XC3120A, XC3130A	-3		34	58	74	54	80	-	-	80	-	-	-	-
XC3330L	XC3020L, XC3030L	-8		34	58	74	54	80	-	-	-	-	-	-	-
XC3342A	XC3042A,	-6		-	-	74	-	82	120	-	82	-	-	-	-
	XC3142,	-3		-	-	74	-	82	120	-	82	-	-	-	-
	XC3142A	-3		-	-	74	-	82	120	-	82	-	-	-	-
XC3342L	XC3042L	-8		-	-	74	-	82	120	-	-	-	-	-	-
XC3390A	XC3064A, XC3090A	-6		-	-	70	-	-	120	144	-	138	144	110	144
	XC3164, XC3190	-3		-	-	70	-	-	120	144	-	138	144	110	144
	XC3164A, XC3190A	-3		-	-	70	-	-	120	144	-	138	144	110	144
XC3390L	XC3064L, XC3090L	-8		-	-	70	-	-	120	144	-	-	-	-	-

- FPGA and HardWire Device not available in this package

* Consult factory for information if faster speed grades are required.

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Xilinx manufactures the HardWire Array using the information from the FPGA design file. Since the HardWire array device is both pinout and architecturally identical with the FPGA it is easily created without the need for all the costly and time-consuming engineering activities which other semicustom solutions would require. No redesign time; no expensive and time consuming simulation runs; no place and route; no test vector generation. The combination of the Programmable array and HardWire Array products simply offer the fastest and easiest way to get your product to market, and ensures a subsequent low-cost, low-risk high-volume cost reduction path.

Electrical Characteristics

The XC3300, HardWire Array families are form, fit and function compatible with the XC3000/XC3100 FPGA families. Accordingly, all XC3300A, HardWire devices meet the electrical specifications of the respective XC3000/XC3100 FPGA device for the Speed Grade shown in Table 1. For specific data, please see the XC3000/XC3100 sections of the Xilinx Programmable Logic Data Book. Absolute Maximum Ratings, Operating Conditions, DC Characteristics and Switching Characteristics of the appropriate device type apply.

Architecture

As shown in Figure 1, the HardWire Array has the same architecture as the FPGA it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed circuit board traces connecting SSI/MSI packages.

The logic functions of the blocks are implemented by look-up tables. Functional options are implemented by user-defined multiplexers. Interconnecting networks between blocks are implemented with user-defined fixed metal connections.

See the *Xilinx Programmable Logic Data Book* for more information on Input/Output Blocks and Configuration Logic Blocks.

I/O Block

Each user-defined IOB provides an interface between the external package pin of the device and the internal user logic. The IOB is identical with that used in the FPGA. There are a wide variety of I/O options available to the user.

Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

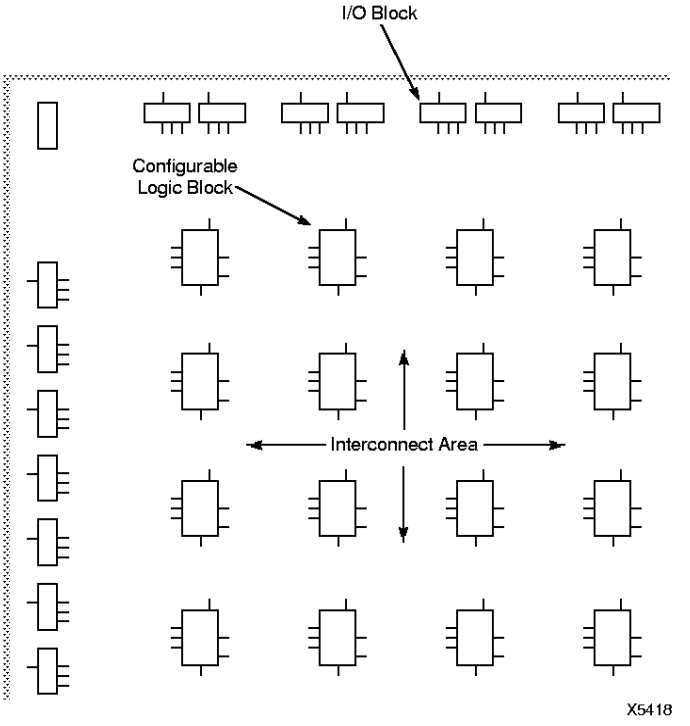


Figure 1. Logic Cell Array Structure

Configurable Logic Block

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3330A/L has 100 such blocks arranged in 10 rows and 10 columns.

The configurable logic block is identical to that used in the XC3000A/L family of FPGAs.

Interconnect

User-defined interconnect resources in the HardWire Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks. Interconnections between blocks are composed from a two-layer grid of metal segments. The XACT development system provides automatic routing of these interconnections. The inputs of the IOBs and CLBs are multiplexers that are defined to select an input network from the adjacent interconnect segments.

Three types of metal resources are provided to accommodate various network interconnect requirements:

- General Purpose Interconnect
- Direct Connection
- Long Lines

The topology of all these interconnect resources is identical with that of the FPGA, but the speed of the interconnect paths is significantly faster (since all interconnections are fixed metal connections).

Configuration and Start-Up

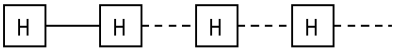
The HardWire Array devices are designed to be fully compatible with their Programmable array equivalents. While the HardWire Array parts do not require the loading of configuration data, they fully support a wide variety of configuration modes.

Configuration

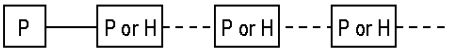
HardWire Array devices can be used stand-alone or in a daisy chain with other arrays. A HardWire Array device cannot act in Master Parallel or Peripheral Mode. However, designs which use these modes can be supported by selection of a mask option which forces the device into Master Mode. This allows the HardWire Array to be used when the original design used Peripheral Mode, without requiring any changes to the circuit board.

Example 1. As a stand alone HardWire Array.

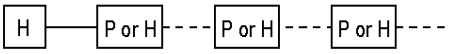
Example 2. As a daisy chain of all HardWire Arrays.



Example 3. As a HardWire Array or programmable slave in a daisy chain with a Programmable device as a master.



Example 4. As a HardWire Array device acting as a Serial Master with any combination of Programmable and HardWire Arrays as slaves.



(P = Programmable device, H = HardWire Array device)

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Figure 2.

An XC3300A/L HardWire Array device will not "swallow" its own configuration data. Whatever configuration bits are fed into the DIN pin will appear on the DOUT pin after a delay TDIO. In any case where a HardWire array device is ahead of a Programmable device in a daisy chain (as in example 3 and 4 shown in Figure 2) the configuration data will need to be modified.

Start-up Sequence

The HardWire Arrays are designed to emulate the start-up sequence of the FPGA devices as closely as possible, however, some differences do exist. The start-up sequence may be thought of as three stages: power-on-reset; internal clear; and configuration.

An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the array begin to operate, the device generates a POR (power-on reset) pulse. The I/O output buffers are disabled and a high-impedance pull-up resistor is provided for the user I/O pins. The length of the POR pulse is user-defined to be either 64 µs or 16 ms. The 64 µs pulse is used for a rapid reset cycle; the 16 ms pulse emulates the power-on sequence of a FPGA. If the M0 pin is held Low during the POR cycle (or if the mask option to force the HardWire Array into Master Mode is selected) the device will operate as a Master Mode device and the POR pulse will be extended to 4 times its nominal delay. This ensures that all daisy-chained slave devices will have sufficient time to power up.

Following the POR cycle, the HardWire Array enters a "clearing" state. This state emulates the configuration memory clear performed by a FPGA upon power-up. The length of the clear cycle is 256 cycles (nominally 256 µs) for a standard POR, but is only 2 cycles if the rapid reset cycle was selected.

At the completion of the clear cycle the RESET pin is sampled. If the RESET pin is being held Low, the "configuration" will be delayed (with the INIT pin held Low) until RESET is driven High. If the RESET pin is being driven High (or once it has been driven High following a delayed "configuration") the open drain INIT pin will be released and the value of the M0 pin will be latched. If the device is in Master Mode (M0 = Low) it will begin to produce CCLKs. If the device is in Slave Mode (M0 = High) it will require CCLKs to be supplied from another device. After 4 CCLK cycles the part is "configured" and the Done/Program (D/P) pin will be released. (If the device is in a daisy chain with the D/P pins tied together the D/P pin will remain Low until all devices have completed configuration.) One CCLK after the D/P pin goes High the I/Os will become active. The internal user-logic reset is user-defined to release either one CCLK cycle before or after the I/O pins become active. A HardWire Array operating in Master Mode will stop producing CCLKs one cycle after the I/Os become active.

INSTANT_ON

When the INSTANT_ON option is selected, the HardWire Array has a short POR delay of nominally 4 µs. If the RESET pin is not held Low, the array goes active within an additional 1 µs. The DONE pin goes High, the I/Os become active, and the internal global set/reset signal goes inactive, Holding the RESET pin Low delays start-up until it is released, at which time the device goes active within 8 µs. The CCLK pin is disabled during the entire power-up and start-up sequence.

3 V/5 V Considerations

The XC3300 HardWire Array can operate either as 5 voly only, or as a 3.3 volt device (part number XC3300L).

Table 2. 5 Volt and 3.3 Volt Operation

	5 Volt Operation				3.3 Volt Operation			
	Vil (max)	Vih (min)	Vol (max)	Voh (min)	Vil (max)	Vih (min)	Vol (max)	Voh (min)
XC3300	0.80	2.00	0.40	3.86*	0.80	2.00	0.40	2.40

* 3.76 volts for Industrial Grade

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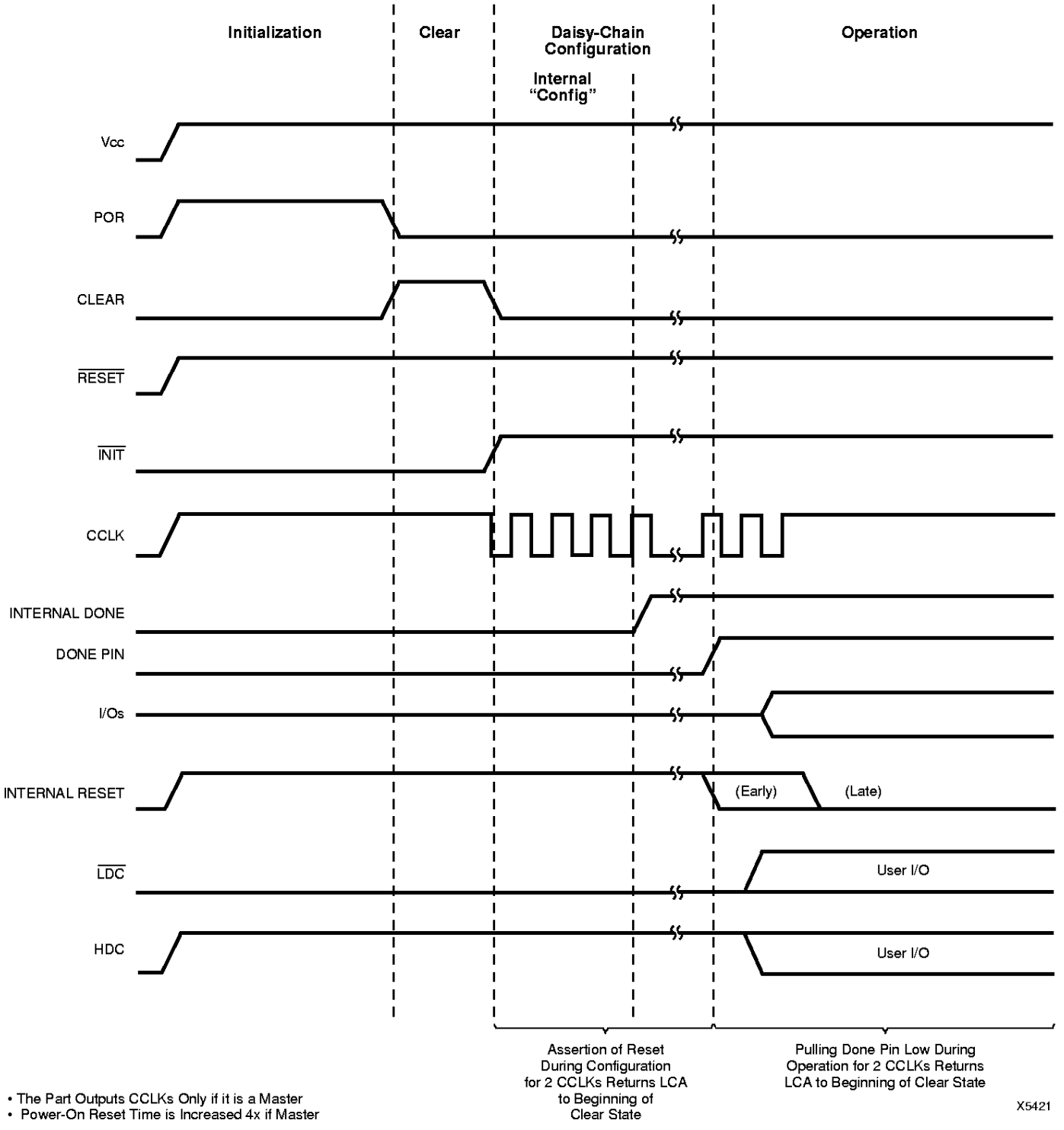

Figure 3. Psuedo-Configuration Waveform (Normal Power-Up)

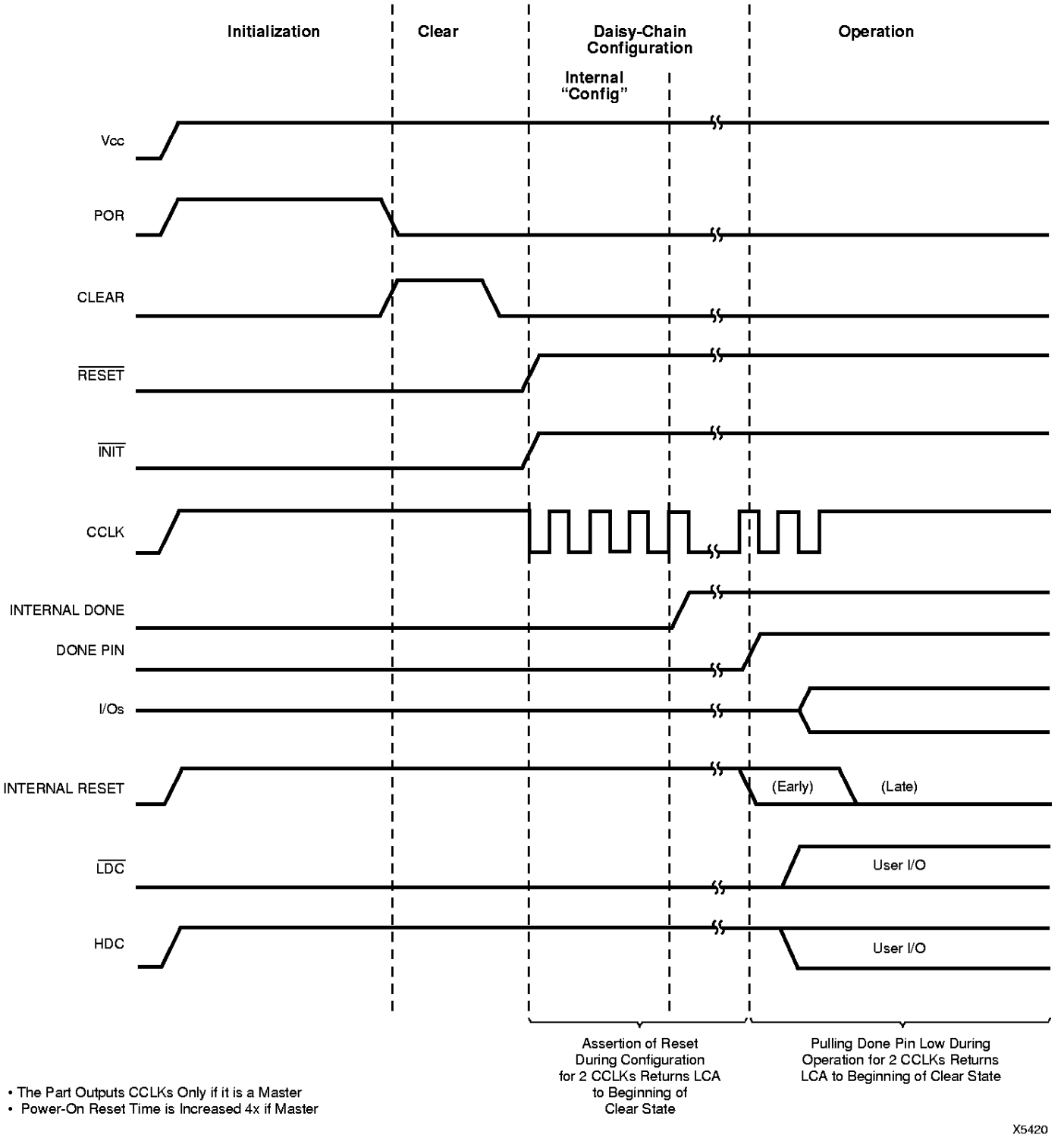

Figure 4. Psuedo-Configuration Waveform (Configuration Delay by Reset)

XC3300A/L Series Boundary-Scan Support:

The family supports IEEE 1149.1 compatible BYPASS, PRE-LOAD/SAMPLE and EXTEST Boundary-Scan instructions. Boundary-Scan is supported by a mask option selectable circuit built into the XC3300A/L family devices.

As more and more sophisticated assembly methods like surface mount technology become common place, Boundary-Scan can be used as a board level testing strategy where the traditional "bed of nails" testing is less appropriate. By using Boundary-Scan, test and design engineers can implement a test structure of a serial and/or parallel connections of a four-pin interface on any Boundary-Scan compatible IC. By scan methodology the user can easily load command and data into these devices to control the output drivers and sample the input signals.

The Boundary-Scan support logic is comprised of a 16-state, state machine, an instruction register and a number of data registers. A register operation begins with a "capture" where in a set of data is parallel loaded into the designated register for shifting out. The next state is "shift", where captured data are shifted out while the desired data are shifted in. States are provided for Wait operations. The last state of a register sequence is the update where the shifted content of the register is loaded into the appropriate instruction or data-holding register, either for instruction-register decode or for data-register pin control.

The primary data register is the Boundary-Scan register. Each IOB pin in the HardWire device includes three bits of shift register and three update latches for In, Out and 3-state control. Each Extest Capture captures all available input pins.

The other standard data register is the single flip-flop bypass register. It re-synchronizes data being passed through a device that need not be involved in the current scan operation.

The XC3300A/L family Boundary-Scan circuit is a mask option selected by the user. If Boundary-Scan is selected the user has the option of when it's enabled.

1) ALWAYS ENABLED: The Boundary-Scan pins are permanent. Boundary-Scan will be active and functional upon power-up. It will not wait for the DONE/PROGRAM pin to go high. The user can power up the device while holding the RESET pin low (delaying start-up) and still operate Boundary-Scan. However, dual function I/O pins such as: HDC, LDC, INIT and DOUT will stay in their "configuration" state until the device is in user-mode.
2) M1 pin controlled: The device will sample the M1 pin after the initialization state (at the same time it samples M0 pin to determine master/ slave configuration control). If the M1 pin is found to be in the "enable Boundary-Scan" mode (logic level to be determined by user as a mask option), the device will be in Boundary-Scan mode, and the Boundary-Scan pins will be enabled. When the M1 pin is driven to the opposite state, the Boundary-Scan pins will become user I/O. To reenter the Boundary-Scan mode, the user must "re-configure" the part (pull DONE/PROGRAM and RESET low) with the M1 pin driven to the "enable Boundary-Scan" state.

Unlike the XC4000 Boundary Scan pins, the TDI, TCK, TMS and TDO can be assigned to any user I/O by mask options. However, the dual function pins: HDC, LDC, INIT and DOUT cannot be used as Boundary-Scan pins due to circuit limitations.

The following instructions are supported in the XC3300A/L Boundary-Scan:

1) EXTEST
2) SAMPLE (only the I/O pad level is sampled)
3) BYPASS (The data shift register will not clock during the BYPASS instruction, unlike the XC4000)
4) 3-STATE (When this instruction is active, all user I/Os are 3-stated)

INTEST is not supported, and SAMPLE does not capture the values of internal nodes --only the I/O pad levels.

Three bits will be used to decode the four instructions, leaving room for extra, user-defined instructions. These extra instructions must be supported by "user-logic" JTAG circuitry that would co-exist with the regular design logic. By keeping the same pins for the JTAG circuit between the programmable design and the converted XC3300A/L design, a seamless transition between the two JTAG circuits can be achieved.

The four supported instructions are decoded as follows:

Instruction I2	I1	I0	Test selected	TDO source	I/O Data
0	0	0	EXTEST	Data Register	Data Register
0	0	1	SAMPLE	Data Register	Pin Logic
1	1	1	BYPASS	Bypass Register	Pin Logic
1	0	0	3-STATE		

In order to support Boundary-Scan during the design phase in which programmable XC3000A/L/XC3100A part are used, there will be a Boundary-Scan emulation circuit which will be available in an application note along with a sample .LCA file. By using this .LCA design file and reconfigurability, the user can put the design into Boundary-Scan test mode, run the tests then re-configure the device for user mode.

Performance

The XC3300A/L family of HardWire Arrays are manufactured in the same high-performance sub-micron CMOS technology as their FPGA equivalents. Traditionally the toggle frequency of a flip-flop has been used to describe the overall performance of a semi-custom device. The configuration used for determining this rate is shown in Figure 5.

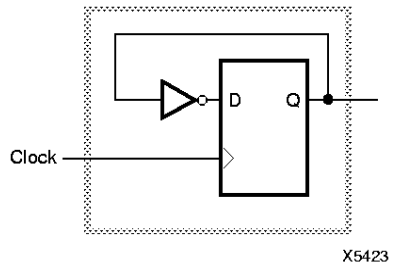

Figure 5. Toggle Flip-Flop. This is used to characterize device performance.

Actual array performance is determined by the timing of critical paths, including the timing for the logic and storage elements in that path and the timing of the associated interconnect. HardWire Array logic block performance is equal to or slightly faster than the equivalent FPGA, while the interconnect performance is significantly faster.

All HardWire Array devices are specified and tested for operation at the fastest equivalent FPGA speed available at the time the HardWire Array device is introduced.

Power

Power for the array is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the LCA, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. (See Figure 6.) An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4-mA loads under worst-case conditions may be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise. A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 500 pF per power/ground pin pair. For slew-rate limited outputs this total is four times larger.

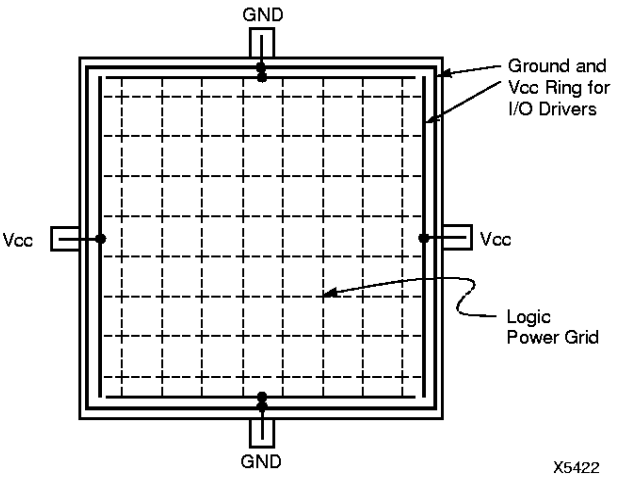

Figure 6. Array Power Distribution.

XC3300A Family Configuration Pin Assignments

CONFIGURATION MODE: <M0>												
SLAVE <1>	MASTER <0>	44 PLCC	68 PLCC	84 PLCC	100 PQFP	100 TQFP/ VQFP	132 PPGA	160 PQFP	176 TQFP	208 PQFP	175 PPGA	USER OPERATION
$\overline{\text{PWR DWN}}$	$\overline{\text{PWR DWN}}$	7	10	12	29	26	A1	159	1	3	B2	$\overline{\text{PWR DWN}}$ (I)
VCC	VCC	12	18	22	41	38	C8	20	23	26	D9	VCC
M1 (I)	M1 (I)	16	25	31	52	49	B13	40	45	48	B14	M1
M0 (HIGH) (I)	M0 (HIGH) (I)	17	26	32	54	51	B14	42	47	50	B15	M0 (I)
		18	27	33	56	53	D14	44	51	56	C15	I/O
HDC (HIGH)	HDC (HIGH)	19	28	34	57	54	G14	45	50	57	C15	I/O
LDC (LOW)	LDC (LOW)	20	30	36	59	56	H12	49	54	61	D16	I/O
$\overline{\text{INIT}}$ *	$\overline{\text{INIT}}$ *	22	34	42	65	62	M13	59	65	77	H15	I/O
GND	GND	23	35	43	66	63	P14	19	67	79	J14	GND
		26	43	53	67	73	N13	76	85	100	P15	XTL2 orI/O
$\overline{\text{RESET}}$ (I)	$\overline{\text{RESET}}$ (I)	27	44	54	78	75	P14	78	87	102	R15	$\overline{\text{RESET}}$ (I)
DONE	DONE	28	45	55	80	77	N13	80	89	107	R14	$\overline{\text{PROGRAM}}$ (I)
			46	56	81	78	M12	81	90	109	N13	I/O
		30	47	57	82	79	P13	82	91	110	T14	XTL1 or I/O
			48	58	83	80	N11	86	92	115	P12	I/O
			49	60	87	84	M9	92	93	122	T11	I/O
			50	61	88	85	N9	93	94	123	R10	I/O
			51	62	89	86	N8	98	95	128	R9	I/O
VCC	VCC	34	52	64	91	88	M8	100	110	130	N9	VCC
			53	65	92	89	N7	102	112	132	P8	I/O
			54	66	93	90	P6	103	113	133	R8	I/O
			55	67	94	91	M6	108	114	138	R7	I/O
			56	70	98	95	M5	114	115	145	R5	I/O
			57	71	99	96	N4	115	116	146	P5	I/O
DIN (I)	DIN (I)	38	58	72	100	97	N2	119	130	151	R3	I/O
DOUT	DOUT	39	59	73	1	98	M3	120	131	152	N4	I/O
CCLK (I)	CCLK	40	60	74	2	99	P1	121	132	153	R2	CCLK (I)
			61	75	5	2	M2	124	135	161	P2	I/O
			62	76	6	3	N1	125	136	162	M3	I/O
			63	77	8	5	L2	128	138	165	P1	I/O
			64	78	9	6	L1	129	139	166	N1	I/O
			65	81	12	9	K1	132	140	172	M1	I/O
			66	82	13	10	J2	133	141	173	L2	I/O
			67	83	14	11	H1	136	144	178	K2	I/O
			68	84	15	12	H2	137	145	179	K1	I/O
GND	GND	1	1	1	16	13	H3	139	154	182	J3	GND
			2	2	17	14	G2	141	156	184	H2	I/O
			3	3	18	15	G1	142	157	185	H1	I/O
			4	4	19	16	F2	147	158	192	F2	I/O
			5	5	20	17	E1	148	159	193	E1	I/O
			6	8	23	20	D1	151	162	199	D1	I/O
			7	9	24	21	D2	152	163	200	C1	I/O
			8	10	25	22	B1	155	164	203	E3	I/O
			9	11	26	26	C2	156	165	204	C2	I/O
		X	X	X	X	X						XC3330
				X	X	X						XC3342
				X			X	X	X	X	X	XC3390

Represents a 50-kΩ to 100-kΩ Pull-Up

* INIT is an Open Drain Output During Configuration

(I) Represents an Input

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Note: Pin assignments of "PGA Footprint" PLCC sockets and PGA packages are not electically identical.
Generic I/O pins are not shown

XC3300A/L Family Pin Assignments

Xilinx offers the three different array size in the XC3300 series in a variety of surface-mount and through-hole package types, with pin counts from 44 to 208.

Each chip is offered in several package types to accomodate the available PC board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without the need for PC board changes.

Note that there may not be a perfect match between the number of I/O pads on the chip and the number of pins on a package. In some cases, the chip has more I/O pads than there are pins on the package, as indicated below on the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

Table 3. Number of Available I/O pins

		Number of Package Pins												
	Max I/O	44	64	68	84	100	132	144	160	175	176	191	196	208
XC3330	80	34	54	58	74	80								
XC3342	96				74	82								
XC3390	144				70		110	120	138	144	144			144

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HardWire Array Testability

The HardWire Array products contain significant on-chip logic to facilitate manufacturability and testing. This logic, combined with Xilinx's internal Automatic Test Generation (ATG) software, assures 100% functionality. In fact, the HardWire Array can be 100% functionally tested by Xilinx without the need for customer generated test vectors (as is required with custom gate arrays).

This section examines the two basic block structures and the special test circuitry in the HardWire Array.

Test Architecture

The HardWire Array contains two types of internal blocks: the Input/Output Block (IOB) and the Configurable Logic Block (CLB). To accomplish 100% functional testing, special test circuitry is designed into the device. This circuitry allows testing of each block (CLB and IOB) in a synchronized procedure known as "Scan Test". Special dedicated test latches (called TBLKs) are included on all HardWire devices. They are completely transparent to the normal operation of the circuit. Scan testing allows the contents of all internal flip-flops to be serially shifted off-chip, and for Xilinx generated test vectors to be shifted into the device, thus enabling all flip-flops to be initialized to any desired state.

These special dedicated test latches are placed into each CLB and IOB. Each CLB has four internal test latches, (placed at the CLB outputs), while each IOB contains four test latches (placed at the IOB inputs) as shown in Figures 7 and 8. The placement of these test latches is very important, since each CLB output or IOB input can fanout to multiple destinations. All sources and destinations of logic blocks come from other logic blocks. Therefore, this placement of the latches provides complete access to all nets and synchronized control of all CLBs and IOBs.

The test latches are connected into a daisy chain which passes through every flip-flop in the array. Figure 9 shows an overview of the scan path. The path begins at the Scan In pin, sequences through each CLB, then through the IOBs, and finally exits at the Scan Out pin. This scan path can be seen in more detail in Figure 4, which shows the precise sequence with which the CLB and IOB internal test latches are loaded or read.

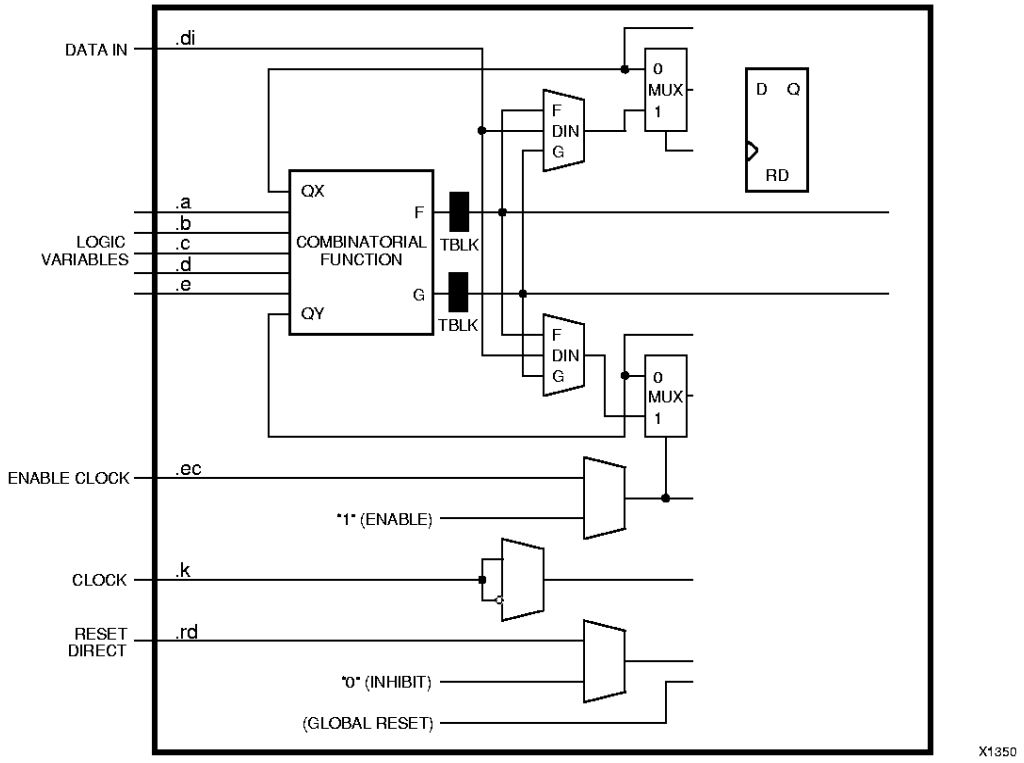

Figure 7. HardWire CLB Test Latch Locations

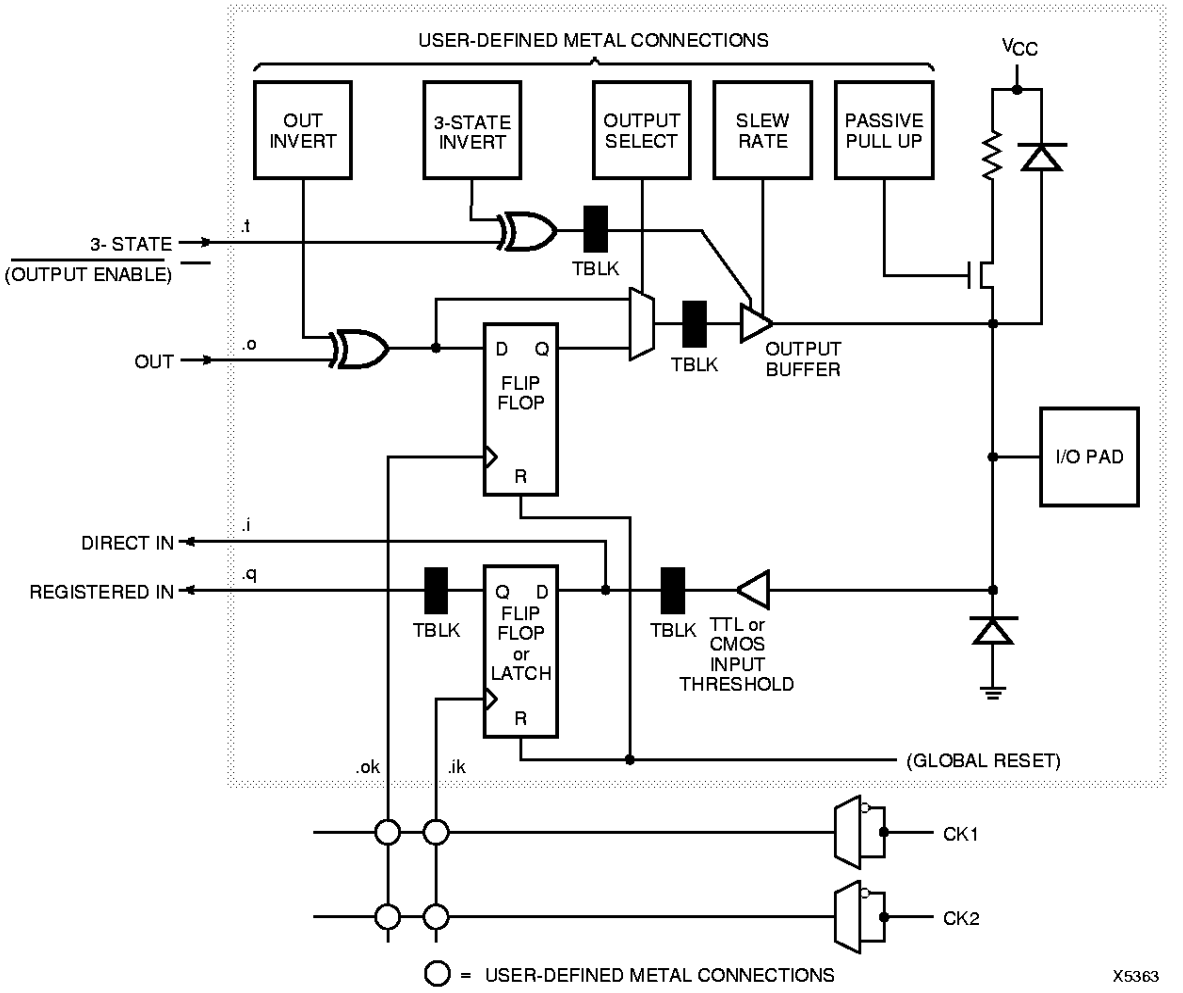

Figure 8. HardWire IOB Test Latch Location

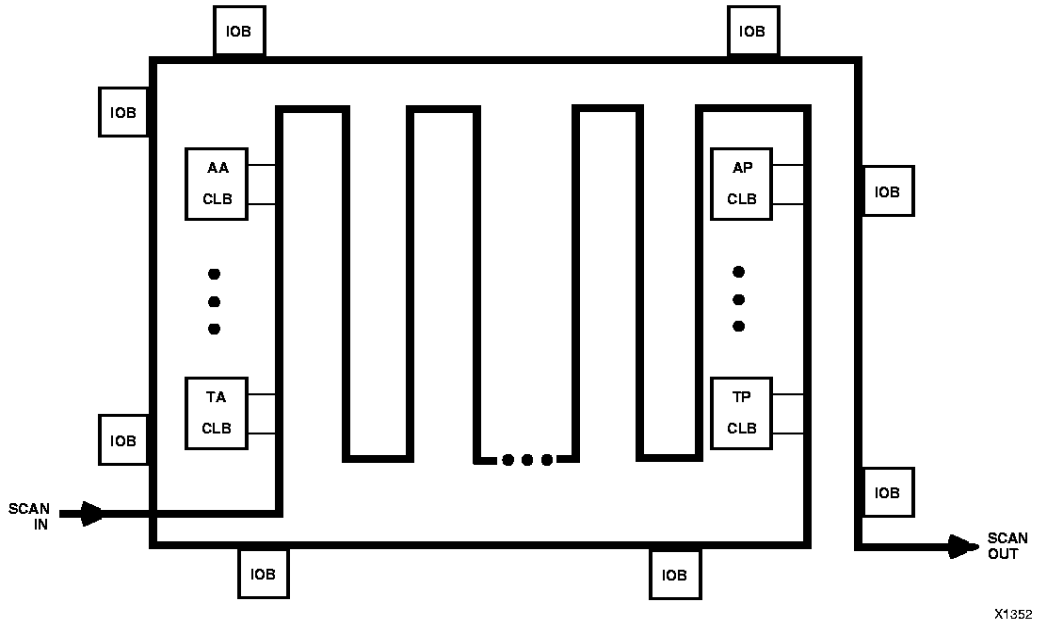

Figure 9. Scan Path Overview

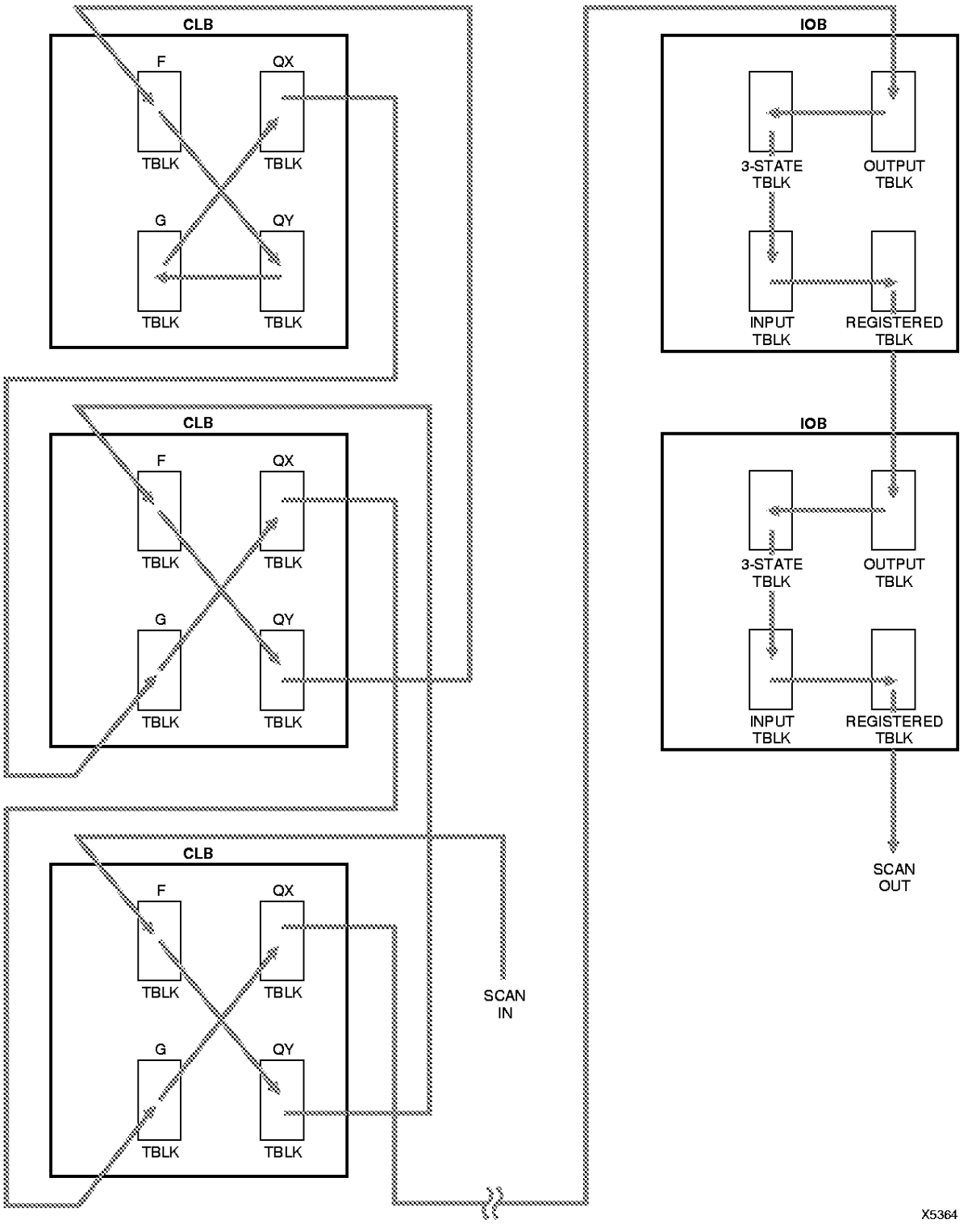

Figure 10. Detailed Scan Path

The internal architecture of a TBLK is shown in Figure 11. In the normal operation mode of the HardWire array, SW1 is in position A and all the test latches are bypassed completely. The HardWire array device is set into Test Mode (SW1 = position B) by Xilinx ATG software. This software inputs unique conditions on several control pins while serially loading a "password" into the device. For this reason, it is not possible for a customer design to inadvertently place the HardWire array into Test Mode. When SW1 is in position B (Test Mode) all the latches can receive data from either the CLB output or the previous latch in the daisy chain (SQn).

Synchronized together by a special test clock, all the test latches operate in two phases. The first phase serially loads all the latches to place a specific vector at the inputs of the logic block to be tested. The second phase is a parallel load of all latches, storing the expected output data of the logic block being tested (SW2 = A). At this point testing returns to phase one and serially clocks out the results, while simultaneously clocking in a new input vector.

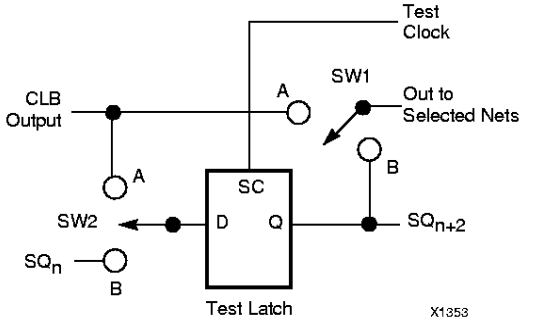

Figure 11. TBLK Block Diagram

Scan Test

To see how scan testing can be used to provide complete functional test coverage, consider the logic shown in Figure 12. This diagram shows a CLB (CLB2) with two inputs being driven by two different CLBs and the other two inputs being driven by two different IOBs. If we apply every possible combination of inputs to CLB2 and all expected output conditions are met, then CLB2 has been 100% functionally tested. The input conditions applied also include any register control signals (such as Clock, Reset, or Clock Enable). The same procedure is used for testing IOBs.

Looking again at Figure 12, CLB2 is tested by first serially loading the X output latches of CLB1 and CLB3 and the input latches of IOB1 and IOB2. Note that the latches on CLB2's outputs are also loaded in this first phase. Not all CLBs and IOBs can be tested at once, due to signal dependencies. To position the correct data into the latches all unused latches still need "don't cares" loaded. Regardless of which CLBs and IOBs are being tested by a particular scan vector, the complete scan path is always shifted in and out for testing and verification. The state of CLB2's output latches will be opposite to their expected results in phase two. This guarantees that CLB2's input data changed the state of its output latches and therefore, is current data.

CLB or IOB data registers using a synchronous or asynchronous clock are not a problem during this special test mode. All customer-used registers are clock inhibited during the phase one load. The inhibit of register clocking is accomplished by logically "ANDing" the register clocks with the global inhibit control line.

The test vectors needed to perform this thorough testing are created by Xilinx. No additional effort or engineering time is required from the user to ensure proper device performance. The customer design file used to create the HardWire Array is used in conjunction with specially developed Xilinx Automatic Test Generation software. This creates the complete set of test vectors required to perform 100% functional testing. This software creates the data for all possible input conditions and corresponding output data for each CLB and IOB used in the customer design. This data is then compiled into the test vectors used to perform the actual testing.

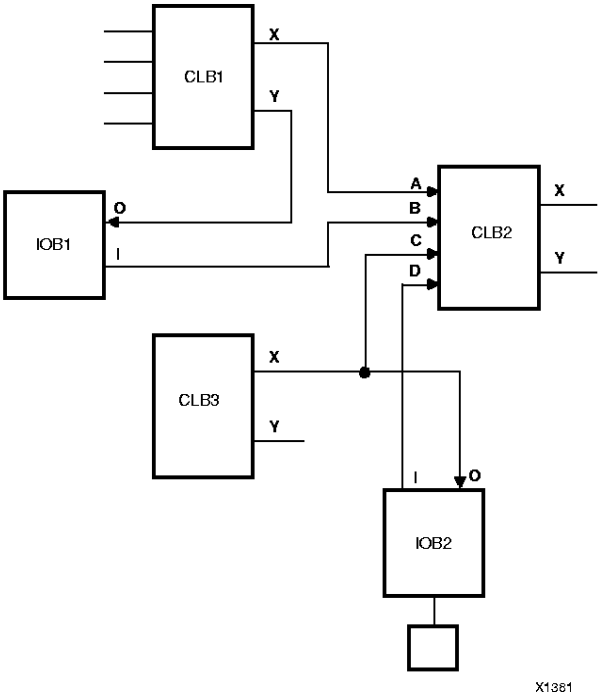

Figure 12. Four Input CLB (CLB2) Driven by Two Different CLB Outputs and Two different IOB Outputs

XC3300A/L Family
44-Pin PLCC Pinouts

Pin Number	XC3330A/L
1	**GND**
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	PWRDWN
8	TCLKIN-I/O
9	I/O
10	I/O
11	I/O
12	**VCC**
13	I/O
14	I/O
15	I/O
16	M1-RDATA
17	M0-RTRIG
18	M2-I/O
19	HDC-I/O
20	LDC-I/O
21	I/O
22	INIT-I/O

Pin Number	XC3330A/L
23	**GND**
24	I/O
25	I/O
26	XTL2(IN)-I/O
27	RESET
28	DONE-PGM
29	I/O
30	XT1(OUT)-BCLK-I/O
31	I/O
32	I/O
33	I/O
34	**VCC**
35	I/O
36	I/O
37	I/O
38	DIN-I/O
39	DOUT-I/O
40	CCLK
41	I/O
42	I/O
43	I/O
44	I/O

XC3330A/L Family 64-Pin Plastic VQFP Pinouts

Pin No.	XC3330A/L
1	I/O
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	**GND**
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	PWRDN
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	**VCC**
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-RDATA
32	M0-RTRIG

Pin No.	XC3330A/L
33	M2-I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	INIT-I/O
41	**GND**
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	XTAL2(IN)-I/O
48	RESET
49	DONE-PG
50	I/O
51	XTAL1(OUT)-BCLKN-I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	**VCC**
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	DIN-I/O
63	DOUT-I/O
64	CCLK

XC3330A/L, XC3342A/L Family
68-Pin and 84-Pin PLCC Pinouts

XC3330A/L, XC3342A/L	68 PLCC	84 PLCC
PWRDN	10	12
TCLKIN-I/O	11	13
I/O		14
I/O	12	15
I/O	13	16
I/O	—	17
I/O	14	18
I/O	15	19
I/O	16	20
I/O	17	21
VCC	18	22
I/O	19	23
I/O	—	24
I/O	20	25
I/O	21	26
I/O	22	27
I/O	—	28
I/O	23	29
I/O	24	30
M1	25	31
M0	26	32
I/O	27	33
HDC-I/O	28	34
I/O	29	35
LDC-I/O	30	36
I/O	31	37
I/O		38
I/O	32	39
I/O	33	40
I/O		41
INIT-I/O	34	42
GND	35	43
I/O	36	44
I/O	37	45
I/O	38	46
I/O	39	47
I/O	40	48
I/O	41	49
I/O		50
I/O		51
I/O	42	52
XTL2(IN)-I/O	43	53

XC3330A/L, XC3342A/L	68 PLCC	84 PLCC
RESET	44	54
DONE-PG	45	55
I/O	46	56
XTL1(OUT)-BCLKIN-I/O	47	57
I/O	48	58
I/O	—	59
I/O	49	60
I/O	50	61
I/O	51	62
I/O	—	63
VCC	52	64
I/O	53	65
I/O	54	66
I/O	55	67
I/O	—	68
I/O		69
I/O	56	70
I/O	57	71
DIN-I/O	58	72
DOUT-I/O	59	73
CCLK	60	74
I/O	61	75
I/O	62	76
I/O	63	77
I/O	64	78
I/O		79
I/O		80
I/O	65	81
I/O	66	82
I/O	67	83
I/O	68	84
GND	1	1
I/O	2	2
I/O	3	3
I/O	4	4
I/O	5	5
I/O		6
I/O		7
I/O	6	8
I/O	7	9
I/O	8	10
I/O	9	11

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of two different chips in two different packages. The first column lists 84 of the 118 pads on the XC3342A/L (and 84 of the 98 pads on the XC3330/L) that are connected to the 84 package pins. Six pads, indicated by a dash (–) in the 68 PLCC column, have no connections in the 68 PLCC package, but are connected in the 84-pin package.

XC3390A/L, Family
84-Pin PLCC Pinout

PLCC Pin Number	XC3390A/L
12	PWRDN
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	**GND***
22	**VCC**
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1
32	M0
33	I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	**VCC***
43	**GND**
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3390A/L
54	RESET
55	DONE-PG
56	I/O
57	XTL1(OUT)-BCLKIN-I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	**VCC**
65	**GND***
66	I/O*
67	I/O*
68	I/O*
69	I/O
70	I/O
71	I/O
72	DIN-I/O
73	DOUT-I/O
74	CCLK
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
1	**GND**
2	**VCC***
3	I/O*
4	I/O*
5	I/O*
6	I/O*
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed ouptuts are default slew-rate limited.

* Different pin definition than XC3342A/L PC84 package

XC3330A/L, XC3342A/L, Family
100-Pin PQFP, TQFP, VQFP Pinouts

TQFP/ VQFP Pin No.	PQFP Pin No.	XC3330A/L, XC3342A/L
13	16	**GND**
14	17	I/O
15	18	I/O
16	19	I/O
17	20	I/O
18	21	I/O
19	22	I/O
20	23	I/O
21	24	I/O
22	25	I/O
23	26	I/O
24	27	**VCC**
25	28	**GND**
26	29	PWRDN
27	30	TCLKIN-I/O
28	31	I/O**
29	32	I/O
30	33	I/O
31	34	I/O
32	35	I/O
33	36	I/O
34	37	I/O
35	38	I/O
36	39	I/O
37	40	I/O
38	41	**VCC**
39	42	I/O
40	43	I/O
41	44	I/O
42	45	I/O
43	46	I/O
44	47	I/O
45	48	I/O
46	49	I/O
47	50	I/O
48	51	I/O
49	52	M1
50	53	**GND**
51	54	M0
52	55	**VCC**
53	56	I/O
54	57	HDC-I/O
55	58	I/O
56	59	LDC-I/O
57	60	I/O
58	61	I/O
59	62	I/O
60	63	I/O
61	64	I/O
62	65	INIT-I/O
63	66	GND
64	67	I/O
65	68	I/O
66	69	I/O
67	70	I/O
68	71	I/O
69	72	I/O
70	73	I/O
71	74	I/O
72	75	I/O
73	76	XTAL2-I/O
74	77	**GND**
75	78	RESET
76	79	**VCC**
77	80	DONE-PG
78	81	I/O
79	82	BCLKIN-XTAL1-I/O
80	83	I/O
81	84	I/O
82	85	I/O
83	86	I/O
84	87	I/O
85	88	I/O
86	89	I/O
87	90	I/O
88	91	**VCC**
89	92	I/O
90	93	I/O
91	94	I/O
92	95	I/O
93	96	I/O
94	97	I/O
95	98	I/O
96	99	I/O
97	100	DIN-I/O
98	1	DOUT-I/O
99	2	CCLK
100	3	**VCC**
1	4	**GND**
2	5	I/O
3	6	I/O
4	7	I/O**
5	8	I/O
6	9	I/O
7	10	I/O
8	11	I/O
9	12	I/O
10	13	I/O
11	14	I/O
12	15	I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs.
Programmed outputs are default slew-rate limited.

This table describes the pinouts of two different chips in two different packages. The third column lists 100 of the 118 pads on the XC3342A/L that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3x30x, which has 98 pads; therefore the corresponding pins have no connections.

XC3390A/L, Family
132-Pin Plastic PGA Pinout

PGA Pin Number	XC3390A/L	PGA Pin Number	XC3390A/L	PGA Pin Number	XC3390A/L	PGA Pin Number	XC3390A/L
C4	**GND**	B13	M1	P14	RESET	M3	DOUT-I/O
A1	PWRDN	C11	**GND**	M11	**VCC**	P1	CCLK
C3	I/O-TCLKIN	A14	M0	N13	DONE-PG	M4	**VCC**
B2	I/O	D12	**VCC**	M12	I/O	L3	**GND**
B3	I/O	C13	I/O	P13	XTAL1-I/O-BCLKIN	M2	I/O
A2	I/O	B14	HDC-I/O	N12	I/O	N1	I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	I/O	K3	I/O
A3	I/O	D13	I/O	M10	I/O	L2	I/O
A4	I/O	D14	LDC-I/O	P11	I/O	L1	I/O
B5	I/O	E13	I/O	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	I/O	K1	I/O
B6	I/O	F13	I/O	N9	I/O	J2	I/O
A6	I/O	F14	I/O	P9	I/O	J1	I/O
B7	I/O	G13	I/O	P8	I/O	H1	I/O
C7	**GND**	G14	INIT-I/O	N8	I/O	H2	I/O
C8	**VCC**	G12	**VCC**	P7	I/O	H3	**GND**
A7	I/O	H12	**GND**	M8	**VCC**	G3	**VCC**
B8	I/O	H14	I/O	M7	**GND**	G2	I/O
A8	I/O	H13	I/O	N7	I/O	G1	I/O
A9	I/O	J14	I/O	P6	I/O	F1	I/O
B9	I/O	J13	I/O	N6	I/O	F2	I/O
C9	I/O	K14	I/O	P5	I/O	E1	I/O
A10	I/O	J12	I/O	M6	I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	I/O	L14	I/O	P4	I/O	D1	I/O
C10	I/O	L13	I/O	P3	I/O	D2	I/O
B11	I/O	K12	I/O	M5	I/O	E3	I/O
A12	I/O	M14	I/O	N4	I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	I/O
A13	I/O	M13	XTAL2(IN)-I/O	N3	I/O	C2	I/O
C12	I/O	L12	**GND**	N2	DIN-I/O	D3	**VCC**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3342A/L, Family
144-Pin Plastic TQFP Pinouts

Pin Number	XC3342A/L
1	PWRDN
2	I/O-TCLKIN
3	–
4	I/O
5	I/O
6	–
7	I/O
8	I/O
9	–
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	–
16	I/O
17	I/O
18	**GND**
19	**VCC**
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	–
29	I/O
30	I/O
31	–
32	–
33	I/O
34	–
35	I/O
36	M1
37	**GND**
38	MO
39	**VCC**
40	I/O
41	HDC-I/O
42	I/O
43	I/O
44	I/O
45	LDC-I/O
46	–
47	I/O
48	I/O

Pin Number	XC3342A/L
49	I/O
50	–
51	I/O
52	I/O
53	INIT-I/O
54	**VCC**
55	**GND**
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	–
64	–
65	I/O
66	I/O
67	I/O
68	I/O
69	XTL2(IN)-I/O
70	**GND**
71	RESET
72	**VCC**
73	DONE-PG
74	D7-I/O
75	XTL1(OUT)-BCLKIN-I/O
76	I/O
77	I/O
78	D6-I/O
79	I/O
80	–
81	I/O
82	I/O
83	–
84	I/O
85	I/O
86	–
87	–
88	I/O
89	I/O
90	**VCC**
91	**GND**
92	I/O
93	I/O
94	–
95	–
96	I/O

Pin Number	XC3342A/L
97	I/O
98	I/O
99	–
100	I/O
101	–
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	CCLK
109	**VCC**
110	**GND**
111	/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	–
122	–
123	I/O
124	I/O
125	–
126	**GND**
127	**VCC**
128	I/O
129	I/O
130	–
131	–
132	–
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	**VCC**
144	**GND**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3390A/L, Family
160-Pin PQFP Pinout

PQFP Pin Number	XC3390A/L
1	I/O
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	**GND**
20	**VCC**
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	M1
41	**GND**
42	M0
43	**VCC**
44	I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	LDC-I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	INIT-I/O
60	**VCC**
61	**GND**
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	XTAL2-I/O
77	**GND**
78	RESET
79	**VCC**
80	DONE/PG
81	I/O
82	XTAL1-I/O-BCLKIN
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	**VCC**
101	**GND**
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	DIN-I/O
120	DOUT
121	CCLK
122	**VCC**
123	**GND**
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	**GND**
140	**VCC**
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O
157	**VCC**
158	**GND**
159	PWRDWN
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs.
Programmed IOBs are default slew-rate limited.

XC3390A/L, Family
175-Pin Plastic PGA Pinout

PGA Pin Number	XC3390A/L
B2	PWRDN
D4	TCLKIN-I/O
B3	I/O
C4	I/O
B4	I/O
A4	I/O
D5	I/O
C5	I/O
B5	I/O
A5	I/O
C6	I/O
D6	I/O
B6	I/O
A6	I/O
B7	I/O
C7	I/O
D7	I/O
A7	I/O
A8	I/O
B8	I/O
C8	I/O
D8	**GND**
D9	**VCC**
C9	I/O
B9	I/O
A9	I/O
A10	I/O
D10	I/O
C10	I/O
B10	I/O
A11	I/O
B11	I/O
D11	I/O
C11	I/O
A12	I/O
B12	I/O
C12	I/O
D12	I/O
A13	I/O
B13	I/O
C13	I/O
A14	I/O

PGA Pin Number	XC3390A/L
D13	I/O
B14	M1
C14	**GND**
B15	M0
D14	**VCC**
C15	I/O
E14	HDC-I/O
B16	I/O
D15	I/O
C16	I/O
D16	LDC-I/O
F14	I/O
E15	I/O
E16	I/O
F15	I/O
F16	I/O
G14	I/O
G15	I/O
G16	I/O
H16	I/O
H15	INIT-I/O
H14	**VCC**
J14	**GND**
J15	I/O
J16	I/O
K16	I/O
K15	I/O
K14	I/O
L16	I/O
L15	I/O
M16	I/O
M15	I/O
L14	I/O
N16	I/O
P16	I/O
N15	I/O
R16	I/O
M14	I/O
P15	XTAL2(IN)-I/O
N14	**GND**
R15	RESET
P14	**VCC**

PGA Pin Number	XC3390A/L
R14	DONE-PG
N13	I/O
T14	XTAL1(OUT)-BCLKIN-I/O
P13	I/O
R13	I/O
T13	I/O
N12	I/O
P12	I/O
R12	I/O
T12	I/O
P11	I/O
N11	I/O
R11	I/O
T11	I/O
R10	I/O
P10	I/O
N10	I/O
T10	I/O
T9	I/O
R9	I/O
P9	I/O
N9	**VCC**
N8	**GND**
P8	I/O
R8	I/O
T8	I/O
T7	I/O
N7	I/O
P7	I/O
R7	I/O
T6	I/O
R6	I/O
N6	I/O
P6	I/O
T5	I/O
R5	/O
P5	I/O
N5	I/O
T4	I/O
R4	I/O
P4	I/O

PGA Pin Number	XC3390A/L
R3	DIN-I/O
N4	DOUT-I/O
R2	CCLK
P3	**VCC**
N3	**GND**
P2	I/O
M3	I/O
R1	I/O
N2	I/O
P1	I/O
N1	I/O
L3	I/O
M2	I/O
M1	I/O
L2	I/O
L1	I/O
K3	I/O
K2	I/O
K1	I/O
J1	I/O
J2	I/O
J3	**GND**
H3	**VCC**
H2	I/O
H1	I/O
G1	I/O
G2	I/O
G3	I/O
F1	I/O
F2	I/O
E1	I/O
E2	I/O
F3	I/O
D1	I/O
C1	I/O
D2	I/O
B1	I/O
E3	I/O
C2	I/O
D3	**VCC**
C3	**GND**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs.
Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected.
Pin A1 does not exist.

XC3390A/L, Family
176-Pin TQFP Pinouts

Pin Number	XC3390A/L
1	PWRDWN
2	TCLKIN-I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	**GND**
23	**VCC**
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	–

Pin Number	XC3390A/L
45	M1
46	**GND**
47	M0
48	**VCC**
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	–
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	INIT-I/O
66	**VCC**
67	**GND**
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	–
83	–
84	I/O
85	XTAL2(IN)-I/O
86	**GND**
87	RESET
88	**VCC**

Pin Number	XC3390A/L
89	DONE-PG
90	I/O
91	XTAL1(OUT)-BCLKIN-I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	**VCC**
111	**GND**
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	CCLK

Pin Number	XC3390A/L
133	**VSS**
134	**GND**
135	I/O
136	I/O
137	–
138	I/O
139	I/O
140	I/O
141	I/O
142	–
143	–
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	**GND**
155	**VCC**
156	I/O
157	I/O
158	I/O
159	I/O
160	–
161	–
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	–
169	I/O
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	**VCC**
176	**GND**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3390A/L, Family
208-Pin PQFP Pinouts

Pin Number	XC3390A/L
1	–
2	GND
3	PWRDWN
4	TCLKIN-I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	–
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	**GND**
26	**VCC**
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	–
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	M1-RDATA
49	**GND**
50	M0-RTRIG
51	–
52	–
53	–
54	–
55	**VCC**
56	M2-I/O
57	HDC-I/O
58	I/O
59	I/O
60	I/O
61	LDC-I/O
62	I/O
63	I/O
64	–
65	–
66	–
67	–
68	I/O
69	I/O
70	I/O
71	I/O
72	–
73	–
74	I/O
75	I/O
76	I/O
77	I/O
78	**VCC**
79	**GND**
80	I/O
81	I/O
82	I/O
83	–
84	–
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	–
91	–
92	–
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	XLT2-I/O
101	**GND**
102	RESET
103	–
104	–
105	–
106	**VCC**
107	D/P
108	–
109	D7-I/O
110	XLT1-BCLKIN-I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	D6-I/O
116	I/O
117	I/O
118	I/O
119	–
120	I/O
121	I/O
122	D5-I/O
123	CS0-I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	D4-I/O
129	I/O
130	**VCC**
131	**GND**
132	D3-I/O
133	CS1-I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	D2-I/O
139	I/O
140	I/O
141	I/O
142	–
143	I/O
144	I/O
145	I/O
146	BUSY-RDY-RCLK-I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	DIN-D0-I/O
152	DOUT-I/O
153	CCLK
154	**VCC**
155	–
156	–
157	–
158	–
159	–
160	**GND**
161	WS-A0-I/O
162	CS2-A1-I/O
163	I/O
164	I/O
165	A2-I/O
166	A3-I/O
167	I/O
168	I/O
169	–
170	–
171	–
172	A15-I/O
173	A4-I/O
174	I/O
175	I/O
176	–
177	–
178	A14-I/O
179	A5-I/O
180	I/O
181	I/O
182	**GND**
183	**VCC**
184	A13-I/O
185	A6-I/O
186	I/O
187	I/O
188	–
189	–
190	I/O
191	I/O
192	A12-I/O
193	A7-I/O
194	–
195	–
196	–
197	I/O
198	I/O
199	A11-I/O
200	A8-I/O
201	I/O
202	I/O
203	A10-I/O
204	A9-I/O
205	**VCC**
206	–
207	–
208	–