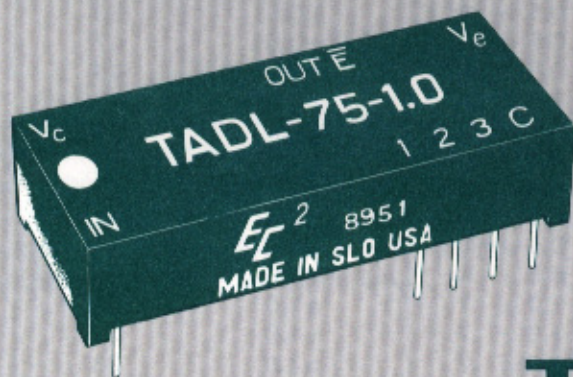# EC-2

low profile

DIP

TRIMMABLE
ANALOG DELAY LINE

- ● Analog input and output
- ● All delays digitally programmable
- ● Delays stable and precise
- ● 24-pin DIP package (.260 high)
- ● Available in delays up to 260.5ns
- ● Available in 40 delay times with trimming resolution from .5 to 1.5ns

the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 1.5 million hours. The design includes internal termination; no additional external components are needed to obtain the required delay.

These Trimmable Analog Delay Lines are digitally programmable by the presence of either a T^2L "1" or a "0" at each of the programming pins. Since the input and the output terminals are fixed and the programming is accomplished only by DC voltage levels, programming may be accomplished by remote switching or permanent termination of the appropriate programming pins; the Delay Line may also be programmed automatically by computer generated data. MUX set-up time is 24ns typical.

design notes

The ''DIP Series'' of Trimmable Analog Delay Lines developed by Engineered Components Company have been designed to allow for final delay adjustment during or after installation in a circuit. These Trimmable Analog Delay Lines incorporate required control circuitry to pick-off analog signals, and are contained in a 24-pin DIP package. These modules are of hybrid construction utilizing

The TADL is offered in 40 models with time delays to a maximum of 260.5ns and with trimming step resolution as shown in the Part Number Table. Programming of final delay is accomplished in 8 delay steps in accordance with the Truth Table examples shown on page 3. Tolerances on minimum delay, delay change per step and deviation from programmed delay are shown in the Part Number Table on page 3.
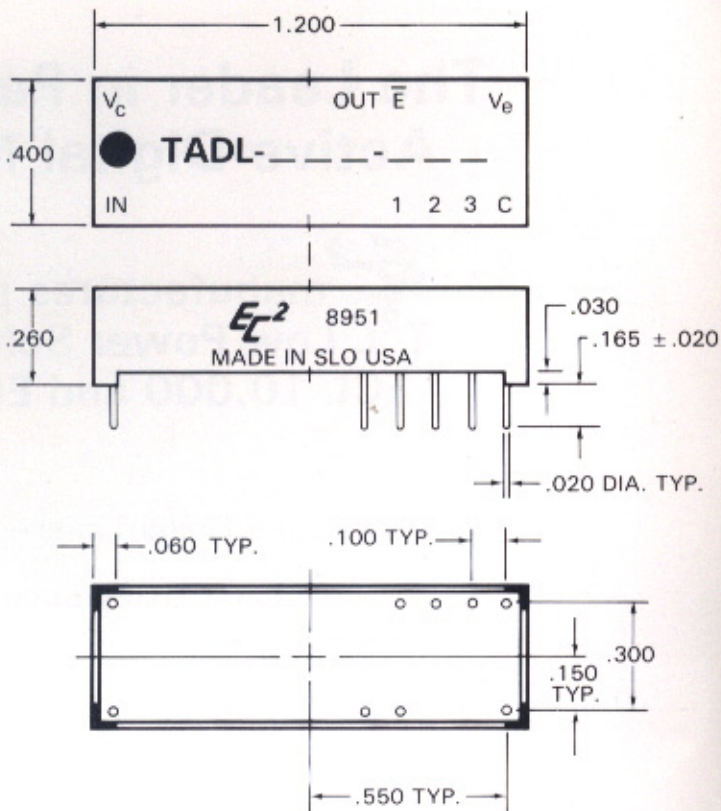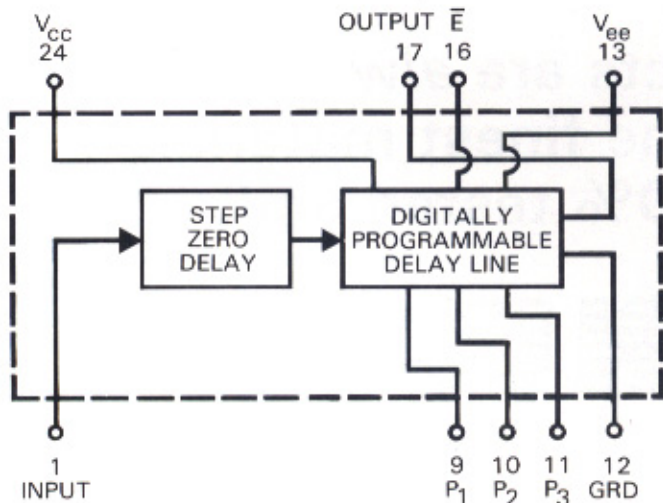
DESIGN NOTES (Continued)

Delay time is measured at the 0 volt level on the leading edge. Temperature coefficient of delay is less than 100 ppm/°C over the operating temperature range of −40 to +85°C.

The TADL is designed for use with analog input signals between −5 and +5 volts and will reproduce them at the output without inversion. Input impedance is 100 ±10 ohms. Output impedance is 170 ohms typical. The −3dB bandwidth is given in the Part Number Table on page 3. In general, shorter delays will correspond to increased line bandwidth.

These "DIP Series" Trimmmable Analog Delay Lines are packaged in a 24-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F and are fully encapsulated in epoxy resin. Leads meet the solderability requirements of MIL-STD-202, Method 208. Corner standoffs on the housing provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

Marking consists of manufacturer's name, logo (EC²), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

MECHANICAL DETAIL IS SHOWN BELOW

TEST CONDITIONS

1. All measurements are made at 25°C.
2. V_{cc} supply voltage is maintained at 5.0V DC.
3. V_{ee} supply voltage is maintained at −5.0V DC.
4. Units with a step zero fixed delay of up to 100ns are tested with a 10Mhz sine wave. Units with a step zero fixed delay of greater than 100ns are tested with a 7Mhz sine wave.
5. Output is loaded with 100K ohms to ground.

OPERATING SPECIFICATIONS

*V_{cc} supply voltage:	4.75 to 5.25V DC
*V_{ee} supply voltage:	−2.0 to −5.25V DC
V_{ee} to V_{cc} voltage:	10.0V DC max.
Supply current:	< 1 ma typical
Input impedance:	100 ohms ±10%

Programming and enable pins:

High level input voltage	2.0V min.
Low level input voltage:	0.8V max.
Input leakage current	1 ua max.
Operating temperature range:	−40 to +85°C.
Storage temperature:	−55 to +125°C.

*For proper operation of the delay line, analog input voltages should not exceed the V_{ee} or V_{cc} supplies.

BLOCK DIAGRAM IS SHOWN BELOW

PART NUMBER TABLE

Part Number	*Step Zero Delay Time	Maximum Delay Time (Nom)	Delay Change Per Step	** Maximum Deviation From Programmed Delay	− 3dB Bandwidth in Mhz
TADL-5.0-0.5	5.0 ± .5	8.5	0.5 ± .4	± 0.5	50
TADL-7.5-0.5	7.5 ± .6	11.0	0.5 ± .4	± 0.5	47
TADL-10.0-0.5	10.0 ± .7	13.5	0.5 ± .4	± 0.5	44
TADL-12.5-0.5	12.5 ± .8	16.0	0.5 ± .4	± 0.5	41
TADL-15.0-0.5	15.0 ± .9	18.5	0.5 ± .4	± 0.5	38
TADL-17.5-0.5	17.5 ± 1.0	21.0	0.5 ± .4	± 0.5	36
TADL-20.0-0.5	20.0 ± 1.1	23.5	0.5 ± .4	± 0.5	34
TADL-22.5-0.5	22.5 ± 1.2	26.0	0.5 ± .4	± 0.5	32
TADL-25.0-0.5	25.0 ± 1.3	28.5	0.5 ± .4	± 0.5	30
TADL-27.5-0.5	27.5 ± 1.4	31.0	0.5 ± .4	± 0.5	28
TADL-30-1.0	30 ± 1.5	37	1.0 ± .7	± 1.0	26
TADL-35-1.0	35 ± 1.5	42	1.0 ± .7	± 1.0	24
TADL-40-1.0	40 ± 2.0	47	1.0 ± .7	± 1.0	23
TADL-45-1.0	45 ± 2.0	52	1.0 ± .7	± 1.0	22
TADL-50-1.0	50 ± 2.5	57	1.0 ± .7	± 1.0	21
TADL-55-1.0	55 ± 2.5	62	1.0 ± .7	± 1.0	20
TADL-60-1.0	60 ± 2.5	67	1.0 ± .7	± 1.0	19
TADL-65-1.0	65 ± 3.0	72	1.0 ± .7	± 1.0	18
TADL-70-1.0	70 ± 3.0	77	1.0 ± .7	± 1.0	18
TADL-75-1.0	75 ± 3.0	82	1.0 ± .7	± 1.0	17
TADL-80-1.0	80 ± 3.0	87	1.0 ± .7	± 1.0	17
TADL-85-1.0	85 ± 4.0	92	1.0 ± .7	± 1.0	16
TADL-90-1.0	90 ± 4.0	97	1.0 ± .7	± 1.0	15
TADL-95-1.0	95 ± 4.0	102	1.0 ± .7	± 1.0	15
TADL-100-1.5	100 ± 4.0	110.5	1.5 ± 1.0	± 1.5	14
TADL-110-1.5	110 ± 4.5	120.5	1.5 ± 1.0	± 1.5	14
TADL-120-1.5	120 ± 4.5	130.5	1.5 ± 1.0	± 1.5	13
TADL-130-1.5	130 ± 5.0	140.5	1.5 ± 1.0	± 1.5	13
TADL-140-1.5	140 ± 5.0	150.5	1.5 ± 1.0	± 1.5	12
TADL-150-1.5	150 ± 5.5	160.5	1.5 ± 1.0	± 1.5	12
TADL-160-1.5	160 ± 5.5	170.5	1.5 ± 1.0	± 1.5	11
TADL-170-1.5	170 ± 6.0	180.5	1.5 ± 1.0	± 1.5	11
TADL-180-1.5	180 ± 6.5	190.5	1.5 ± 1.0	± 1.5	10
TADL-190-1.5	190 ± 7.0	200.5	1.5 ± 1.0	± 1.5	10
TADL-200-1.5	200 ± 7.5	210.5	1.5 ± 1.0	± 1.5	9.0
TADL-210-1.5	210 ± 8.0	220.5	1.5 ± 1.0	± 1.5	9.0
TADL-220-1.5	220 ± 8.5	230.5	1.5 ± 1.0	± 1.5	8.0
TADL-230-1.5	230 ± 9.0	240.5	1.5 ± 1.0	± 1.5	8.0
TADL-240-1.5	240 ± 9.5	250.5	1.5 ± 1.0	± 1.5	7.0
TADL-250-1.5	250 ± 10.0	260.5	1.5 ± 1.0	± 1.5	7.0

Table caption: φ DELAYS AND TOLERANCES (in ns)

TRUTH TABLE EXAMPLES

Part Number \ Programming Pins	3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
TADL-10-0.5		10	.5	1	1.5	2	2.5	3	3.5
TADL-50-1.0		50	1	2	3	4	5	6	7
TADL-100-1.5		100	1.5	3	4.5	6	7.5	9	10.5
ETC.									

* Delay at step zero is referenced to the input pin.

** All delay times after step zero are referenced to step zero.

φ Special modules can be readily manufactured to improve accuracies and/or provide customer specified delay times for specific applications.

Catalog No. C/121589