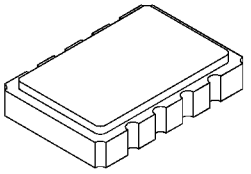
SC0015B
550.00 MHz Differential Sine-Wave Clock

- *Quartz SAW Frequency Stability*
- *Fundamental Fixed Frequency*
- *Very Low Jitter and Power Consumption*
- *Rugged, Miniature, Surface-Mount Case*
- *Low-Voltage Power Supply (5.0 VDC)*



SMC-8 Case

This digital clock is designed for use with high-speed CPUs and digitizers. Fundamental-mode oscillation is made possible by surface-acoustic-wave (SAW) technology. The design results in low jitter, compact size, and low power consumption. Differential outputs provide a sine wave that is capable of driving 50 Ω loads.

Electrical Characteristics

Characteristic		Sym	Notes	Minimum	Typical	Maximum	Units
Output Frequency	Absolute Frequency	f_O	1, 2	549.89		550.1	MHz
	Tolerance from 550.000 MHz	Δf_O				±200	ppm
Q and $\overline{Q}$ Output	Voltage into 50Ω (VSWR ≤ 1.2)	V_O	1, 3	0.60		1.1	V_{P-P}
	Operating Load VSWR					2:1	
	Symmetry		3, 4, 5	49		51	%
	Harmonic Spurious		3, 4, 6			-30	dBc
	Nonharmonic Spurious					-60	dBc
Q and $\overline{Q}$ Period Jitter	No Noise on V_{CC}		3, 4, 6, 7		15	30	ps_{P-P}
	200 mV_{P-P} from 1 MHz to ½ f_O on V_{CC}		3, 4, 7, 8			35	ps_{P-P}
Output (Disabled)	Amplitude into 50 Ω		3, 9			75	mV_{P-P}
Output DC Resistance (between Q & $\overline{Q}$)			3	50			KΩ
ENABLE (Terminal 14)	Input HIGH Voltage	V_{IH}	3, 9	V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
	Input LOW Voltage	V_{IL}		0.0		0.20	V
	Input HIGH Current	I_{IH}			3	5	mA
	Input LOW Current	I_{IL}				-1	mA
	Propagation Delay	t_{PD}				1	ms
DC Power Supply	Operating Voltage	V_{CC}	1, 3	4.75	5.0	5.25	VDC
	Operating Current	I_{CC}			20	40	mA
Operating Ambient Temperature		T_A	1, 3	0		+70	°C
Lid Symbolization (YY = Year, WW = Week)		RFM SC0015B 550.00 MHz YYWW					

CAUTION: Electrostatic Sensitive Device. Observe precautions for handling.

Notes:

1. Unless otherwise noted, all specifications include any combination of load VSWR, VCC, and TA. In addition, Q and $\overline{Q}$ are terminated into 50 Ω loads to ground. (See: Typical Test Circuit.)
2. One or more of the following United States patents apply: 4,616,197; 4,670,681; 4,760,352.
3. The design, manufacturing process, and specifications of this device are subject to change without notice.
4. Only under the nominal conditions of 50 Ω load impedance with VSWR ≤ 1.2 and nominal power supply voltage.
5. Symmetry is defined as the pulse width (in percent of total period) measured at the 50% points of Q or $\overline{Q}$. (See: Timing Definitions.)
6. Jitter and other spurious outputs induced by externally generated electrical noise on V_{CC} or mechanical vibration are not included. Dedicated external voltage regulation and careful PCB layout are recommended for optimum performance.
7. Applies to period jitter of Q and $\overline{Q}$. Measurements are made with the Tektronix CSA803 signal analyzer with at least 1000 samples.
8. Period jitter measured with a 200 mV_{P-P} sine wave swept from 1 MHz to one-half of f_O at the V_{CC} power supply terminal.
9. The outputs are enabled when Terminal 8 is at logic HIGH. Propagation delay is defined as the time from the 50% point on the rising edge of ENABLE to the 90% point on the rising edge of the output amplitude or as the fall time from the 50% point to the 10% point. (SEE: Timing Definitions.)

RF Monolithics, Inc. Phone: (972) 233-2903 Fax: (972) 387-8148 E-mail: info@rfm.com
RFM Europe Sales Phone: (33-0) (1) 39.16.42.89 Fax: (33-0) (1) 39.16.42.70 http://www.rfm.com