GOULD

AMI Semiconductors

CMOS Single Chip μ-Law/A-Law Synchronous Combo Codecs with Filters

Industrial Temperature

S3506I/S3507I/S3507AI

Features

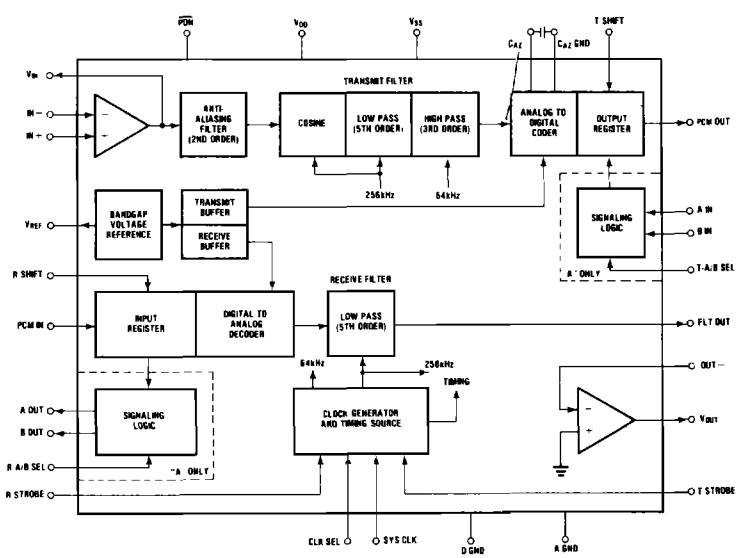
- ☐ Independent Transmit and Receive Sections With 75dB Isolation
- ☐ Low Power CMOS 80mW (Operating) 10mW (Standby)
- ☐ Stable Voltage Reference On-Chip
- ☐ Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- ☐ Input Analog Filter Eliminates Need for External Anti-Aliasing Prefilter
- ☐ Input/Output Op Amps for Programming Gain
- ☐ Output Op Amp Provides ±3.1V into a 600Ω Load or Can Be Switched Off for Reduced Power (70mW)
- ☐ Special Idle Channel Noise Reduction Circuitry for Crosstalk Suppression
- ☐ Encoder has Dual-Speed Auto-Zero Loop for Fast Acquisition on Power-up
- ☐ Low Absolute Group Delay = 450μsec @ 1kHz

General Description

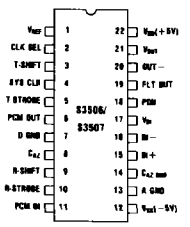
The S3506 and S3507 are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analog↔digital conversion circuits that conform to the desired transfer characteristic. The S3506 provides the European A-Law companding and the S3507 provides the North American μ-Law companding characteristic.

Modems, Filters & PCM Products

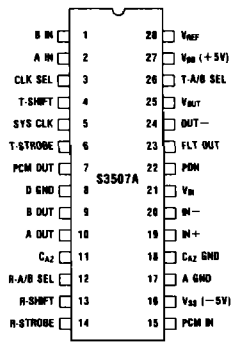
Block Diagram



Pin Configuration (22 Pin)



Pin Configuration (28 Pin)



General Description (Continued)

These circuits provide the interface between the analog signals of the subscriber loop and the digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ±5V.

For a sampling rate of 8kHz, PCM input/output data rate can vary from 64kb/s to 2.1Mb/s. Separate transmit/receive timing allows synchronous or time-slot asynchronous operation.

In 22-pin cerdip or ceramic packages (.400" centers) the S3506/S3507 are ideally suited for PCM applications: Exchange, PABX, or Digital Telephone as well as fiber optic and other non-telephone uses. A 28-pin version, the S3507A, provides standard μ-Law A/B signaling capability. These devices are also available in a 28-pin chip carrier.

Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+ 6.0V
DC Supply Voltage V_{SS}	− 6.0V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to + 150°C
Power Dissipation at 25°C	1000mW
Digital Input	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$
Analog Input	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$

Electrical Operating Characteristics (T_A = −46° to 90°C)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{DD}	Positive Supply	4.75	5.0	5.25	V	
V_{SS}	Negative Supply	−4.75	−5.0	−5.25	V	
P_{OPR}	Power Dissipation (Operating)		80	140	mW	
P_{OPR}	Power Dissipation (Operating w/o Output Op Amp		70		mW	V_{DD} = 5.0V
P_{STBY}	Power Dissipation (Standby)		10	25	mW	V_{DD} = −5.0V

AC Characteristics: (Refer to Figures 3A and 4A)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
D_{SYS}	System Clock Duty Cycle	40	50	60	%	
f_{SC}	Shift Clock Frequency	0.064		2.048	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}	Shift Clock to Strobe (On) Delay	−100	0	200	ns	
t_{sw}	Strobe Width	600ns		124.3μs	@2.048 MHz	700ns min @1.544MHz

AC Characteristics (Continued) (Refer to Figures 3A and 4A)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{cd}	T-Shift Clock to PCM OUT Delay		100	150	ns	100pF, 510Ω Load
t_{dc}	R-Shift Clock to PCM IN Set-Up Time	60			ns	
t_{rd}	PCM Output Rise Time $C_L = 100pF$		50	100	ns	to 3V; 510Ω to V_{DD}
t_{fd}	PCM Output Fall Time $C_L = 100pF$		50	100	ns	to .4V; 510Ω to V_{DD}
t_{dss}	A/B Select to Strobe Trailing Edge Set-up Time	100			ns	

DC Characteristics: (V_{DD} = +5V, V_{SS} = −5V)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{INA}	Analog Input Resistance IN+, IN−	100			KΩ	
C_{IN}	Input Capacitance to Ground		7	15	pF	All Logic and Analog Inputs
	R-Shift Clock, T-Shift Clock, PCM IN, System Clock, Strobe, $\overline{PDN}$					
I_{INL}	Logic Input Low Current			1	μA	V_{IL} = 0.8V
I_{INH}	Logic Input High Current			1	μA	V_{IH} = 2.0V
	T-A/B SEL, A IN, B IN, R-A/B SEL					
I_{INL}	Logic Input Low Current			600	μA	V_{IL} = 0.8V
I_{INH}	Logic Input High Current			600	μA	V_{IH} = 2.0V
V_{IL}	Logic Input "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.0			V	
V_{OL}	Logic Output "Low" Voltage (PCM Out)			0.4	V	510Ω Pull-up to V_{DD} + 2 LSTTL
V_{OL}	Logic Output "Low" Voltage (A/B OUT)			0.4	V	I_{OL} = 1.6mA
V_{OH}	Logic Output "High" Voltage	2.4			V	I_{OH} = 40μA
R_L	Output Load Resistance V_{OUT}	600			Ω	

Transmission Delays

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Encoder		125		μs	From T_{STROBE} to the Start of Digital Transmitting
	Decoder	30	8T + 25		μs	T = Period in μs of R_{SHIFT} CLOCK
	Transmit Section Filter			182	μs	@1kHz
	Receive Section Filter			110	μs	@1kHz

S3507/S3507A Single-Chip μ-Law Filter/Codec Performance

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
ICN_W	Idle Channel Noise (Weighted Noise)			−85	−66.5	dBm0p	CCITT G.712 4.1
ICN_{SF}	Idle Channel Noise (Single Frequency Noise)				−60	dBm0	CCITT G.712 4.2
ICN_R	Idle Channel Noise (Receive Section)				−74	dBm0p	CCITT G.712 4.3
	Spurious Out-of-Band Signals at Channel Output				−28	dBm0	CCITT G.712 6.1
IMD_{2F}	Intermodulation (2 Tone method)				−35	dBm	CCITT G.712 7.1
IMD_{PF}	Intermodulation (1 Tone + Power Frequency)				−49	dBm	CCITT G.712 7.2
	Spurious In-Band Signals at the Channel Output Port				−40	dBm0	CCITT G.712 9
	Interchannel Crosstalk $V_{IN} - V_{OUT}$		75	80		dB	CCITT G.712 11
$V_{IN(Max)}$	Max Coding Analog Input Level			±3.1		V_{0pk}	
V_{OUT} (Max)	Max Coding Analog Output Level			±3.1		V_{0pk}	$R_L = 600\Omega$
AD	Absolute Delay End-to-End @ 1KHz			450	500	μsec	@ 0dBm0
ED	Envelope Delay Distortion	500 to 600Hz		200	750	μsec	Relative to Minimum Delay Frequency
		600 to 1000Hz		120	375	μsec	
		1000Hz to 2600Hz		110	125	μsec	
		2600Hz to 2800Hz		160	750	μsec	
SD	Signal to Total Distortion	0 to −30dBm0	33.5	39		dB	Method 2 - Sine-wave Signal Used
		−40dBm0	27.5	31		dB	
		−45dBm0	22.5	26		dB	
FR	Frequency Response 300Hz to 3000Hz				±.25	dB	
GT	Gain Tracking with Input Level Variations (End-to-End. Each half channel is one half this value.)			±0.2 ±0.4 ±1.0	±0.5 ±1.0 ±3.0	dB	+3 to −40 dBm0 −45 to −50 dBm0 −55dBm0
ΔG	Gain Variation with Temperature and Power Supply Variation			±0.25		dB	
	Transmit Gain Repeatability			±0.1	±0.2	dB	
	Receive Gain Repeatability			±0.1	±0.2	dB	
$OTLP_R$	Zero Transmission Level Point (Decoder See Figure 1)			1.51		VRMS	V_{OUT} Digital Milliwatt Response
$OTLP_T$	Zero Transmission Level Point (Encoder See Figure 1)			1.51		VRMS	V_{IN} to Yield Same as Digital Milliwatt Response at Decoder

S3507/S3507A Single-Chip μ-Law Filter/Codec Performance

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
ICN_W	Idle Channel Noise (Weighted Noise)			5	−66.5	dBm0	
ICN_{SF}	Idle Channel Noise (Single Frequency Noise)				−60	dBm0	
ICN_R	Idle Channel Noise (Receive Section)				−74	dBm0	
	Spurious Out-of-Band Signals at the Channel Output				−28	dBm0	
$OTLP_T$	Zero Transmission Level Point (Encoder See Figure 1)			1.51		VRMS	V_{IN} to Yield Same as Digital Milliwatt Response at Decoder
$OTLP_R$	Zero Transmission Level Point (Decoder See Figure 1)			1.44		VRMS	V_{OUT} Digital Milliwatt Response
AD	Absolute Delay End-to-End @ 1KHz			450	500	μsec	@ 0dBm0
ED	Envelope	500 to 600Hz		200	750	μsec	Relative to
	Delay	600 to 1000Hz		120	375	μsec	Minimum
	Distortion	1000Hz to 2600Hz		110	125	μsec	Delay
		2600Hz to 2800Hz		160	750	μsec	Frequency
SD	Signal to	0 to −30dBm0	33.5	39		dB	
	Total	−40dBm0	27.5	31		dB	
	Distortion	−45dBm0	22.5	26		dB	
FR	Frequency Response 300Hz to 3000Hz				±.25	dB	
IMD_{2F}	Intermodulation (2 Tone method)				−35	dBm	
IMD_{PF}	Intermodulation (1 Tone + Power Frequency)				−49	dBm	
	Spurious In-Band Signals at the Channel Output Port				−40	dBm0	
	Interchannel Crosstalk $V_{IN}-V_{OUT}$		75	80		dB	
$V_{IN(Max)}$	Max Coding Analog Input Level			±3.1		V_{0pk}	
$V_{OUT(Max)}$	Max Coding Analog Output Level			±3.1		V_{0pk}	$R_L = 600\Omega$
GT	Gain Tracking with Input Level Variations (End-to-End. Each Half Channel is One Half of this Value.)			±0.2	±0.5	dB	+3 to −40 dBm0
				±0.4	±1.0	dB	−45 to −50 dBm0
				±1.0	±3.0	dB	−55 dBm0
△G	Gain Variation with Temperature and Power Supply Variation			±0.25		dB	
	Transmit Gain Repeatability			±0.1	±0.2	dB	
	Receive Gain Repeatability			±0.1	±0.2	dB	

Pin/Function Descriptions

Pin	S3506/S3507	S3507A	Description
SYS CLK	4	5	**System Clock**—This pin is a TTL compatible input for a 256kHz, 1.544MHz, 2048MHz, or 1.536MHz clock that is divided down to provide the filter clocks. The status of CLK SEL pin must correspond to the provided clock frequency.
T-SHIFT	3	4	**Transmit Shift Clock**—This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
R-SHIFT	9	13	**Receive Shift Clock**—This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
T-STROBE	5	6	**Transmit Strobe**—This TTL compatible pulse input (8kHz) is used for analog sampling and for initiating the PCM output from the coder. It must be synchronized with the T-SHIFT clock with its positive going edges occurring with the positive edge of the shift clock. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
R-STROBE	10	14	**Receive Strobe**—This TTL compatible pulse input (8kHz) initiates clocking of PCM input data into the decoder. It must be synchronized with the R-SHIFT clock with its positive going edges occurring with the positive edge of the shift clock. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
CLK SEL	2	3	**Clock Select**—This pin selects the proper divide ratios to utilize either 256kHz, 1.544MHz, 2.048MHz, or 1.536MHz as the system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz, to V_{SS} (−5V) for 1.544MHz or 1.536MHz operation, or to D GND for 256kHz operation.
PCM OUT	6	7	**PCM Output**—This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of T-SHIFT clock signal following a positive edge of the T-STROBE input. Data is clocked out by the positive edge of the T-SHIFT clock into one 510Ω pull-up per system plus 2 LS-TTL inputs.
PCM IN	11	15	**PCM Input**—This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of T-SHIFT clock.
C_{AZ} C_{AZ} GND	8 14	11 18	**Auto Zero**—A capacitor of 0.1μF ±20% should be connected between these pins for coder auto zero operation. Sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
V_{REF}	1	28	**Voltage Reference**—Output of the internal band-gap reference voltage (≈−3.075V) generator is brought out to V_{REF} pin. Do not load this pin.
IN+ IN− V_{IN}	15 16 17	19 20 21	These pins are for analog input signals in the range of $-V_{REF}$ to $+V_{REF}$. IN− and IN+ are the inputs of a high input impedance op amp and V_{IN} is the output of this op amp. These three pins allow the user complete control over the input stage so that it can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel. V_{IN} should not be loaded by less than 47K ohms.
FLT OUT	19	23	**Filter Out**—This is the output of the low pass filter which represents the recreated analog signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 47K ohms, or the Digital MilliWatt response will fall off slightly.

Pin/Function Descriptions (Continued)

Pin	S3506/S3507	S3507A	Description
OUT –	20	24	These two pins are the output and input of the uncommitted output amplifier stage. Signal at the FLT OUT pin can be connected to this amplifier to realize a low output impedance with unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel. The V_{OUT} pin has the capability of driving 0dBm into a 600Ω load. (See Figure 1). If OUT – is connected directly to V_{SS} the op amp will be powered down, reducing power consumption by 10mW, typically.
V_{OUT}	21	25	
V_{DD}	22	27	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins, repectively (typ. +5V, –5V). V_{DD} should be applied first.
V_{SS}	12	16	
A GND	13	17	Analog and digital ground pins are separate for minimizing crosstalk.
D GND	7	8	
$\overline{PDN}$	18	22	**Power Down**—This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high or low, but as long as they are static, the powered down mode is in effect. Should be tied to +5 when not used.
A IN		2	The transmit A/B select input selects the A signal input on a positive transition and the B signal input on the negative transition. These inputs are TTL compatible. The A/B signaling bits are sent in bit 8 of the PCM word in the frame following the frame in which T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronized to the T-STROBE input in each device.
B IN		1	
T-A/B SEL		26	
A OUT		10	In the decoder the A/B signaling bits received in the PCM input word are latched to the respective outputs in the same frame in which the R-AB SEL input makes a transition. A bit is latched on a positive transition and B bit is latched on a negative transition. A common A/B select input can be used for all channels in a multiplex operation.
B OUT		9	
R-A/B SEL		12	

Functional Description

The simplified block diagram of the S3506/S3507 appears on page one. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. A bandgap voltage generator supplies the reference level for the conversion process.

Transmit Section

Input analog signals first enter the chip at the uncommitted op amp terminals. This op amp allows gain trim to be used to set 0TLP in the system. From the V_{IN} pin the signal enters the 2nd order analog antialiasing filter. This filter eliminates the need for any offchip filtering as it provides attenuation of 34dB (typ.) at 256kHz and 46dB (typ.) at 512Hz. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 256kHz, followed by a 3rd Order High-Pass Filter clocked at 64kHz. The resulting band-pass characteristics meet the CCITT G.711, G.712 and G.733 specifications. Some representative attenuations are >26dB (typ) from 0 to 60Hz and >35dB (typ) from 4.6kHz to 100kHz. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The polarity of the incoming signal selects the appropriate polarity of the reference voltage. The successive approximation analog-to-digital conversion process requires 9½ clock cycles, or about 72μs. A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

The PCM data word is formatted according to the μ-law companding curve for the S3507 with the sign bit and the ones complement of the 7 magnitude bits according to the AT&T D3 specification. In the S3506 the PCM data word is formatted according to the A-Law companding curve with alternate mark inversion (AMI), meaning that the even bits are inverted per CCITT specifications.

Included in the circuitry of the S3507/S3507A is "All Zero" code suppression so that negative input signal values between decision value numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronization by T1 line clock recovery circuitry as there are never more than 15 consecutive zeros. The 8-bit PCM data is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz.

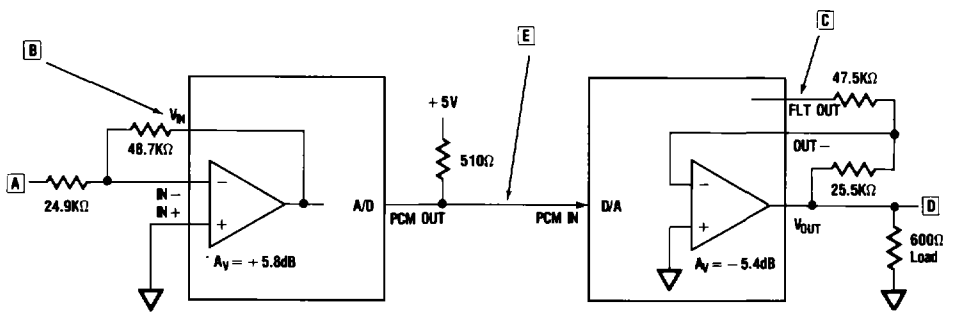
Idle Channel Noise Suppression

An additional feature of the CODEC is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of the chip is such that for 250msec. the only code words generated were +0, −0, +1, or −1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation, resetting the 250msec. timer. This feature is a form of Idle Channel Noise or Crosstalk Suppression. It is of particular importance in the S3506 A-Law version because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz to 2.048MHz, clocks the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 256kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 47kΩ. When used in this fashion the low impedance output amp can be switched off for a savings in power consumption. When it is required to drive a 600Ω load the output is configured as shown in Figure 1 allowing gain trimming as well as impedance matching. With this configuration a transmission level of 0dBm can be delivered into the load with the +3.14dB or +3.17dB overload level being the maximum expected level.

Figure 1. S3507 Input/Output Reference Signal Levels



The resistors are illustrated for a 0dBm IN/0dBm OUT system. Point [A] bridges a 600Ω termination and Point [D] drives a 600Ω load (illustrated). The 0dBm level produces the equivalent digital milliwatt code at Point [E] as defined in the AT&T and CCITT specifications for PCM. This is called the zero transmission level point or OTLP and 3.17dB of overload capability remains before saturation occurs.

	[A]	[B]	[C]	[D]	[E]
Voltage for OTLP	.775VRMS 1.10Vpk	1.51VRMS 2.13Vpk	1.44VRMS 2.04Vpk	.775VRMS 1.10Vpk	Digital Milliwatt Code per AT&T/CCITT
Voltage for Saturation	1.12VRMS 1.58Vpk	2.17VRMS 3.075Vpk	2.07VRMS 2.93Vpk	1.12VRMS 1.58Vpk	Saturation Codes

Power Down Logic

Powering down the CODEC can be done in several ways. The most direct is to drive the PDN pin to a low level. Stopping both the transmit strobe and the receive strobe will also put the chip into the stand-by mode. The strobes can be held high or low.

Voltage Reference Circuitry

A temperature compensated band-gap voltage generator (−3.075V) provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed during assembly to ensure a minimum gain error of ±0.2dB due to all causes. The V_{REF} pin should not be connected to any load.

Power Supply and Clock Application

For proper operation V_{DD} and V_{SS} should be applied simultaneously. If not possible, then V_{SS} should be applied first. To avoid forward-biasing the device the clock voltages should not be applied before the power supply voltages are stable. When cards must be plugged into a "hot" system it may be necessary to install 1000Ω current-limiting resistors in series with the clock lines to prevent latch-up.

Timing Requirements

The internal design of the Single-Chip CODEC paid careful attention to the timing requirements of various systems. In North America, central office and channelbank designs follow the American Telephone and Telegraph Company's T1 Carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Yet, in digital telephone designs, CODEC's may be used in a non-multiplexed form with a data rate as low as 64kb/s. The S3507 and S3507A fill these requirements.

In Europe, telephone exchange and channelbank designs follow the CCITT carrier PCM format to multiplex 30 voice channels at a data rate of 2.048Mb/s. The S3506 is designed for this market and will also handle PABX and digital telephone applications requiring the A-Law transfer characteristics.

The timing format chosen for the AMI Codec allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kb/s to 2.048Mb/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows the variable data rate capability. Additionally, the S3506/S3507 does not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe, forcing the PCM output in a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and transmit/receive shift clocks are synchronized to it. Figure 2 shows the waveforms in typical multiplexed uses of the CODEC.

System Clock

The basic timing of the Codec is provided by the system clock. This 2.048MHz, 1.544MHz, or 256kHz clock is divided down internally to provide the various filter clocks and the timing for the conversions. In most systems this clock will also be used as the shift clock to clock in and out the data. However, the shift clock can actually be between 64kHz and 2.048MHz as long as one of the system clock frequencies is provided. Independent strobes and shift clocks allow asynchronous time slot operation of transmit and receive. The 3507 will also operate with a 1.536MHz system clock, as used in some PABX systems, with the CLK SEL pin in the 1.544MHz Mode.

Signaling in μ-Law Systems

The S3506 and S3507 are compact 22-pin devices to meet the two worldwide PCM standards. In μ-Law systems there can be a requirement for signaling information to be carried in the bit stream with the coded analog data. This coding scheme is sometimes called 7-5/6 bit rather than 8 bit because the LSB of every 6th frame is replaced by a signaling bit. This is referred to as A/B Signaling and if a signaling frame carries the "A" bit, then 6 frames later the LSB will carry the "B" bit. To meet this requirement, the S3507A is available in a 28-pin dip package, or in a 28-pin chip carrier, as 6 more pins are required for the inputs and outputs of the A/B signaling.

Pin Configuration—S3507A 28-Lead Chip Carrier

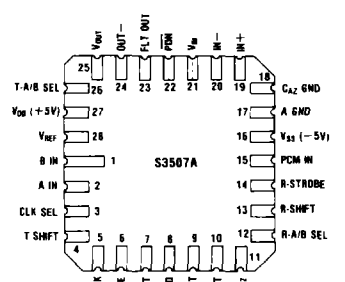
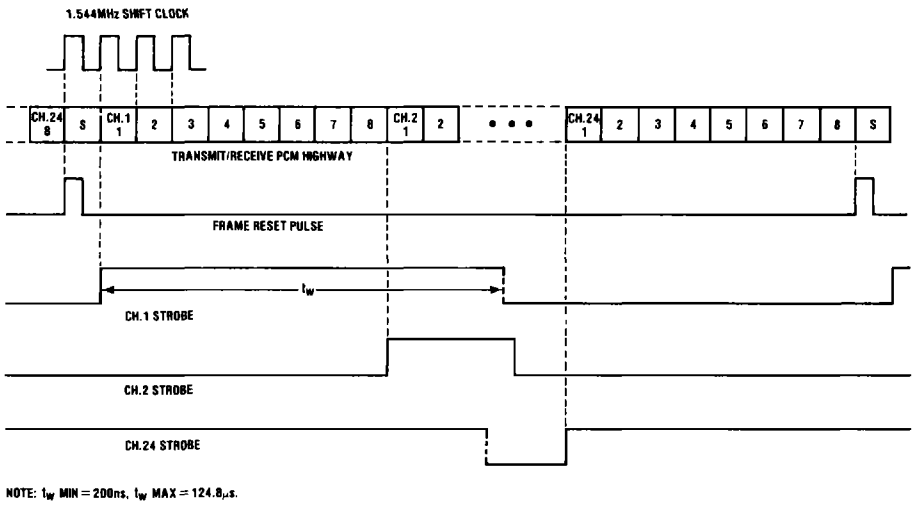
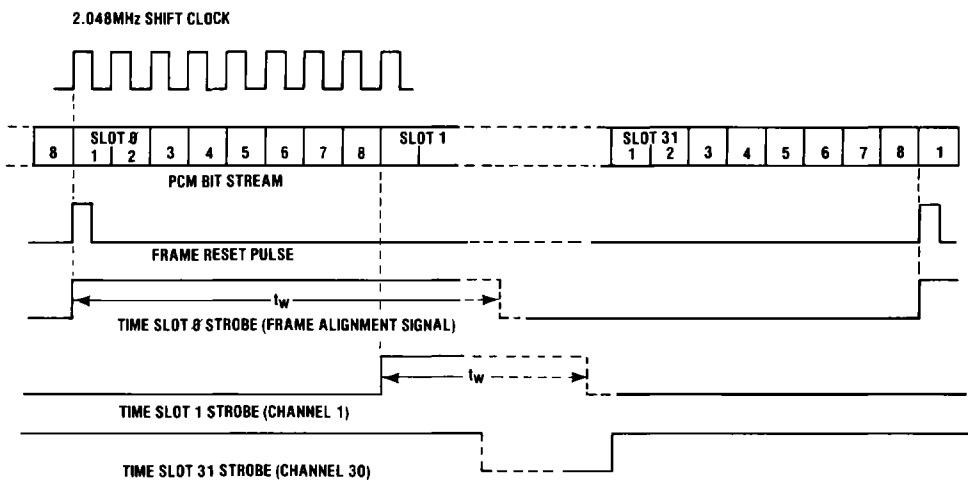


Figure 2A. Waveforms in a 24 Channel PCM System



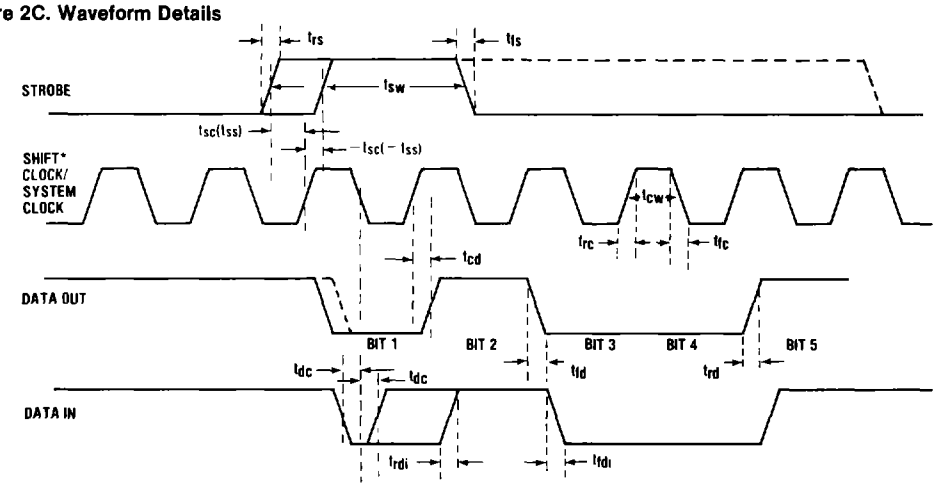
NOTE: t_w MIN = 200ns, t_w MAX = 124.8μs.

Figure 2B. Waveforms in 30 Channel PCM System



NOTE: 200ns $\leq$ Tw $\leq$ 124.8μsec

Figure 2C. Waveform Details



*In this example, the shift clock is the system clock (1.544 or 2.048MHz). In systems where the data shift rate is not the same, the relationship of each to the strobe remains the same. The system clock and shift clock must relate to the strobe within the t_{sc}, t_{ss} timing requirements.

The effect of the strobe occurring after the shift clock is to shorten the first (sign) bit at the data output.

The length of the strobe is not critical. It must be at a logic state longer than one system clock cycle. Therefore, the minimum would be >488ns at 2.048 and the maximum <124.3μsec at 1.544MHz.

	MIN	MAX
t_{cw}	195nsec	9.38μsec.
t_{rs}		100ns
t_{fs}		100ns
$t_{sc}(t_{ss})$	−100nsec.	200ns
t_{rc}		100ns
t_{fc}		100ns
t_{sw}	600ns*	124.3μsec.
t_{cd}	100nsec	150ns
t_{dc}(setup time, hold time)	60nsec.	
t_{rdi}		100ns
t_{fdi}		100ns

‡That is, the strobe can precede the shift clock by 200nsec. or follow it by as much as 100nsec.
*@2.048MHz 700ns @1.544MHz

In the AT&T T1 carrier PCM format an A/B signaling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground, etc., depending on the application. Two signaling conditions (A and B) per channel, giving four possible signaling states per channel are repeated every 12 frames (1.5 milliseconds). The A signaling condition is sent in bit 8 of all 24 channels in frame 6. The B signaling conditions is sent in frame 12. In each frame, bit 193 (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The S3507A in a 28-pin package is designed to simplify the signaling interface. For example, the A/B select input pins are transition sensitive. The transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronizes the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channelbank. The A and B signaling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore, A/B select input must go positive in the beginning of frame 5 and the negative in the beginning of frame 11 (see Figure 3).

Figure 3. Signaling Waveforms in a T1 Carrier System

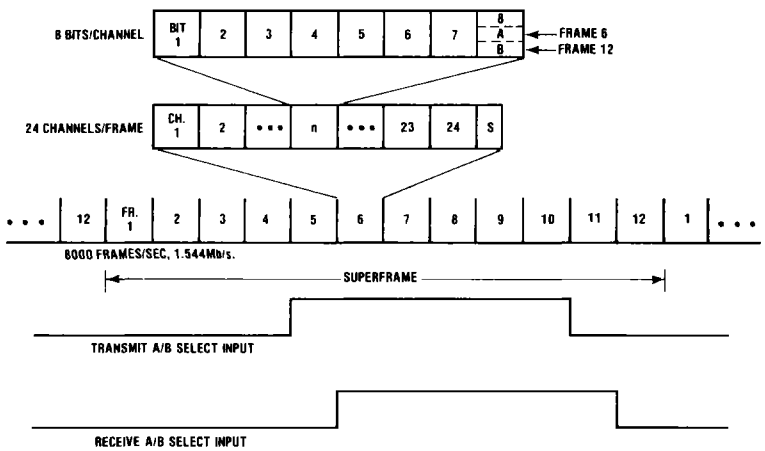
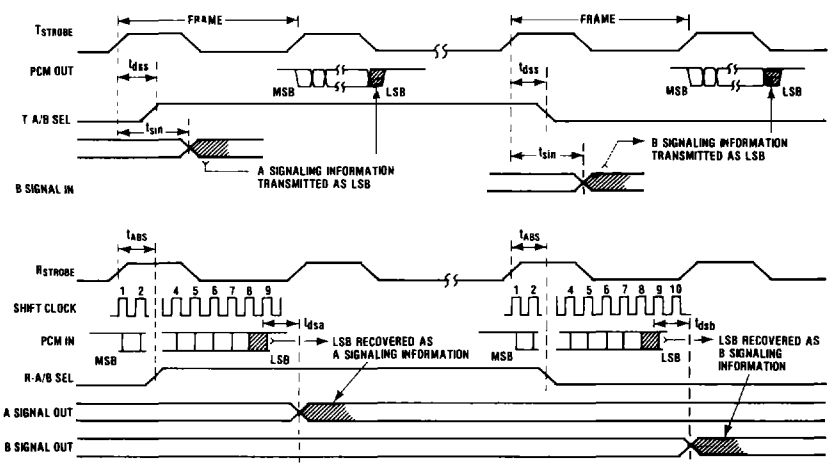
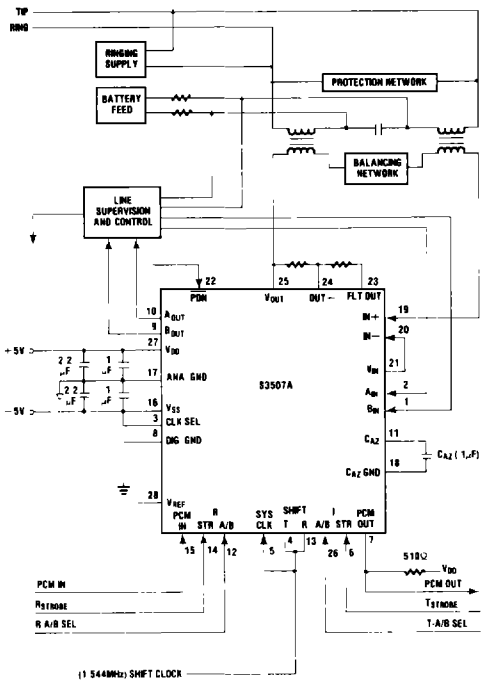


Figure 3A. Signaling Waveform Details



	tdss	tsin	tABS	tdsa	tdsb
max	1.4µs	80µs	3µs	300ns	300ns

Figure 4. A Subscriber Line Interface Circuit



The decoder uses a similar scheme for receiving the A and B signaling bits, with one difference. They are latched to the respective outputs in the same frame in which the A/B select input makes a transition. Therefore, the receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12.

Applications Examples

There are two major categories of Codec applications. Central office, channel bank and PABX applications using a multiplex scheme, and digital telephone type dedicated applications. Minor applications are various A/D or D/A needs where the 8 bit word size is desirable for μP interface and fiber optic multiplex systems where non-standard data rates may be used.

A Subscriber Line Interface Circuit

Figure 4 shows a typical diagram of a subscriber line interface circuit using the S3507A. The major elements of such a circuit used in the central office or PABX are a two-to-four wire converter, PCM Codec with filters (S3507A) and circuitry for line supervision and control. The two-to-four wire converter—generally implemented by a transformer-resistor hybrid—provides the interface between the two-wire analog subscriber loop and the digital signals of the time-division-multiplexed PCM highways. It also supplies battery feed to the subscriber telephone. The line supervision and control circuitry provides off-hook and disconnect supervision, generates ringing and decodes rotary dial pulses. It supplies the A/B signaling bits to the coder for transmission within the PCM voice words. It receives A/B signaling outputs from the decoder and operates the A/B signaling relays.

In the T1 carrier system, 24 voice channels are multiplexed to form the transmit and receive highways, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mb/s.

Within the channelbank the transmit and receive channels of a Codec can occupy the same time slot for a synchronous operation or they can be independent of each other for time slot asynchronous operation. Asynchronous operation helps minimize switching delays through the system. Since the strobe or sync pulse for the coder and decoder sections is independent of each other in the S3507A, it can be operated in either manner.

In the CCITT carrier system, 30 voice channels and 2 framing and signaling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mb/s.

The line supervision and control circuitry within each subscriber line interface can generate all the timing signals for the associated Codec under control of a central processor. Alternatively, a common circuitry within the channelbank can generate the timing signals for all channels. Generation of the timing signals for the S3506 and S3507 is straightforward because of the simplified timing requirements (see Timing Requirements for details). Figures 5 and 5A show design schemes for generating these timing signals in a common circuitry. Note that only three signals: a shift clock, a frame reset pulse (coincident with the S bit) and a superframe reset pulse (coincident with the S bit in Frame 1) are needed. These signals are generated by clock recovery circuitry in the channelbank. Since the Gould Codec does not need channel strobes to be exactly 8-bit periods wide, extra decoding circuitry is not needed.

Figure 5. Generating Timing Signals in a T1 Carrier System

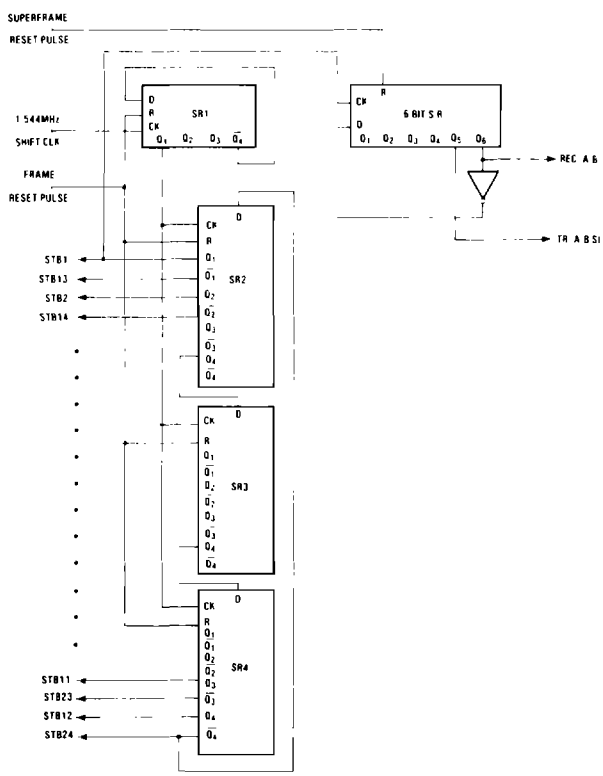
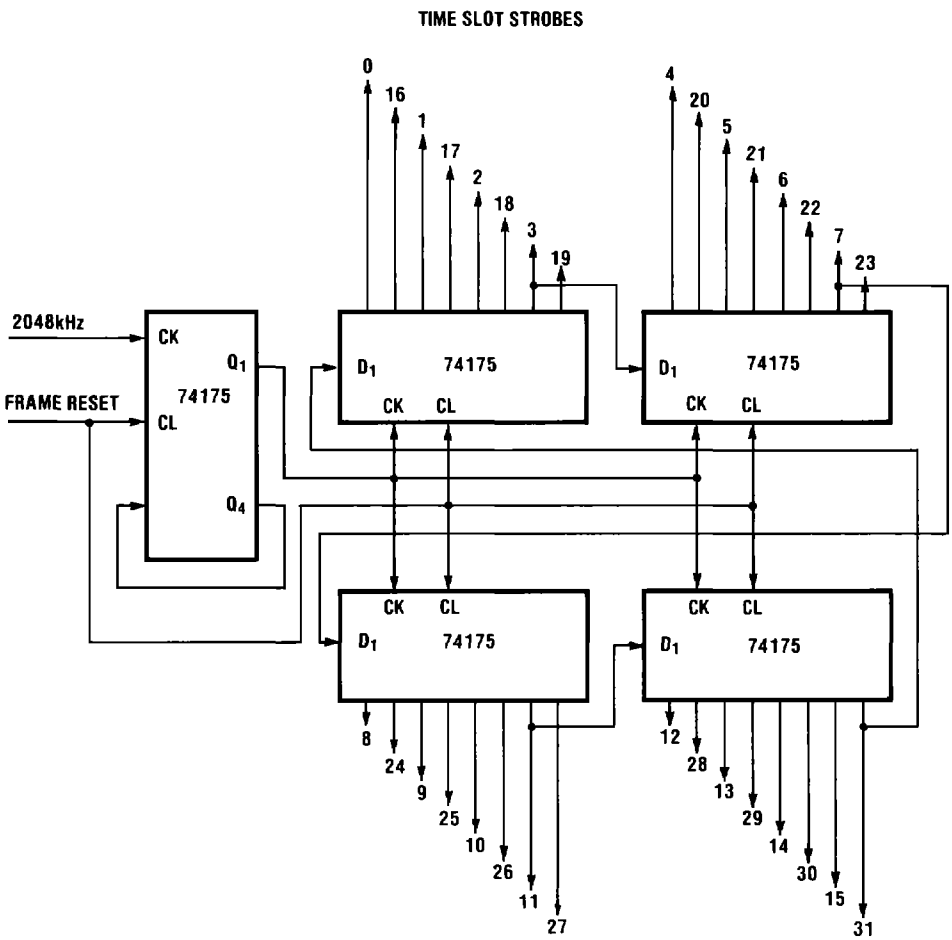


Figure 5A. Generating Timing Signals in a CCITT Carrier System (30 + 2 Channels)



A Digital Telephone Application

Most new PABX designs are using PCM techniques for voice switching with an increasing trend toward applying them at the telephone level. The simplest form of a digital telephone design uses four wire pairs to interface to the switch. Two pairs carry transmit and receive PCM voice data. One pair supplies an 8kHz synchronizing clock signal and the remaining pair supplies power to the telephone. More sophisticated designs reduce costs by time-division-multiplexing and superimposition techniques which minimize the number of wire pairs. The Gould Single-Chip Codec is ideally suited for this application because of the low component count and its simplified timing requirements. Figure 6 shows a schematic for a typical digital telephone design.

Since asynchronous operation is not necessary, transmit and receive timing signals are common. A phase-lock-loop derives the 256kHz system clock and 64kHz shift clock from the 8kHz synchronizing signal received from the switch. The synchronizing signal also serves as the transmit/receive strobe signal since its duty cycle is not important for Codec operation. Microphone output feeds directly into the coder input while the decoder output drives the receiver through an impedance transformer to complete the design.

Figure 6. A Digital Telephone Application