mosaic

Mosaic Semiconductor Inc.

1M x 1 DRAM

MDM11000-80/10/12/15

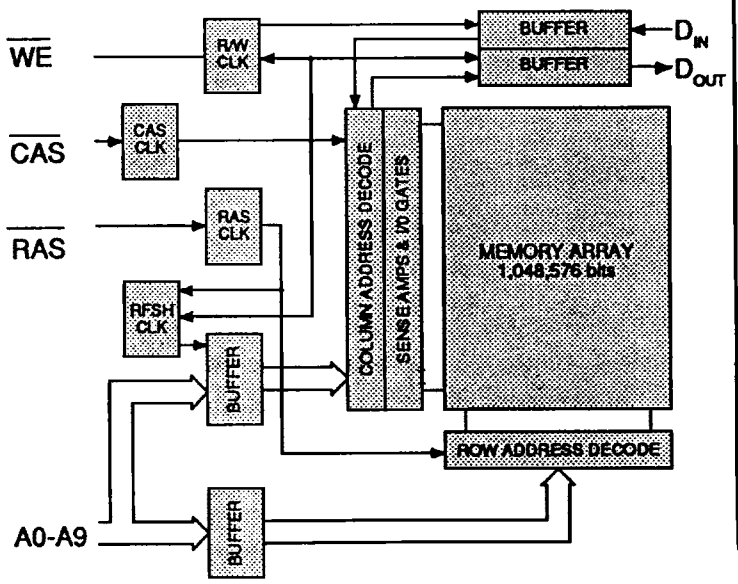
Issue 3.1 : October 1991

1,048,576 x 1 CMOS High Speed Dynamic RAM

Features

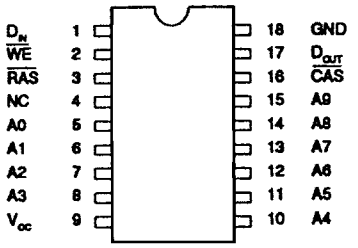
Row Access Times of 80,100/120/150 ns
5 Volt Supply ± 10%
512 Refresh Cycles (8 ms)
$\overline{CAS}$ before $\overline{RAS}$ Refresh
$\overline{RAS}$ only Refresh
Hidden Refresh
Fast Page Mode Capability
May be processed to MIL-STD-883C (suffix MB)

Block Diagram

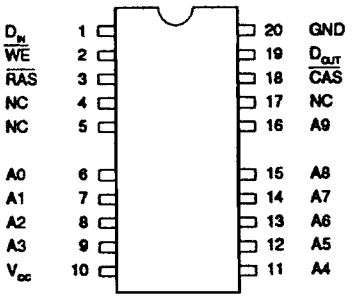


Pin Definitions

Package Type: T,V



Package Type:'G', 'J'



*Package Type 'VX' see page 7

Pin Functions

A0-A9	Address Inputs	$\overline{WE}$	Read/Write Input
D_{IN}	Data Input	D_{OUT}	Data Output
V_{CC}	Power (+5V)	**GND**	Ground
$\overline{RAS}$	Row Address Strobe	**NC**	No Connect
$\overline{CAS}$	Column Address Strobe		

Package Details

Pin Count	Description	Package Type	Material	Pin Out
18	0.3" Dual-in-line (DIP)	T	Ceramic	JEDEC
18	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
24	0.1" Vertical-in-Line (VIL™)	VX	Ceramic	ASIC
20	Bottom Brazed Flat Pack	G	Ceramic	JEDEC
20	Small Outline 'J' lead (SOJ)	J	Ceramic	JEDEC

Package Dimensions and details on pages 7,8 and 9

VIL is a Trademark of Mosaic Semiconductors Inc., US Patent No. D316251.

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-1 V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C
Short circuit output current	I_{OSC}	50	mA

Note : Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I)
	T_{AM}	-55	-	125	°C (M/MB)

Capacitance (V_{CC}=5V±10%,T_A=25°C)

Parameter		*Symbol*	*typ*	*max*	*Unit*	*Notes*
Input Capacitance:	Address,	C_{I1}	-	6	pF	1
	$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$	C_{I2}	-	8	pF	1,2
I/O Capacitance:	Data-in/out	$C_{I/O}$	-	7	pF	1,2

Notes: 1. Capacitance calculated, not measured. 2. $\overline{CAS}$=V_{IH} to disable Dout.

DC Electrical Characteristics T_A=T_{AM}, V_{CC}=V_{CC} ±5%

Parameter	*Symbol*	*Test Condition*	*-80*		*-10*		*-12*		*-15*		*Unit*
			min	*max*	*min*	*max*	*min*	*max*	*min*	*max*	
Operating Current	I_{CC1}	$\overline{RAS}$,$\overline{CAS}$ Cycling: t_{RC}=min.(See Note 1)	-	70	-	60	-	50	-	40	mA
Refresh Current	I_{CC3}	$\overline{RAS}$ only Refresh, t_{RC}=min.	-	70	-	60	-	50	-	40	mA
Refresh Current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min.	-	70	-	60	-	50	-	40	mA
Page Mode Supply Current	I_{CC4}	$\overline{RAS}$=V_{IL},$\overline{CAS}$ Cycling, t_{PC}=min.	-	60	-	50	-	40	-	35	mA
Standby Current	I_{CC2}	$\overline{RAS}$,$\overline{CAS}$=V_{IH},	-	2	-	2	-	2	-	2	mA
	I_{CC5}	$\overline{RAS}$,$\overline{CAS}$ = V_{CC}-0.2V	-	1	-	1	-	1	-	1	mA
Input Leakage	I_{LI}	V_{IN}=0 to +7V	-10	10	-10	10	-10	10	-10	10	µA
Output Leakage	I_{LO}	V_{OUT}=0 to +7V, D_{OUT} is disabled.	-10	10	-10	10	-10	10	-10	10	µA
Output Levels	V_{OH}	I_{OUT}=-5mA	2.4	-	2.4	-	2.4	-	2.4	-	V
	V_{OL}	I_{OUT}=4.2mA	-	0.4	-	0.4	-	0.4	-	0.4	V

Note 1: I_{cc} depends on output loading condition when the device is selected,Icc max. is specified at the output open condition.

AC Test Conditions

* Input pulse levels: 0.6 to 2.4V
* Input rise and fall times: 10nS
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF

Electrical Characteristics & Recommended AC Operating Conditions (1,9)

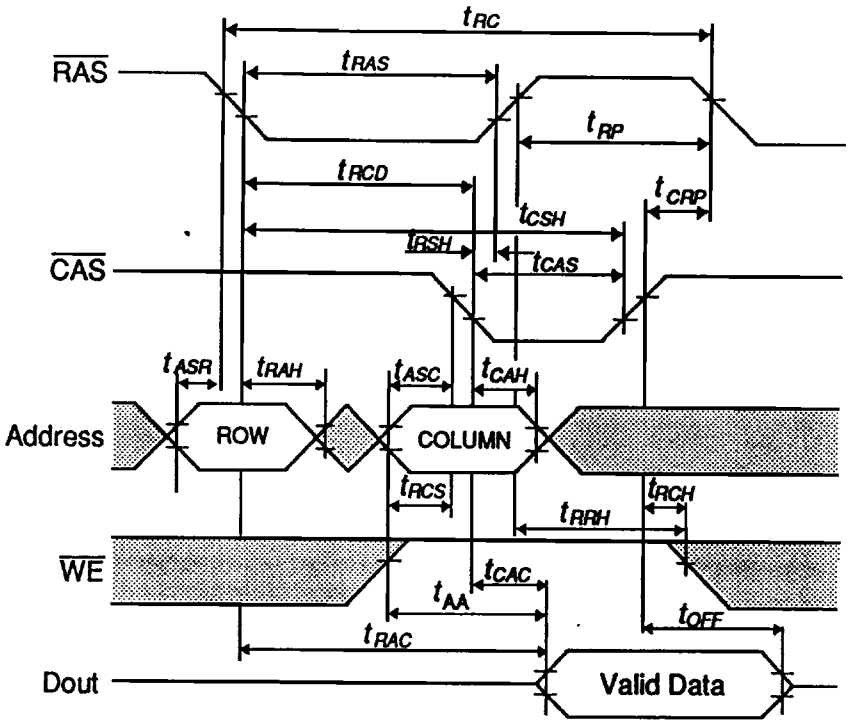
Parameter	Symbol	-80 min	-80 max	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit	Note
Access Time from $\overline{RAS}$	t_{RAC}	-	80	-	100	-	120	-	150	ns	2,3
Access Time from $\overline{CAS}$	t_{CAC}	-	20	-	25	-	30	-	35	ns	2,3
Output Buffer Turn-off Delay	t_{OFF}	0	20	0	25	0	30	0	35	ns	5,11
Transition Time (Rise & Fall)	t_T	3	50	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	160	-	190	-	220	-	250	-	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	-	80	-	90	-	100	-	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	25	10000	30	10000	35	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	25	90	30	105	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	25	-	25	-	30	-	35	-	ns	11
$\overline{CAS}$ Hold Time	t_{CSH}	85	-	100	-	120	-	150	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	-	10	-	10	-	10	-	ns	11
Row Address Setup Time	t_{ASR}	0	-	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	12	-	12	-	15	-	20	-	ns	
Column Address Setup Time	t_{ASC}	0	20	0	20	0	25	0	25	ns	
Column Address Hold Time	t_{CAH}	20	-	20	-	25	-	25	-	ns	
Write Command Setup Time	t_{WCS}	0	-	0	-	0	-	0	-	ns	8
Write Command Hold Time	t_{WCH}	15	-	20	-	25	-	30	-	ns	
Write Command Pulse Width	t_{WP}	20	-	20	-	25	-	25	-	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	-	30	-	35	-	40	-	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	-	20	-	25	-	30	-	ns	
Data in Setup Time	t_{DS}	0	-	0	-	0	-	0	-	ns	
Data in Hold Time	t_{DH}	20	-	20	-	25	-	35	-	ns	
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	0	-	ns	11
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	-	0	-	0	-	0	-	ns	10,11
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	-	10	-	10	-	10	-	ns	10,11
Refresh Period (512 Cycles)	t_{REF}	-	8	-	8	-	8	-	8	ms	
$\overline{CAS}$ Setup Time	t_{CSR}	10	-	10	-	10	-	10	-	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	20	-	20	-	25	-	30	-	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	-	0	-	0	-	0	-	ns	
Page Mode Read or Write Cycle	t_{PC}	50	-	60	-	70	-	80	-	ns	11
$\overline{CAS}$ Precharge Time,Page Cycle	t_{CP}	10	25	10	25	15	30	20	35	ns	11
Access Time from column address	t_{AA}	-	45	-	50	-	60	-	60	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	20	60	ns	

Notes:

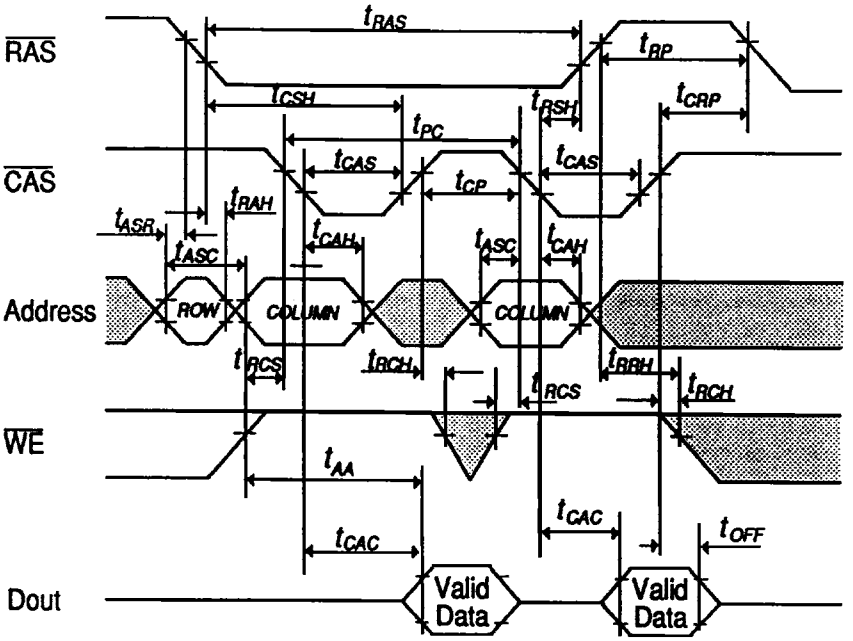
1. AC measurements assume t_T=5ns.
2. Assumes that t_{RCD} is less than or equal to t_{RCD} (max.).If t_{RCD} is greater than the max. recommended value shown in this table,t_{RAC} exceeds the value shown.
3. Measured with a load current equivalent to two TTL loads and 100pF.
4. Assumes that t_{RCD} is greater than or equal to t_{RCD} (max.).
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} is not a restrictive operating parameter. It is included in the Data Sheet as Electrical Characteristics only.
9. An initial pause of 100µs is required after power-up. Then execute at least 8 initialisation ($\overline{RAS}$) cycles.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. This parameter is not tested

Timing Waveforms

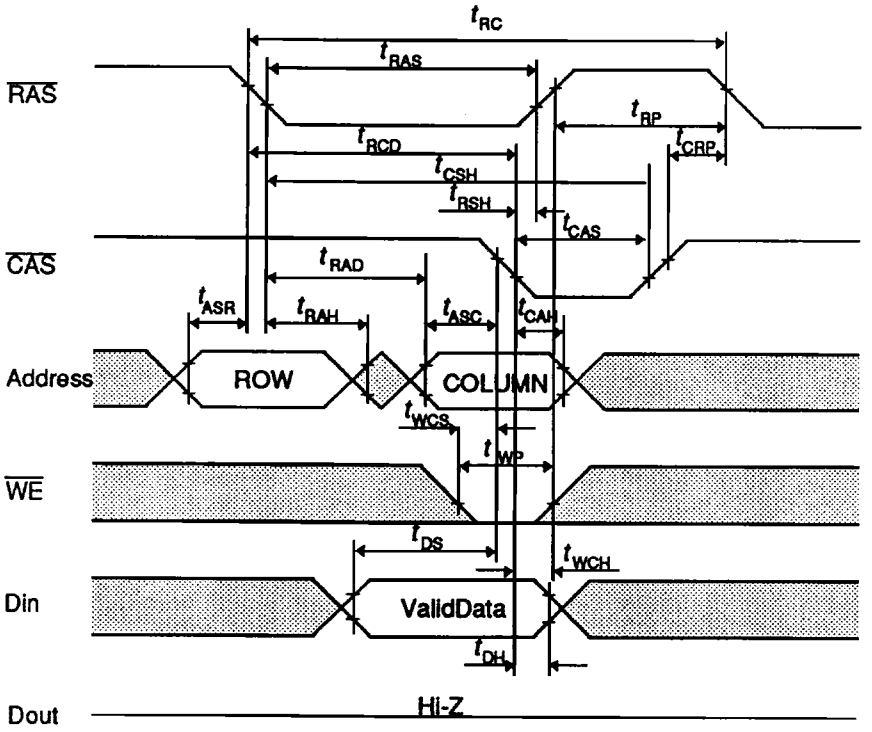
Read Cycle



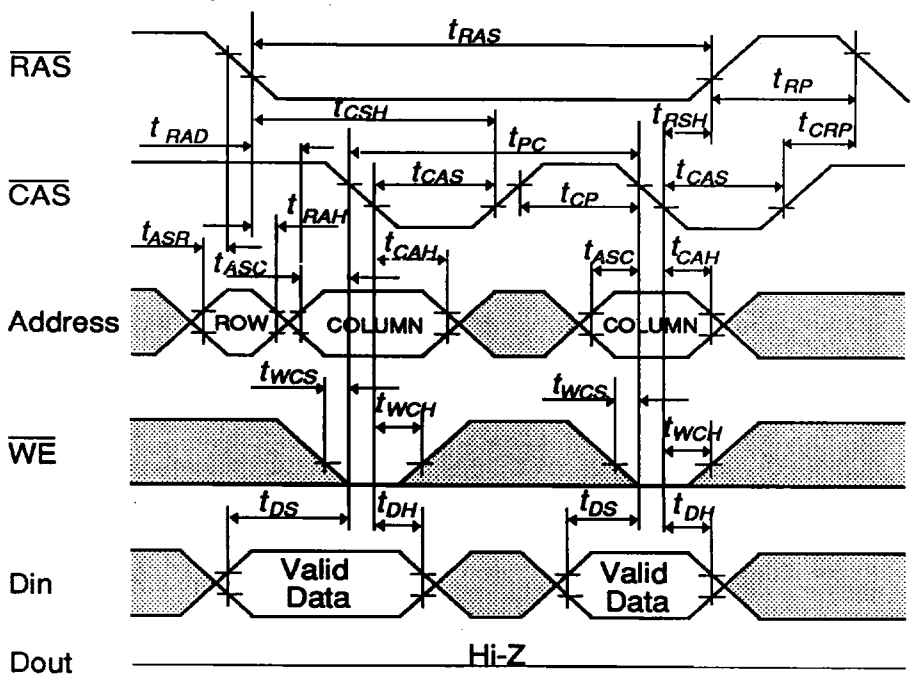
Page Mode Read Cycle



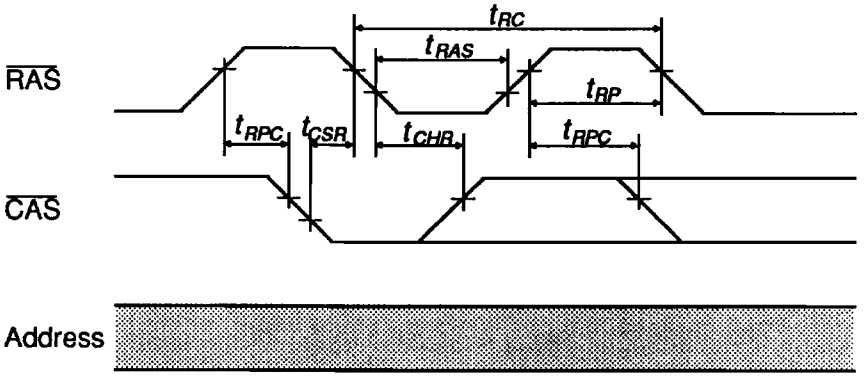
Write Cycle



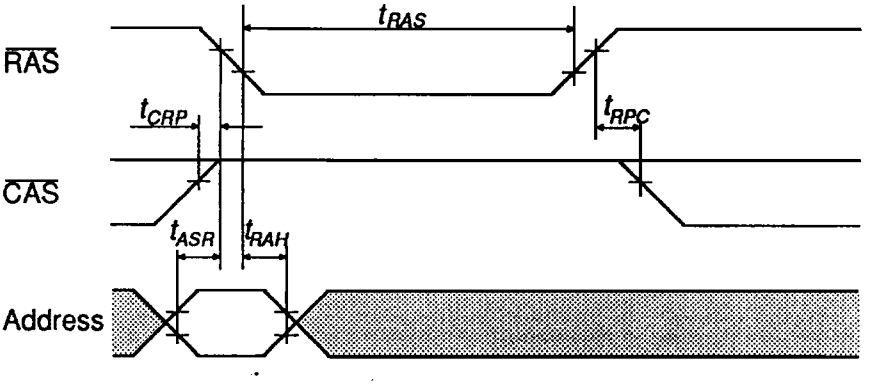
Page Mode Write Cycle



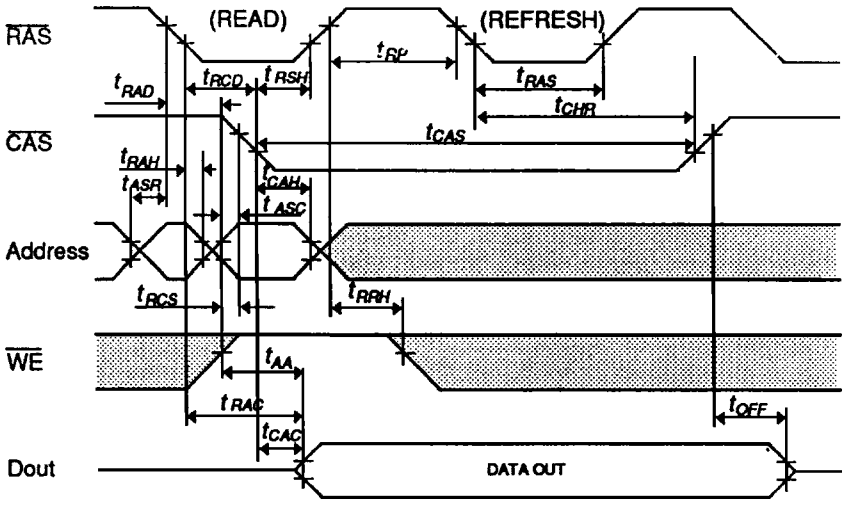
CAS Before RAS Refresh Cycle



RAS Only Refresh Cycle

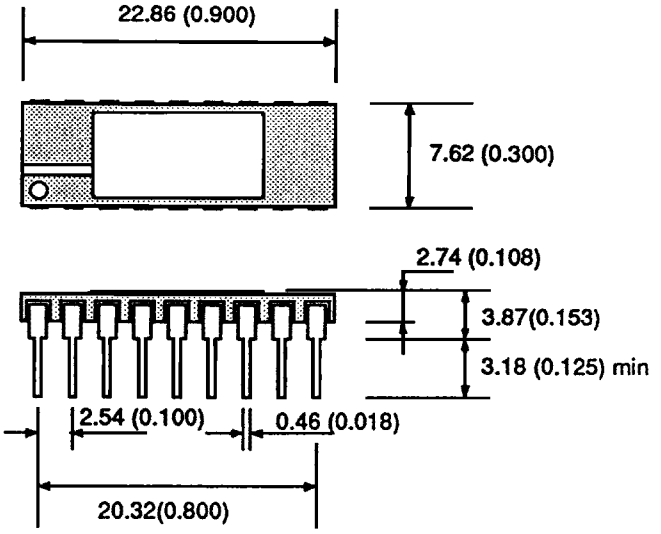


Hidden Refresh Cycle

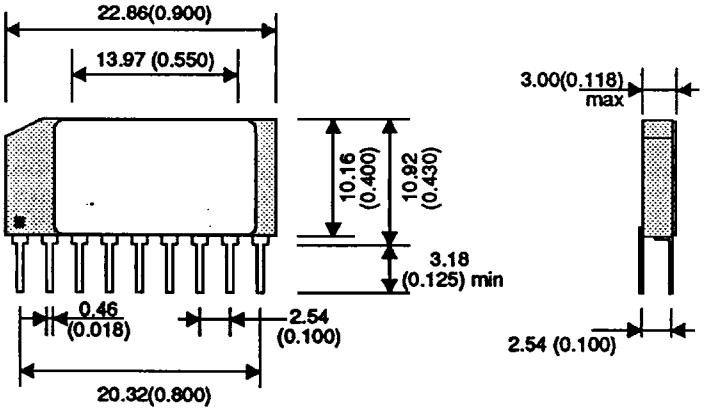


Package Details Dimensions in mm (inches).

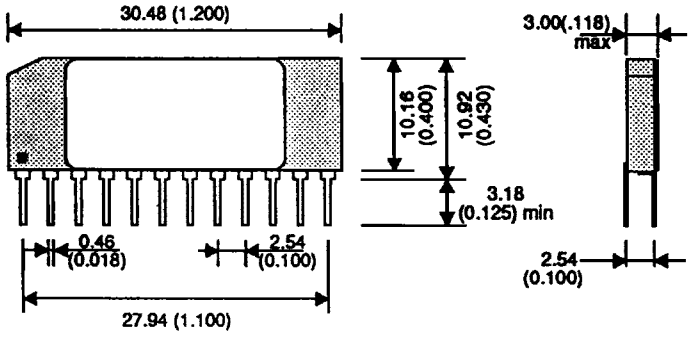
18 Pin DIL ('T' Package)



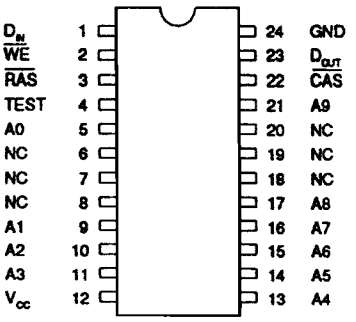
18 Pin VIL ('V' Package)



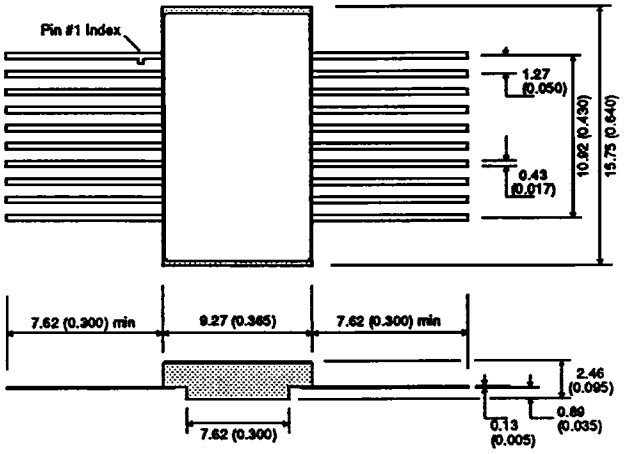
24 Pin Vertical In line ('VX' Package)



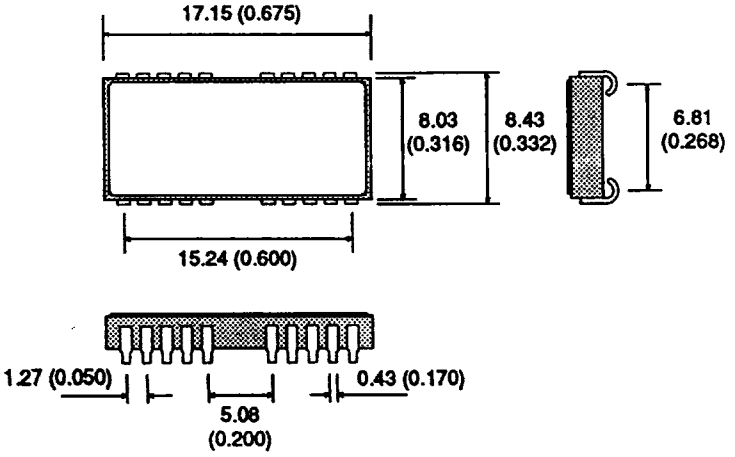
Package Type:'VX'



20 Pin Flat Pack ('G' Package)



20 Pin CSOJ ('J' Package)



Military Screening Procedure

Component Screening Flow for high reliability product is in accordance with Mil-883C method 5004 and is detailed below:

MB COMPONENT SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
High-temperature storage	1008 Condition C (24hrs @ +150°C)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at Ta=+25°C	100%
Burn-in	Method 1015,Condition D,Ta=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at Ta=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MDM11000TI-10

Speed	80	= 80 ns
	10	= 100 ns
	12	= 120 ns
	15	= 150 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed to MIL-883 B, Method 5004
Package	T	= 18 Pin 0.3" DIL
	V	= 18 Pin 0.1" VIL
	VX	= 24 Pin 0.1" VIL
	G	= 20 Pin Ceramic Flat Pack
	J	= Ceramic Small-Outline J-Lead (SOJ)

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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Mosaic
Semiconductor
Inc.

7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
FAX: (619) 271 6058