# DATA SHEET

# Class 1, NP0 50 V feedthrough

## Surface-mount ceramic multilayer capacitors

Product specification
Supersedes data of 25th August 1999

2001 May 30 Rev.3



Phycomp
A FORMER PHILIPS COMPANY

# Surface-mount ceramic multilayer capacitors

# Class 1, NP0 50 V feedthrough

## FEATURES

- High capacitance per unit volume
- Supplied in tape on reel or in bulk
- For high frequency applications
- NiSn terminations.

## APPLICATIONS

- Consumer electronics
- Telecommunications
- Automotive
- Data processing.

## DESCRIPTION

The capacitor consists of a rectangular block of ceramic dielectric in which a number of interleaved precious metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the four terminations, silver dipped with a barrier layer of plated nickel and finally covered with a layer of plated tin (NiSn). A 3D diagram of the structure is shown in Fig.1.

## QUICK REFERENCE DATA

| DESCRIPTION | VALUE |
|---|---|
| Rated voltage $U_R$ (DC) | 50 V (IEC) |
| Capacitance range (E12 series) | 47 pF to 1 nF |
| Tolerance on capacitance | ±10%; ±5% |
| Test voltage (DC) for 1 minute | $2.5 \times U_R$ |
| Sectional specifications | IEC 60384-10, second edition 1989-04; also based on CECC 32 100 |
| Detailed specification | based on CECC 32 101-801 |
| Climatic category (IEC 60068) | 55/125/56 |

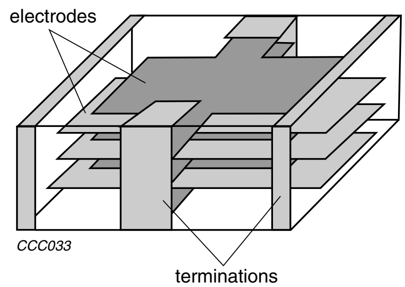
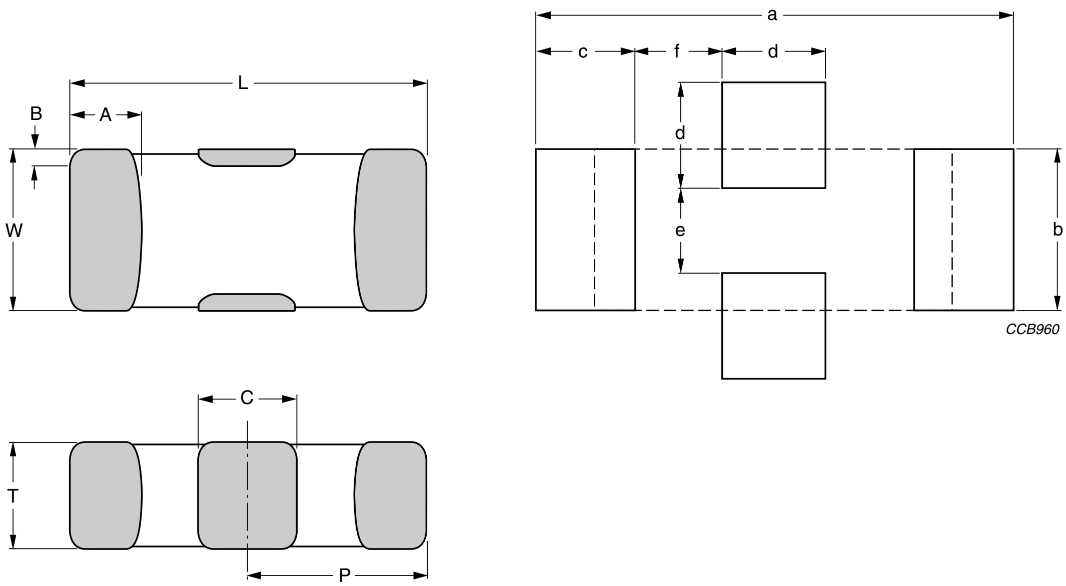



Fig.1 Construction of a Feedthrough capacitor.

## MECHANICAL DATA




a. Outline.

b. Dimensions of solder lands.

For dimensions see Tables 1 and 2.

Fig.2 Physical dimensions.

### Physical dimensions

**Table 1** Capacitor dimensions in millimetres

| CASE SIZE | L | W | T | A | B | C | P |
|---|---|---|---|---|---|---|---|
| 1206 | 3.2 ±0.20 | 1.6 ±0.20 | 0.80 ±0.10 | 0.50 ±0.20 | 0.30 ±0.15 | 0.90 ±0.20 | 1.60 ±0.15 |

**Table 2** Dimensions of solder lands in millimetres

| a | b | c | d | e | f |
|---|---|---|---|---|---|
| 4.45 ±0.20 | 1.65 ±0.20 | 1.00 ±0.15 | 0.90 ±0.20 | 1.00 ±0.15 | 0.70 ±0.10 |

## SELECTION CHART

| C (pF) | LAST TWO DIGITS OF 12NC | 50 V |
|---|---|---|
| | | 1206 |
| 47 | 32 | |
| 100 | 36 | |
| 220 | 41 | 0.8 ±0.1 |
| 330 | 43 | |
| 470 | 45 | |
| 1000 | 49 | |

### Thickness classification and packing quantities

| THICKNESS CLASSIFICATION (mm) | 8 mm TAPE WIDTH QUANTITY PER REEL |
|---|---|
| | ∅180 mm; 7" |
| | PAPER |
| 0.8 ±0.1 | 4000 |

## ORDERING INFORMATION

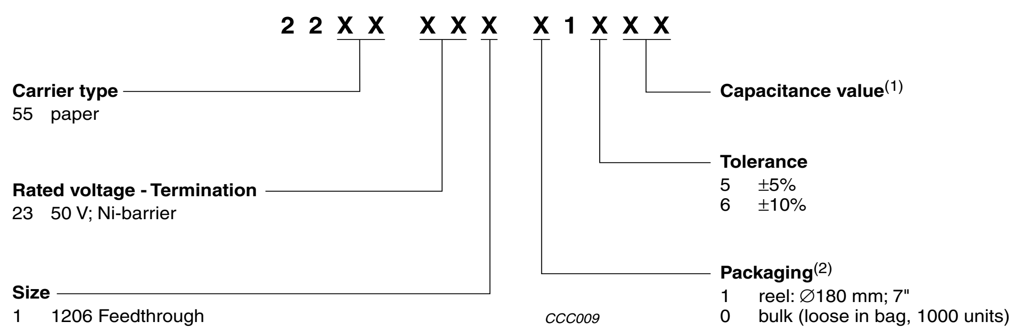
Components may be ordered by using either a simple 15-digit clear text code or Phycomp's unique 12NC.

### Clear text code

EXAMPLE: 1206CG102J9B20F

| SIZE CODE | TEMP. CHAR. | CAPACITANCE | TOL. | VOLTAGE | TERMINATION | PACKING | MARKING | SERIES |
|---|---|---|---|---|---|---|---|---|
| 1206 | CG = NP0 | 102 = 1000 pF; the third digit signifies the multiplying factor:<br>0 = × 1<br>1 = × 10<br>2 = × 100 | J = ±5%<br>K = ±10% | 9 = 50 V | B = NiSn | 2 = 180 mm; 7" paper<br>A = bulk | 0 = no marking | F = feedthrough |

### Ordering code 12NC




(1) Refer to chapter "Selection chart".

(2) Quantity on reel depends on thickness classification, see section "Thickness classification and packing quantities".

## ELECTRICAL CHARACTERISTICS

**Class 1 capacitors; NP0 dielectric; NiSn terminations**

Unless otherwise stated all electrical values apply at an ambient temperature of 23 ±3 °C, an atmospheric pressure of 86 to 106 kPa, and a relative humidity of 63 to 67%.

| DESCRIPTION | VALUE |
|---|---|
| Capacitance range (E12 series) | 47 pF to 1 nF |
| Tolerance on capacitance | ±10%; ±5% |
| Rated voltage $U_R$ (DC) | 50 V |
| Test voltage (DC) for 1 minute | $2.5 \times U_R$ |
| Tan $\delta$; note 1 | $\leq 10 \times 10^{-4}$ |
| Insulation resistance after 1 minute at $U_R$ (DC) | $R_{ins} > 10^5$ MΩ |
| Rated DC resistance | 1 Ω max. |

**Note**

1. Measured at 1 V, 1 MHz for C ≤ 1000 pF and 1 V, 1 kHz for C > 1000 pF, using a four-gauge method.

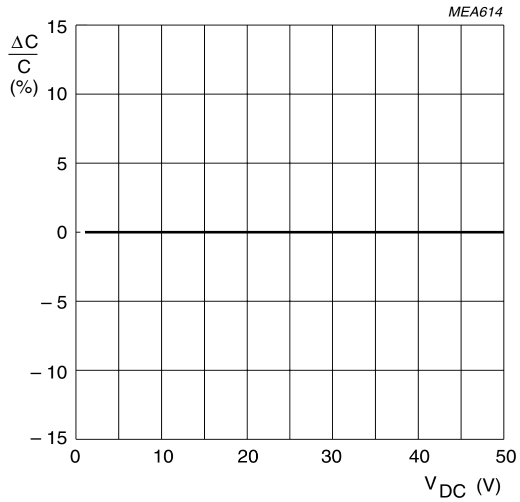



Fig.3 Typical capacitance change with respect to the capacitance at 1 V as a function of DC voltage.

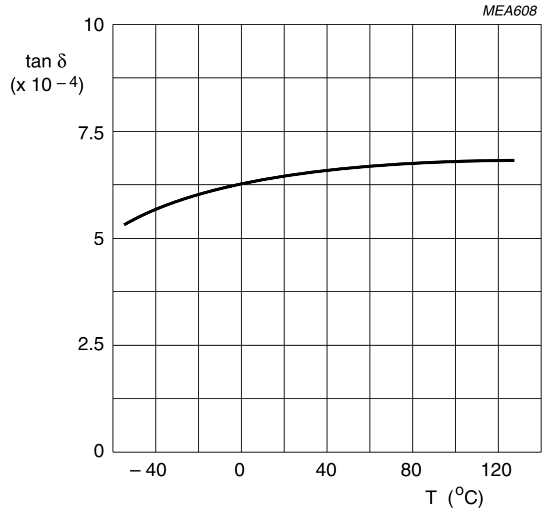



Fig.4 Typical tan δ as a function of temperature.

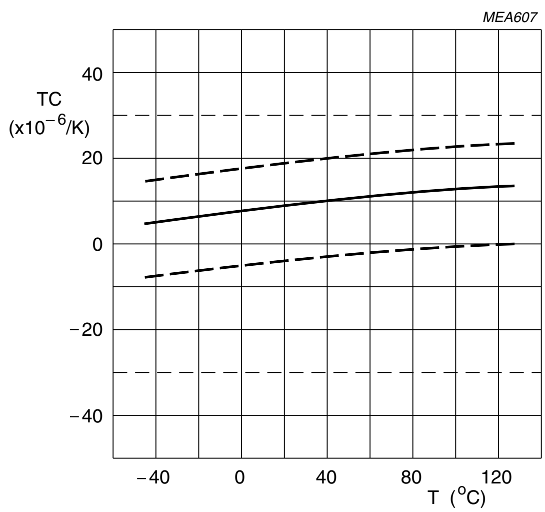



Fig.5 Typical capacitance change as a function of temperature.

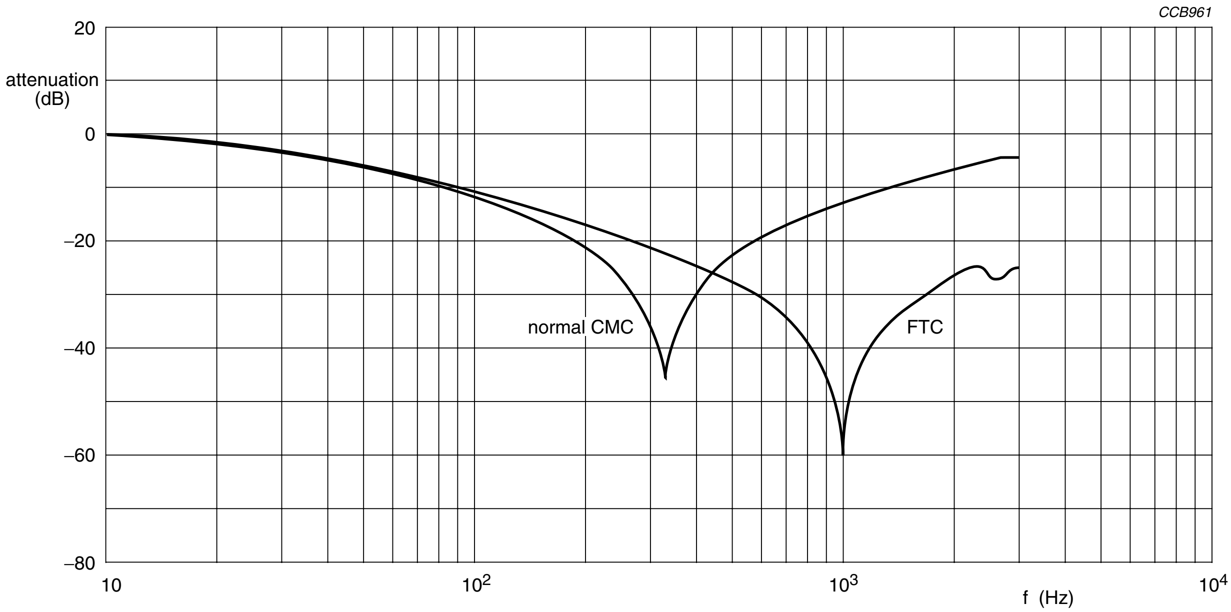



Fig.6 Insertion loss characteristics.

## HIGH FREQUENCY BEHAVIOUR OF MULTILAYER CHIP CAPACITORS

Multilayer chip capacitors (MLCCs) are suitable for use at high frequencies. At frequencies below the series resonance frequency, the MLCC can be represented by an equivalent circuit as shown in Fig.7.

In general, the quantities C, ESR and L are frequency dependent. For most applications, C and L can be regarded as frequency independent below 1 GHz.

The equivalent series self-inductance L is:

- Independent of the dielectric material.
- Dependent on the size of the capacitor, it increases with increasing length and decreases with increasing width or thickness of the product.
- The value of L is approximately:
  - 0.6 nH for case size 0603
  - 1 nH for case sizes 0805, 1206 and 1210
  - 1.5 nH for case sizes 1812 and 2220.

These figures are accurate to within 20%.

Because of the inductance L, associated with the MLCC, there will be a frequency at which the inductive reactance will be equal to the reactance of the capacitor.

This is known as the series resonance frequency (SRF) and is given by:

$$SRF = \frac{1}{2\pi\sqrt{LC}}$$

At the SRF, the MLCC will appear as a small resistor. The transmission loss through the MLCC at this series resonance frequency will be low.

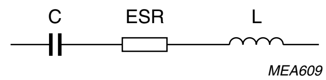
Using the values of C, L = 1 nH and the ESR at a specific frequency (f), two often used quantities can be derived.

The impedance (Z) is given by:

$$Z = \frac{1 - (2\pi f)^2 LC}{2j\pi fC} + ESR$$

The quality factor (Q) is given by:

$$Q = \frac{\left|1 - (2\pi f)^2 LC\right|}{2\pi f ESRC}$$




C = capacitance.

ESR = equivalent series resistance which is determined by the energy dissipation mechanisms (in the dielectric material as well as in the electrodes).

L = equivalent series self-inductance.

Fig.7 Equivalent series representation of a MLCC.

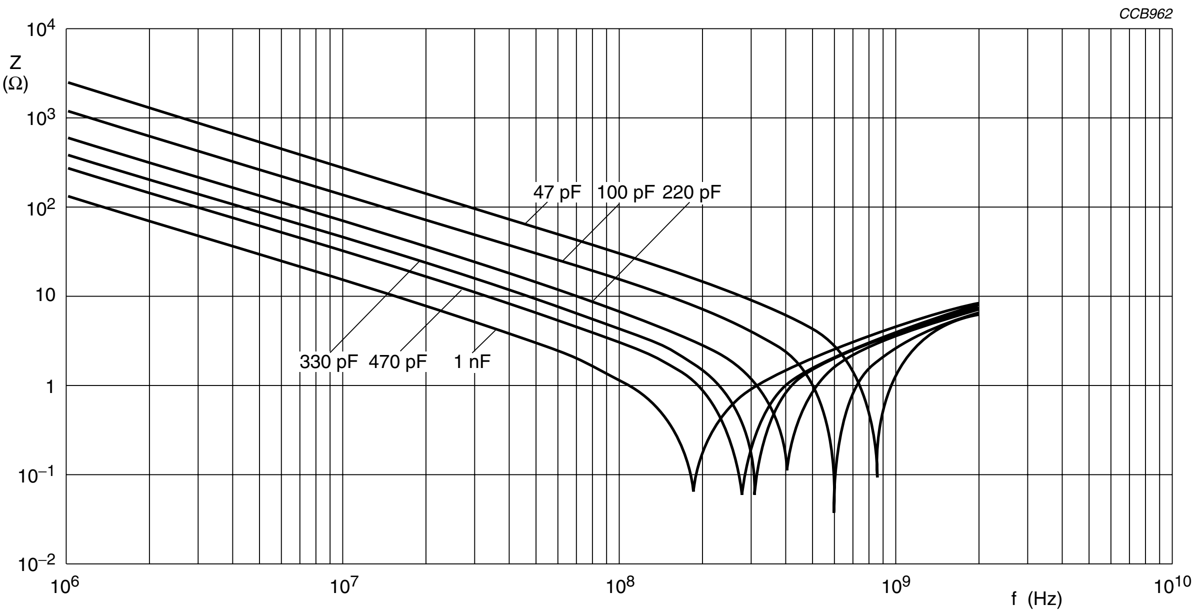



Fig.8 Impedance of FTC as a function of frequency.

Figures 9 and 10 show the comparative inductance of a conventional MLCC and an FTC, when the capacitor is mounted on a substrate. The high frequency capability of the FTC is better than a conventional MLCC due to the inductance of an FTC being less than the MLCC.

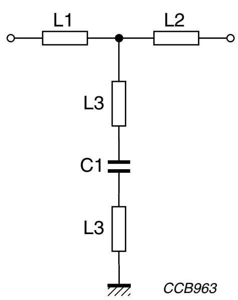



Fig.9 Inductance of LMCC.

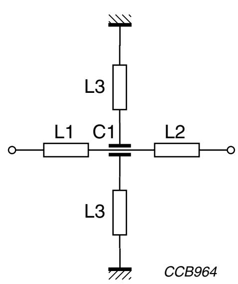



Fig.10 Inductance of FTC.

The equivalent circuits show parasitic inductances L1, L2 and L3. The resonance frequency ($f_r$) can be determined as follows: $f_r = \frac{1}{2\pi\sqrt{L_g \times C1}}$ ($L_g$ = inductance between signal through line and GEN).

The inductance of the FTC ($L_{gFTC} = L3//L3 = \frac{L3}{2}$) is one quarter that of the MLCC ($L_{gCMC} = L3 + L3 = L3 \times 2$).

## TESTS AND REQUIREMENTS

**Table 3** Test procedures and requirements

| IEC 60384-10/ CECC 32 100 CLAUSE | IEC 60068-2 TEST METHOD | TEST | PROCEDURE | REQUIREMENTS |
|---|---|---|---|---|
| 4.4 | | mounting | the capacitors may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering (including vapour phase soldering) or conductive adhesive | no visible damage |
| 4.5 | | visual inspection and dimension check | any applicable method using ×10 magnification | in accordance with specification |
| 4.6.1 | | capacitance | f = 1 MHz; measuring voltage 1 $V_{rms}$ at 20 °C | within specified tolerance measured 1000 hours after date of manufacture |
| 4.6.2 | | tan δ | f = 1 MHz; measuring voltage 1 $V_{rms}$ at 20 °C | in accordance with specification |
| 4.6.3 | | insulation resistance | at $U_R$ (DC) for 1 minute | in accordance with specification |
| 4.6.4 | | voltage proof | 2.5 × $U_R$ for 1 minute | no breakdown or flashover |
| 4.7.1 | | temperature coefficient | between minimum and maximum temperature | in accordance with specification |
| 4.8 | | adhesion | a force of 5 N applied for 10 s to the line joining the terminations and in a plane parallel to the substrate | no visible damage |
| 4.9 | | bond strength of plating on end face | mounted in accordance with CECC 32 100, paragraph 4.4 | no visible damage |
| | | | conditions: bending 1 mm at a rate of 1 mm/s, radius jig 340 mm | ΔC/C: ≤10% |
| 4.10 | Tb | resistance to soldering heat; jig clamps to the second component along the longitudinal line | 260 ±5 °C for 10 ±0.5 s in a static solder bath | the terminations shall be well tinned after recovery<br>ΔC/C: ±0.5% or 0.5 pF whichever is greater |
| | | resistance to leaching; jig clamps to the second component along the longitudinal line | 260 ±5 °C for 30 ±1 s in a static solder bath | using visual enlargement of ×10, dissolution of the terminations shall not exceed 10% |

| IEC 60384-10/ CECC 32 100 CLAUSE | IEC 60068-2 TEST METHOD | TEST | PROCEDURE | REQUIREMENTS |
|---|---|---|---|---|
| 4.11 | Ta | solderability; jig clamps to the second component along the longitudinal line | zero hour test, and test after storage (20 to 24 months) in original packing in normal atmosphere;<br>unmounted chips completely immersed for 2 ±0.5 s in a solder bath at 235 ±5 °C | the terminations shall be well tinned ≥95% |
| 4.12 | Na | rapid change of temperature | preconditioning, class 2 only;<br>5 cycles in the following sequence:<br>30 minutes at –55 °C, change within 30 minutes to +125 °C | no visible damage<br>after 24 hours recovery:<br>ΔC/C: ±1% or ±1 pF |
| 4.14 | Ca | damp heat | preconditioning, class 2 only:<br>56 days at 40 °C;<br>90 to 95% RH; $U_R$ applied;<br>30 minutes at –55 °C, change within 30 minutes to +125 °C | no visual damage<br>after 1 to 2 hours recovery:<br>ΔC/C: ±2% or ±1 pF, whichever is greater<br>tan δ: ≤2 × specified value<br>$R_{ins}$: ≥2500 MΩ or $R_iC_R$ ≥ 25 s, whichever is less |
| 4.15 | | endurance | preconditioning, class 2 only (thermal treatment):<br>1000 hours at 125 °C and 2 × $U_R$ applied | no visual damage<br>after 1 to 2 hours recovery:<br>ΔC/C: ±2% or 1 pF, whichever is greater<br>tan δ: ≤2 × specified value<br>$R_{ins}$: ≥4000 MΩ or $R_iC_R$ ≥ 40 s, whichever is less |