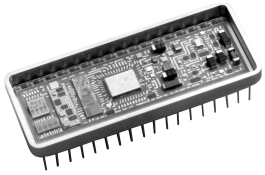


SYNCHRO/RESOLVER-TO-DIGITAL CONVERTERS

DESCRIPTION

The SD-14595 is a low-cost, high reliability, synchro- or resolver-to-digital converter with 14-bit-only, 16-bit-only or pin programmable 14-bit or 16-bit resolution. Packaged in a 36-pin DDIP, the SD-14595/96/97 series feature Built-In-Test (BIT) output.

The SD-14595/96/97 series accepts broadband inputs: 360 to 1 kHz. Other features are solid-state signal and reference isolation and high common mode rejection. In addition, the SD-14596 and SD-14597 are pin-for-pin replacements for the Natel 1044 and 1046, respectively.

The digital angle output from the SD-14595/96/97 is a natural binary code, parallel positive logic and is TTL/CMOS compatible. The SD-14595/96/97 accomplishes synchronization to a computer with the Converter Busy (CB) output and/or the Inhibit (INH) input.

APPLICATIONS

Because of its high reliability, small size, and low power consumption, the SD-14595/96/97 is ideal for military ground or avionics applications. All models are available with MIL-PRF-38534 processing.

Designed with three-state output, the SD-14595/96/97 is especially well-suited for use with computer based systems. Among the many possible applications are radar and navigation systems, fire control systems, flight instrumentation, and flight trainers or simulators.

FEATURES

- ***Single +5 V Power Supply***
- ***Accuracy to 1.3 Arc Minutes***
- ***Pin Programmable 14 Bit/16 Bit, 14 Bit Only or 16 Bit Only***
- ***No 180° False Lock-up***
- ***Internal Synthesized Reference***
- ***Built-In-Test (BIT) Output***
- ***Low Power***
- ***Pin-for-Pin Replacement for Natel's 1044 and 1046***

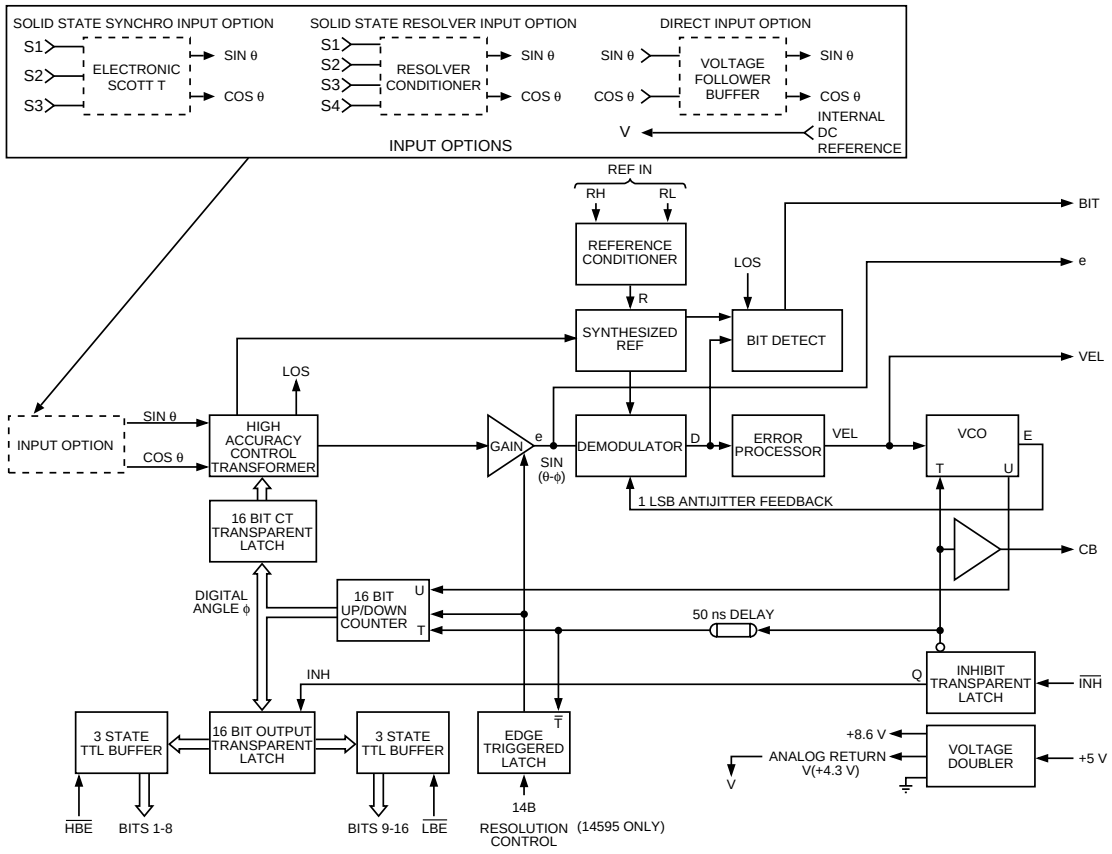


FIGURE 1. SD-14595/96/97 BLOCK DIAGRAM

SD-14595/96/97 SPECIFICATIONS

Specifications apply over temperature range, power supply range, reference frequency, and amplitude range; 15% signal amplitude variation, up to 10% harmonic distortion in the reference, and up to 45° of signal to reference phase shift.

PARAMETER	UNIT	VALUE
RESOLUTION	Bits	14 or 16
ACCURACY	Min	5.2, 2.6, or 1.3
REPEATABILTY	LSB	1 Max
REFERENCE INPUT CHARACTERISTICS		
Carrier Frequency Range	Hz Hz	47-1000 (60 Hz Unit) 360-1000 (400 Hz Unit)
Voltage Range	Vrms	4-130 (for 11.8 V or 90 V signal input) 3-100 (for 1 V direct signal input)
Input Impedance: ■ Single Ended ■ Differential	 Ohm Ohm	250k min 500k min 250 peak max
Common Mode Range	V	
SIGNAL INPUT CHARACTERISTICS (voltage options and minimum input impedance)		
Input Impedance Imbalance	%	0.2 max
■ Synchro	V	11.8 V L-L / 90 V L-L
• Zin Line-to-Line	Ohm	17.5k / 130k
• Zin Each Line-to-Gnd	Ohm	11.5k / 85k
• Common Mode Range	Vpeak	30 / 180
• Maximum Transient Peak Voltage	V	150
■ Resolver	V	11.8 V L-L
• Zin Single Ended	Ohm	23k
• Zin Differential	Ohm	46k
• Zin Each Line-to Gnd	Ohm	23k
• Common Mode Range	V	60 max
• Maximum Transient Peak Voltage	V	150
■ Direct (1.0 V L-L)		
• Input Signal Type		Sin and Cos resolver signals referenced to converter internal DC reference V.
• Sin/Cos Voltage Range	Vrms	1 V nominal, 1.15 V max
• Max Voltage w/o Damage		15 V continuous 100 V Peak Transient
• Input Impedance	Ohm	Zin > 20M // 10 pf voltage follower
REFERENCE SYNTHESIZER		
± Sig/Ref Phase Shift	Deg	60 typ, 45 guaranteed
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs:		Logic 0 = 0.8 V max Logic 1 = 2.0 V min Loading = 30 µA max
Inhibit ($\overline{\text{INH}}$)		Logic 0 inhibits Data stable within 0.5 µs (pull up)

TABLE 1. SD-14595/96/97 SPECIFICATIONS (CONT)

PARAMETER	UNIT	VALUE
DIGITAL INPUT/OUTPUT (cont)		
Resolution Control (14B) (for Programmable Units Only)		Logic 1 for 14 bits Logic 0 for 16 Bits Pull-up current source to +5 V//5 pF max CMOS transient protected
Enable Bits 1 to 8 ($\overline{\text{HBE}}$) Enable Bits 9 to 16 ($\overline{\text{LBE}}$) (9 to 14 for 14-bit mode)		Logic 0 enables Data Valid within 150 ns Logic 1 = High Z Data High Z within 100 ns Pull-down current source to GND//5 pF max CMOS transient protected
Outputs:		
Parallel Data	Bits	14 or 16 parallel lines; natural binary angles, positive logic (see TABLE 3)
Converter Busy (CB)		0.8 to 3.0 µs positive pulse; leading edge initiates counter update.
BIT		Logic 1 for fault conditions.
Drive Capability		50 pF + rated logic drive Logic 0; 1 TTL load, 1.6 mA at 0.4 V max Logic 1; 10 TTL loads, 0.4 mA at 2.8 V min High Z;10 µA//5 pF max Logic 0; 100 mV max driving CMOS Logic 1; +5 V supply minus 100 mV min driving CMOS
ANALOG OUTPUT		
Analog Return (V)		+4.3 V nom
Velocity (VEL) (See note 3.)		See TABLE 4.
AC error (e) ■ 14-Bit Mode ■ 16-Bit Mode	 mV_{rms} mV_{rms}	 3.5 per LSB of error 1.75 per LSB of error
Load	mA	1
DYNAMIC CHARACTERISTICS		See TABLE 6
POWER SUPPLY CHARACTERISTICS		
Nominal Voltage	V	+5
Voltage Tolerance	%	±10
Max Voltage w/o Damage	V	+7
Current	mA	25 max+digital output load
TEMPERATURE RANGES		
Operating (-1XX or -4XX)	°C	-55 to +125
(-3XX or -8XX)	°C	0 to 70
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS	in (mm) oz(g)	.9 x 0.78 x 0.21 (48 x 20 x 5.3) 36-Pin Double Dip 0.7 max (20)

TABLE 1. SD-14595/96/97 SPECIFICATIONS (CONTD)

PARAMETER	VALUE
TRANSFORMER CHARACTERISTICS (See ordering information for list of Transformers. Reference Transformers are Optional for Both Solid-State and Voltage Follower Input Options.)	
400 Hz TRANSFORMERS	
Reference Transformer	
Carrier Frequency Range	360 - 1000 Hz
Voltage Range	18 - 130 V
Input Impedance	40 kΩ min
Breakdown Voltage to GND	1200 V peak
Signal Transformer	
Carrier Frequency Range	360-1000 Hz
Breakdown Voltage to GND	700 V peak

Minimum Input impedances (Balanced)	SynchroZIN(ZSO)	ResolverZIN
90 V L-L	180 Ω	100 kΩ
26 V L-L	-	30 kΩ
11.8 V L-L	20 kΩ	30 kΩ

60 Hz TRANSFORMERS	
Reference Transformer	
Carrier Frequency Range	47 - 440 Hz
Input Voltage Range	80 -138 V rms; 115 V rms nominal resistive
Input Impedance	600 kΩ min, resistive
Input Common Mode Voltage	500 V rms transformer isolated
Output Description	+R (in phase with RH-RL) and -R (in phase with RL- RH) derived from op-amps. Short-Circuit proof.
Output Voltage	3.0 V nominal riding on ground reference V. Output Voltage level tracks input level.
Power Required	4 mA typ, 7 mA max from +15 V supply.
Signal Transformer	
Carrier Frequency Range	47 - 440 Hz
Input Voltage Range	10 -100 V rms L- L; 90 V rms L- L nominal
Input Impedance	148 kΩ min L- L balanced resistive
Input Common Mode Voltage	±500 V rms, transformer isolated
Output Description	Resolver output, - sine (- S) + Cosine (+C) derived from op-amps. Short circuit proof.
Output Voltage	1.0 V rms nominal riding on ground reference V. Output voltage level tracks input level.
Power Required	4 mA typ, 7 mA max from +15 V supply.

Notes:
(1) Pin Programmable.
(2) See TABLE 7.
(3) VEL polarity is negative volltage for positive angular rate

THEORY OF OPERATION

The SD-14595/96/97 series are small, 36-pin DDIP synchro-to-digital hybrid converters. As shown in the block diagram (FIGURE 1), the SD-14595/96/97 can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.

CONVERTER OPERATION

As shown in FIGURE 1, the converter section of the SD-14595/96/97 contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO), up-down counter, and reference conditioner. The converter produces a digital angle which tracks the analog input angle to within the specified accuracy of the converter.The control transformer performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta \cos\phi - \cos\theta \sin\phi$$

Where:

θ is angle theta representing the resolver shaft position.

ϕ is digital angle phi contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) = 0$, so that ϕ will represent the shaft position θ.

The output of the demodulator is an analog dc level proportional to $\sin(\theta - \phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. It's single ended Input Z is 250k ohms/min, 500k ohms differential.

SPECIAL FUNCTIONS

REFERENCE SYNTHESIZER-QUADRATURE VOLTAGES.

The synthesized reference section of the SD-14595 eliminates errors caused by quadrature voltage. Due to the inductive nature of synchros and resolvers, their signals typically lead the reference signal (RH and RL) by about 6°. When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. In a 14-bit converter it is not necessary to compensate for the reference signal's phase shift. A 6° phase shift will, however, cause problems for the one minute accuracy converters. As shown in FIGURE 1, the converter synthesizes its own $\cos(\omega t + \alpha)$ refer-

ence signal from the sinθ - cos(ωt + α), cosθ - cos(ωt + α) signal inputs and from the cosωt reference input. The phase angle of the synthesized reference is determined by the signal input. The reference input is used to choose between the +180° and -180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be eliminated. **The synthesized reference circuit also eliminates the 180° false error null hangup.**

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error=(Quadrature Voltage/Full Scale (FS).signal) • tan(α)
Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full Scale signal is in volts.
α = signal to REF phase shift

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8 mV
Let: FS signal = 11.8 V
Let: α = 6°

Then: Magnitude of Error = 0.35 min ≅ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the synchro or resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage=(rotational speed/carrier frequency) • FS signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotational speed is the rps (rotations per second) of the synchro or resolver.
Carrier frequency is the REF in Hz.

BUILT-IN-TEST (BIT, PIN 15)

The Built-In-Test output (BIT) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 180 LSBs (of the selected resolution) the logic level at BIT will change from a logic 0 to logic 1. This condition will occur during a large step and reset after the converter settles out. BIT will also change to logic 1 for an over-velocity condition, because the converter loop cannot maintain input-output and/or if the converter malfunctions where it cannot maintain the loop at a null. BIT will also be set for a Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR).

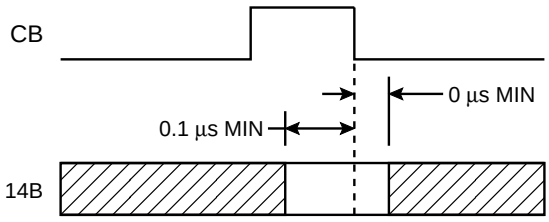


FIGURE 2. RESOLUTION CONTROL TIMING DIAGRAM

PROGRAMMABLE RESOLUTION (14B, PIN 16)

Resolution is controlled by one logic input,14B. The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, input 14B is latched internally on the trailing edge of CB (see FIGURE 2).

Note: The SD-14595 has programmable resolution whereas the SD-14596 and 97 do not.

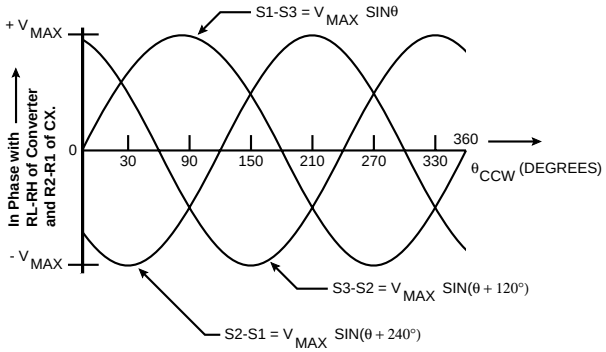
INTERFACING - INPUTS

SIGNAL INPUT OPTIONS

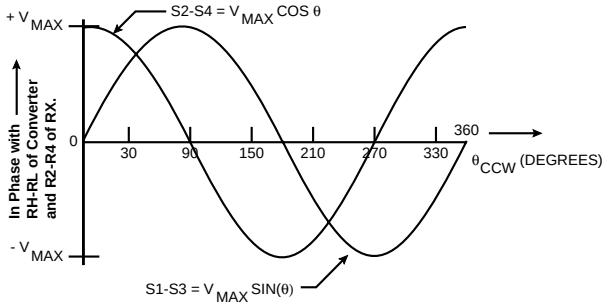
The SD-14595/96/97 series offers direct synchro or resolver inputs. In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form sinθcosωt, sin(θ+120°) cosωt, and sin(θ+240°)cosωt are internally converted to resolver format, sinθcosωt and cosθcosωt.

FIGURE 3 illustrates synchro and resolver signals as a function of the angle θ.

The solid-state signal and reference inputs are true differential inputs with high ac and dc common mode rejection. *Input impedance is maintained with power off.*



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 3. SYNCHRO AND RESOLVER SIGNALS

SOLID-STATE BUFFER INPUT PROTECTION — TRANSIENT VOLTAGE SUPPRESSION

The solid-state signal and reference inputs are true differential inputs with high ac and dc common rejection, so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent ac peak + dc common mode voltage should not exceed the values in TABLE 2.

TABLE 2.

INPUT	COMMON MODE MAXIMUM	MAX TRANSIENT PEAK VOLTAGE
11.8 VL-L 90 VL-L Reference	30 V Peak 180 V Peak 250 V Peak	150 V 150 V 150 V
1 VL-L		100 V

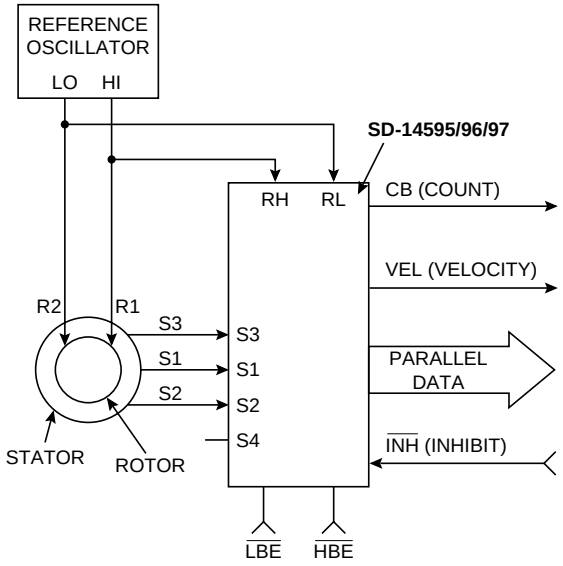


FIGURE 4. SYNCHRO INPUT CONNECTION DIAGRAM

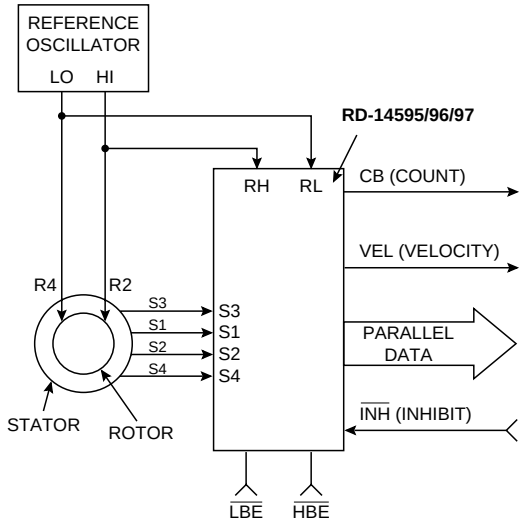


FIGURE 5. RESOLVER INPUT CONNECTION DIAGRAM

90 V line-to-line systems may have voltage transients which exceed the 500 V specification listed. *These transients can destroy the thin-film input resistor network in the hybrid.* Therefore, 90 V L-L solid-state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver are switched on and off. For instance a 1000 V transient can be generated when the primary of a CX or TX driving a synchro or resolver input is opened. See FIGURE 6.

INTERFACING - DIGITAL OUTPUTS AND CONTROLS

DIGITAL INTERFACE

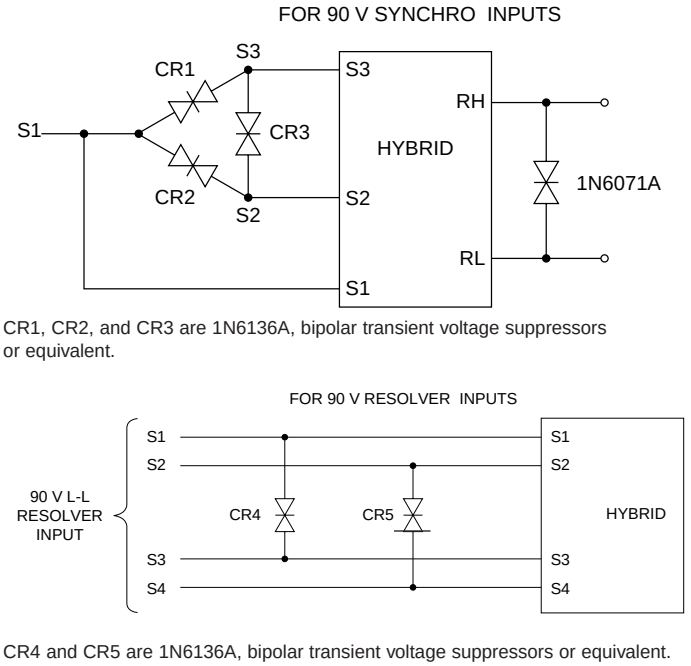
The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the SD-14595/96/97.

2. Furnishes parallel tri-state data formats.

3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the SD-14595/96/97, applying an Inhibit ($\overline{INH}$) command will lock the data in the inhibit transparent latch without interfering with the continuous tracking of the converter's feedback loop. Therefore the digital angle ϕ is always updated and the $\overline{INH}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50 ns delay are part of the inhibit circuitry. For further information see the INHIBIT ($\overline{INH}$, PIN 13) paragraph.



CR1, CR2, and CR3 are 1N6136A, bipolar transient voltage suppressors or equivalent.

CR4 and CR5 are 1N6136A, bipolar transient voltage suppressors or equivalent.

FIGURE 6. CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

DIGITAL ANGLE OUTPUTS (LOGIC INPUT/OUTPUT)

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{HBE}$ (pin 35) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{LBE}$ (pin 17) to a logic 0.

The second byte will contain either bits 9-14 (14-bit resolution) or bits 9-16 (16-bit resolution). All unused LSBs will be at logic 0. TABLE 3 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{HBE}$ or $\overline{LBE}$ are activated with a logic 0 and are high impedance within 100 ns max after $\overline{HBE}$ and $\overline{LBE}$ are set to logic 1 (see FIGURE 7). Both enables are internally pulled down.

TABLE 2. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1(MSB)	180	10800
2	90	5400
3	45	2700
4	22.5	1350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14(LSB 14 BIT MODE)	0.0220	1.32
15	0.0110	0.66
16(LSB 16 BIT MODE)	0.0055	0.33

Note: $\overline{HBE}$ enables the 8 MSBs and $\overline{LBE}$ enables the LSBs.

DIGITAL ANGLE OUTPUT TIMING

The digital angle output is 14 or 16 parallel data bits and CONVERTER BUSY (CB). All logic outputs are short-circuit proof to ground and +5 V. The CB output is a positive, 0.8 to 3.0 µs pulse.

The digital output data changes approximately 50 ns after the leading edge of the CB pulse because of an internal delay. Data is valid 0.2 µs after the leading edge of CB (see FIGURE 8). The angle is determined by the sum of the bits at logic 1. The digital outputs are valid 150 ns max after $\overline{HBE}$ or $\overline{LBE}$ go low and are high impedance within 100 ns max of $\overline{HBE}$ or $\overline{LBE}$ going high.

INHIBIT ($\overline{INH}$, PIN 13)

When an Inhibit ($\overline{INH}$) input is applied to the SD-14595/96/97, the Output Transparent Latch is locked causing the output data bits to remain stable while data is being transferred (see FIGURE 9). The output data bits are stable 0.5 µs after $\overline{INH}$ goes to logic 0.

A logic 0 at the input of the Inhibit Transparent Latch latches the data, and a logic 1 applied, allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic 0 and the $\overline{INH}$ latch is transparent; when CB goes to logic 1, the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is: (1) Apply $\overline{INH}$; (2) Wait 0.5 µs min; (3) Transfer the data; (4) Release $\overline{INH}$ (see FIGURE 9).

A logic 1 for the $\overline{INH}$ enables the output data to be updated. The time it takes for $\overline{INH}$ to go to a logic 1 should be 100 ns minimum before valid data is transferred. To allow the update of the output data with valid information the $\overline{INH}$ must remain at a logic 1 for 1 µs minimum (see FIGURE 10 below).

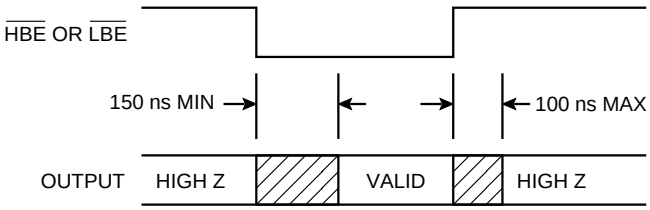


FIGURE 7. TRI-STATE OUTPUT TIMING

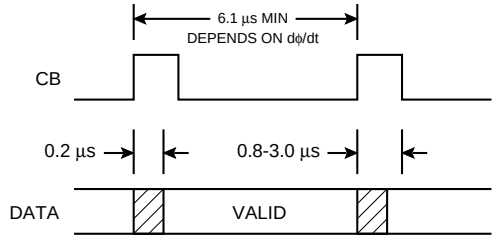


FIGURE 8. CONVERTER BUSY TIMING DIAGRAM

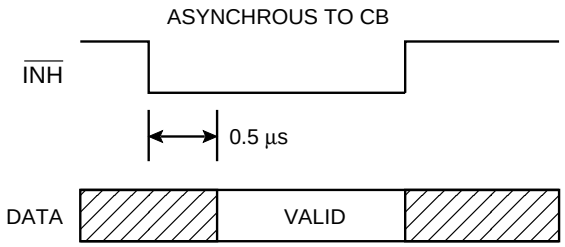


FIGURE 9. INHIBIT TIMING DIAGRAM

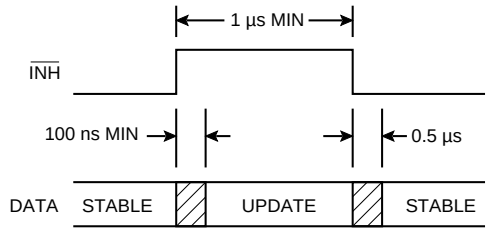


FIGURE 10. OUTPUT DATA UPDATE TIMING

INTERFACING - DIGITAL OUTPUTS AND CONTROLS (CONTD)

DATA TRANSFERS

Digital output data from the SD-14595/96/97 can be transferred to 8-bit and 16-bit bus systems. For 8-bit systems, the MSB and LSB bytes are transferred sequentially. For 16-bit systems all bits are transferred at the same time

DATA TRANSFER TO 8-BIT BUS

FIGURES 11 and 12 show the connections and timing for transferring data from the SD-14595/96/97 to an 8-bit bus.

As can be seen by the timing diagram, the following occurs:

1. The converter $\overline{INH}$ control is applied and must remain low for a minimum of 500 ns before valid data is transferred.

2. $\overline{HBE}$ is set to a low state (logic 0) 350 ns MIN after $\overline{INH}$ goes low and must remain low for a minimum of 150 ns before the MSB data (1-8) is valid and transferred.

3. As $\overline{HBE}$ is set to a high state (logic 1), $\overline{LBE}$ is brought low for a 150 ns MIN before the LSB data is valid and transferred.

4. $\overline{LBE}$ should go high (to logic 1) at least 100 ns MAX before another device uses the bus.

5.Setting $\overline{INH}$ high when data transfer is done, the data refresh cycle can begin. Note the time it takes for $\overline{INH}$ to go to a logic 1 should be 100 ns minimum before valid data is transferred.

Note: For further understanding, refer to the beginning of this section (Digital Interface, Digital Angle Outputs, Digital Angle Output Timing, and Inhibit).

16-BIT DATA TRANSFER

Data transfer to the 16-bit bus is much simpler than the 8-bit bus. FIGURES 13 and 14 (page 8) show the connections and timing for transferring data from the SD-14595/96/97 to a 16-bit bus.

As can be seen by the timing diagram the following occurs:

1. The converter $\overline{INH}$ control is applied and must remain low for a minimum of 500 ns before valid data is transferred.

2. $\overline{HBE}$ and $\overline{LBE}$ are set to a low state (logic 0) 350 ns MIN after INH goes low and must remain low for a minimum of 150 ns before the data (1-16) is valid and transferred.

3. $\overline{HBE}$ and $\overline{LBE}$ should go high (to logic 1) at least 100 ns MAX before another device uses the bus.

4. $\overline{INH}$ goes high and data transfer is done and the data refresh cycle can begin. Note the time it takes for $\overline{INH}$ to go to a logic 1 should be 100 ns minimum before valid data is transferred.

Note: For further understanding, refer to the beginning of this section (Digital Interface, Digital Angle Outputs, Digital Angle Output Timing, and Inhibit).

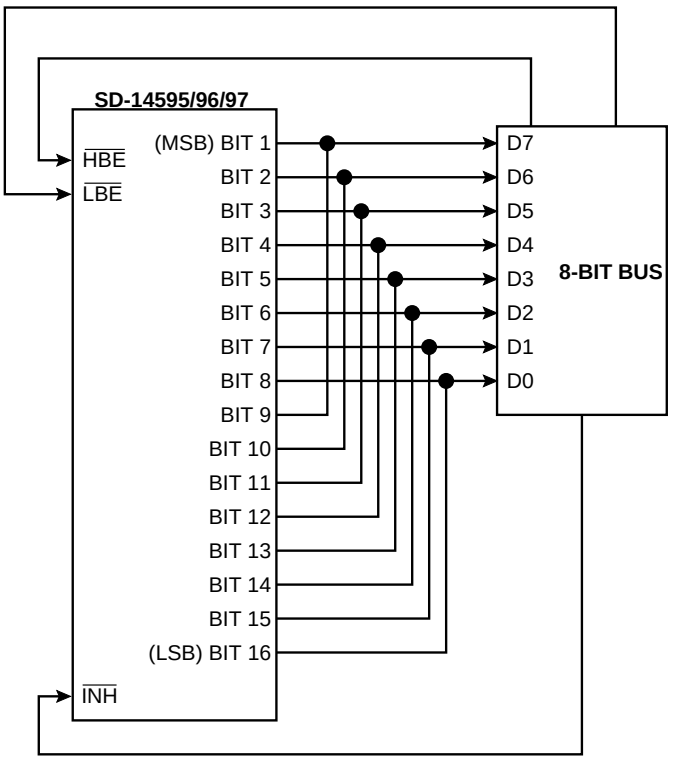


FIGURE 11. DATA TRANSFER TO 8-BIT BUS

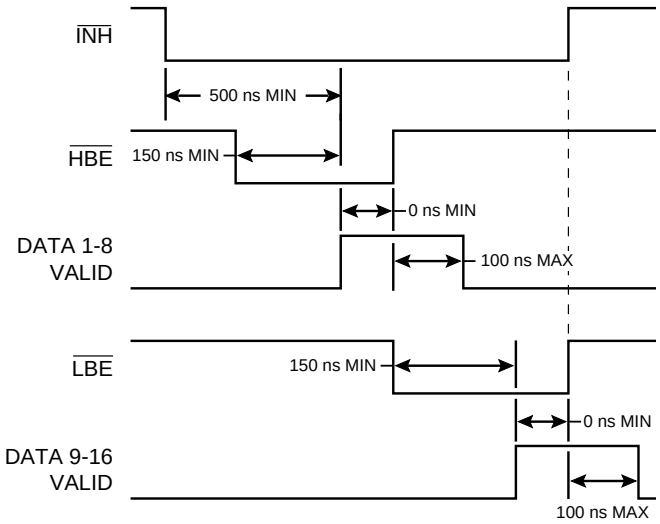


FIGURE 12. DATA TRANSFER TO 8-BIT BUS TIMING

INTERFACING - ANALOG OUTPUTS

The analog outputs are ac error (e), Analog Return (V), and Velocity (VEL).

AC ERROR (e, PIN 12)

The ac error is proportional to the difference between the input angle θ and the digital input angle ϕ, (θ-ϕ), with a scaling of:

3.5 mV rms/LSB (14-bit mode)
1.75 mV rms/LSB (16-bit mode)

The e output can swing ±3 V min with respect to Analog Return (V).

ANALOG RETURN (V, PIN 11)

This internal voltage is not required externally for normal operation of the converter. It is used as the internal dc reference and the return for the VEL and e outputs. It is nominally +4.3 V and is proportional to the +5 V DC supply.

VELOCITY (VEL, PIN 10)

The velocity output (VEL, pin 10) is a dc voltage proportional to angular velocity dθ/dt. The velocity is the input to the voltage controlled oscillator (VCO), as shown in FIGURE 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO.

The VEL output can swing ±1.10 V with respect to Analog Return (V). The analog output VEL characteristics are listed in TABLES 4 and 5.

The VEL output has dc tachometer quality specs such that it can be used as the velocity feedback in servo applications.

TABLE 4. VELOCITY CHARACTERISTICS

PARAMETER	UNITS	TYP		MAX	
Polarity	VEL is negative for positive angular rate.				
Device Type		60 Hz	400 Hz	60 Hz	400 Hz
Output Voltage (see note)	V	1.1	1.1	1.1	1.1
Voltage Scaling	rps/1.1 V	See Vel. Voltage Scaling TABLE 5.			
Scale Factor Error	%	10	10	15	15
Reversal Error	%	1	1	2	2
Linearity Error	% output	0.5	0.5	1	1
Zero Offset	mV	5	5	20	20
Load	mA	0.5	0.5	0.5	0.5
Note: With respect to Analog Return (V)					

TABLE 5. VELOCITY VOLTAGE SCALING (Values in V/rps)

DEVICE TYPE	14 BIT	16 BIT
60 Hz	0.56	2.23
400 Hz	0.11	0.44

Note: If the resolution is changed while the input is changing, then the velocity output voltage and the digital output will have a transient until it settles to the new velocity scaling at a speed determined by the bandwidth.

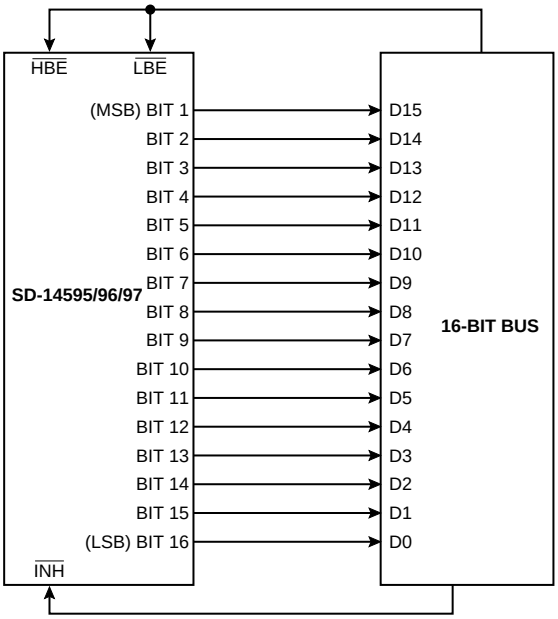


FIGURE 13. 16-BIT DATA TRANSFER

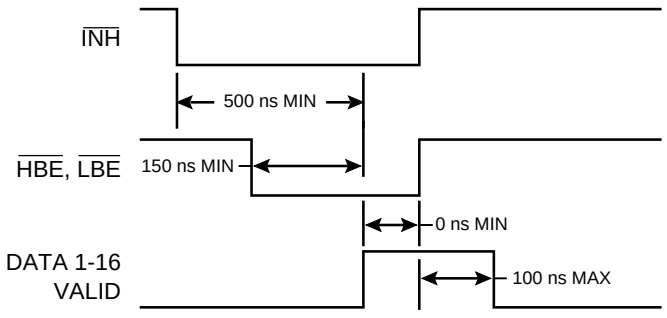


FIGURE 14. 16-BIT DATA TRANSFER TIMING

INTERFACING - DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the SD-14595/96/97 superior dynamic performance. If the power supply voltage is not the +5 V DC nominal value, the specified input rates will increase or decrease in proportion to the fractional change in voltage.

TRANSFER FUNCTIONS

The dynamic performance of the converter can be determined from its transfer function block diagram (FIGURE 15) and open and closed loop Bode plots (FIGURES 16 and 17). Values for the transfer function block can be obtained from TABLE 6.

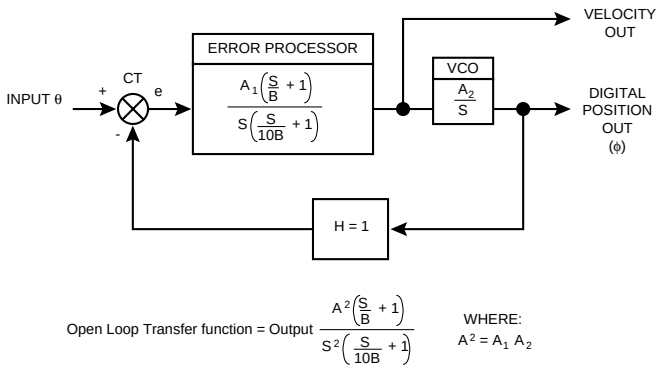


FIGURE 15. TRANSFER FUNCTION BLOCK DIAGRAM

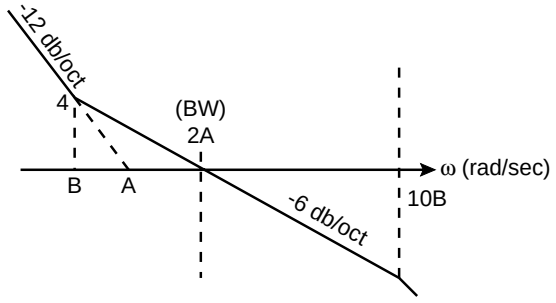


FIGURE 16. OPEN LOOP BODE PLOT

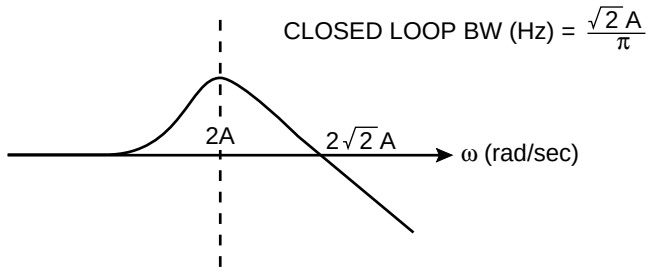


FIGURE 17. CLOSED LOOP BODE PLOT

TABLE 6. DYNAMIC CHARACTERISTICS

PARAMETER	UNIT	60 Hz UNIT		400 Hz UNIT	
		14-BIT	16-BIT	14-BIT	16-BIT
Input Freq.	Hertz	47-1k	47-1k	360-1k	360-1k
Tracking Rate	rps	1.5	0.5	10	2.5
Bandwidth, cl	Hertz	40	20	320	110
Ka	1/sec	7,680	1920	192,000	48,000
A1	1/sec	0.1	0.045	1.2	0.3
A2	1/sec	40k	40k	160,000	160,00
A	1/sec	88	44	440	0
B	1/sec	14.2	14.2	100	220
acc-1 LSB lag	/sec	169	11	4220	100
Settling Time					264
180° degree Step	ms	450	2000	100	
1.4° degree Step	ms	100	250	10	400
					30

RESPONSE PARAMETERS

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. FIGURE 18 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

FASTER SETTLING TIME USING "BIT" TO REDUCE RESOLUTION

Since the SD-14595 has higher precision in the 16-bit mode and faster settling in the 14-bit mode, the BIT output can be used to program the SD-14595 for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit.

CONNECTING THE SD-14595/96/97 TO A P.C. BOARD

The SD-14595/96/97 can be attached to a printed circuit board using hand solder or wave soldering techniques. Limit exposure to 300°C (572°F) max, for 10 seconds maximum.

Since the SD-14595/96/97 converters contain a CMOS device, standard CMOS handling procedures should be followed.

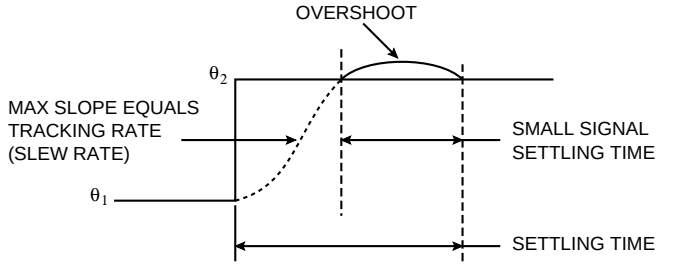
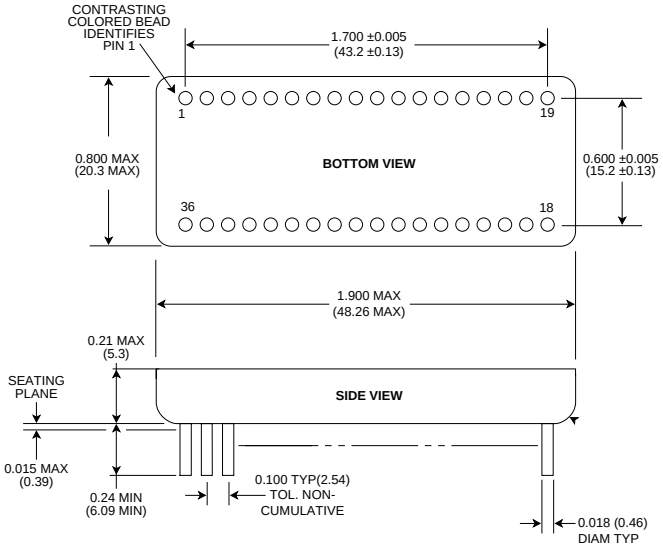


FIGURE 18. RESPONSE TO STEP INPUT

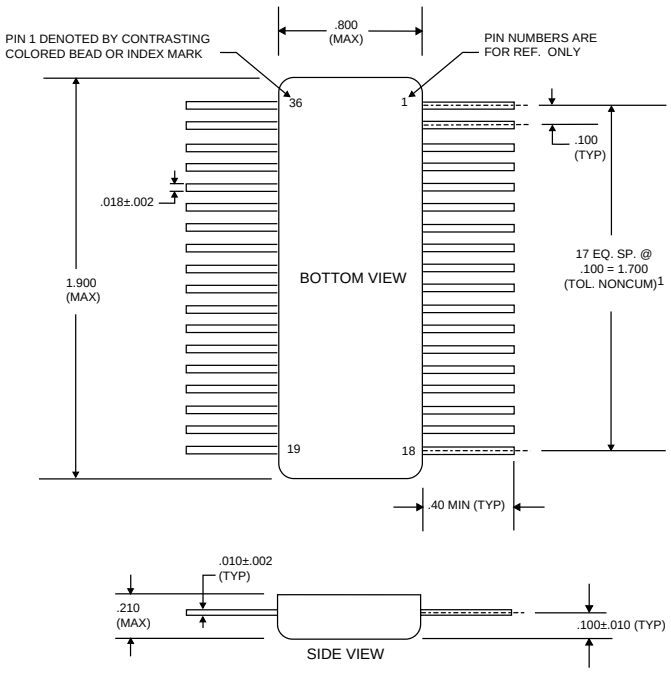
TABLE 7. SD-14595/96/97 PINOUTS			
PIN	**FUNCTION**	**PIN**	**FUNCTION**
1	S1(Res) S1(Syn) -------	36	+5 V
2	S2(Res) S2(Syn) Cos(x)	35	$\overline{\text{HBE}}$
3	S3(Res) S3(Syn) Sin(x)	34	B1 (MSB)
4	S4(Res) ---------- -------	33	B2
5	N/C	32	B3
6	N/C	31	B4
7	N/C	30	B5
8	RL	29	B6
9	RH	28	B7
10	VEL	27	B8
11	Analog Return (V)	26	B9
12	$\overline{\text{e}}$	25	B10
13	$\overline{\text{INH}}$	24	B11
14	CB	23	B12
15	BIT	22	B13
16	14B (14595 only)	21	B14
17	$\overline{\text{LBE}}$	20	B15
18	GND	19	B16 (LSB)

Note: “(Res)” means resolver, “(Syn)” means synchro, and “(x)” means direct.



NOTES:
1. Dimensions shown are in inches (mm).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.01(0.25) of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Package is kovar with electroless nickel plating.
5. Case is electrically floating.
6. Leads are gold coated kovar.

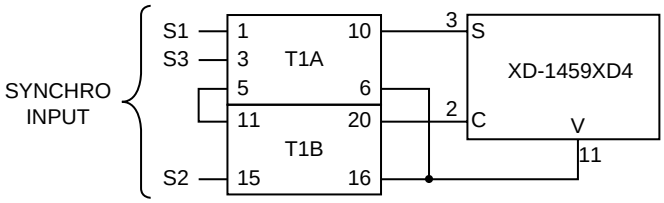
FIGURE 19. SD-14595/96/97 MECHANICAL OUTLINE 36-PIN DDIP (KOVAR)



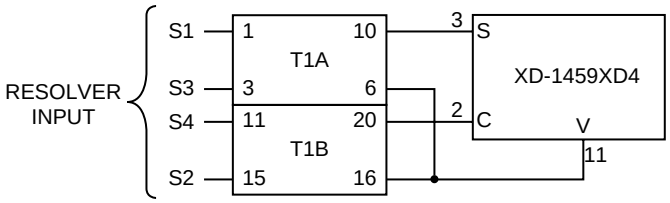
Note: Lead Cluster to be centralized about case centerline within ±.010

FIGURE 20. SD-14595/96/97 MECHANICAL OUTLINE 36-PIN FLAT PACK (CERAMIC)

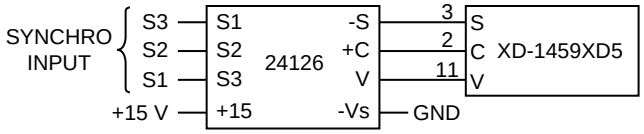
400 Hz SYNCHRO TRANSFORMER T1 21044 OR 21045



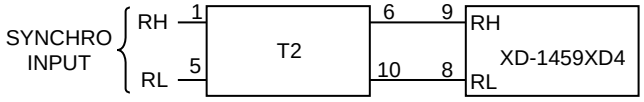
400 Hz RESOLVER TRANSFORMER T1 21046 OR 21047 OR 21048



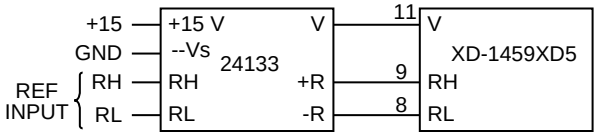
60 Hz SYNCHRO TRANSFORMER 24126 *



400 Hz REF TRANSFORMER 21049



60 Hz REF TRANSFORMER 24133



* NOTE: S3 AND S1 CONNECTIONS

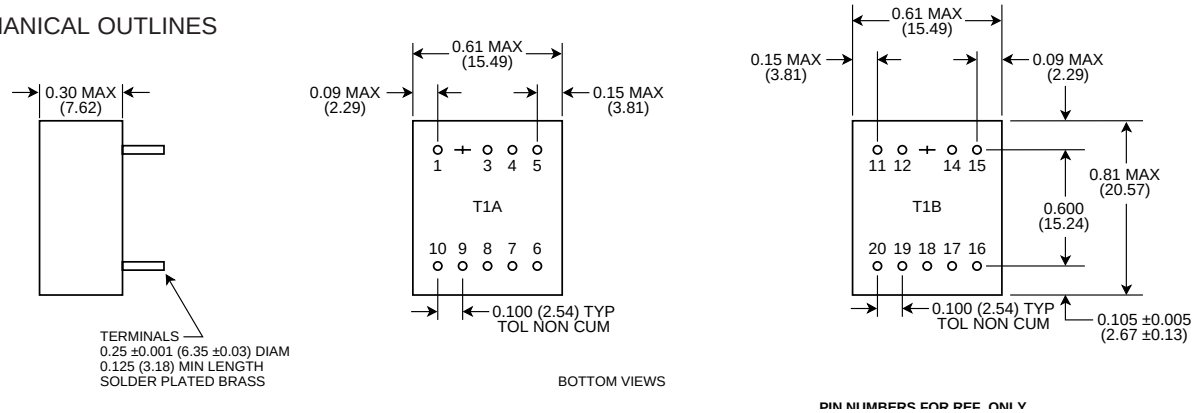
FIGURE 21. TRANSFORMER CONNECTION DIAGRAMS

These external transformers are for use with converter modules with voltage follower buffer inputs.

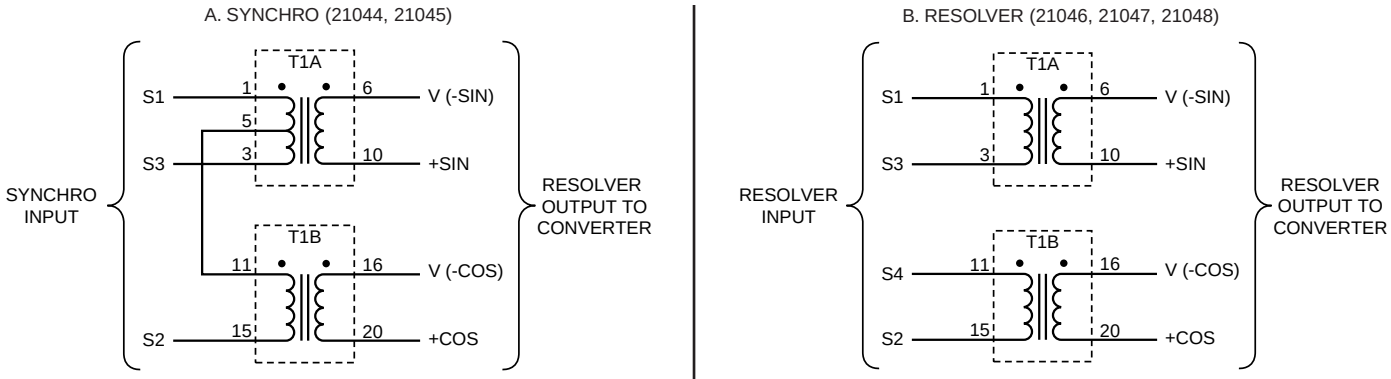
400 Hz SYNCHRO AND RESOLVER TRANSFORMER DIAGRAMS (TIA AND TIB)

EACH TRANSFORMER CONSISTS OF TWO SECTIONS, TIA AND TIB

1. MECHANICAL OUTLINES



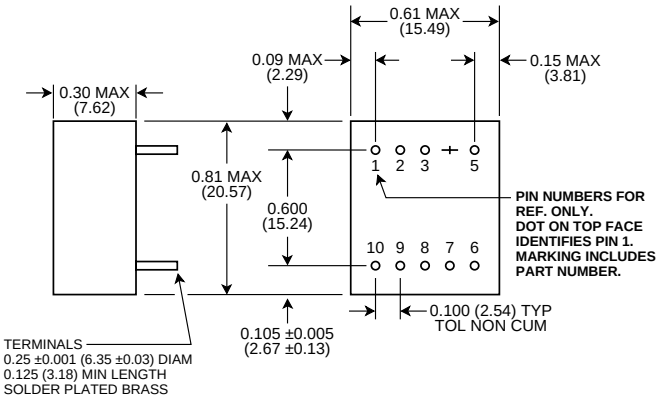
2. SCHEMATIC DIAGRAMS



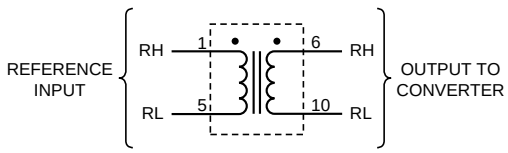
400 Hz REFERENCE TRANSFORMER DIAGRAMS (T2)

(21049)

1. MECHANICAL OUTLINE



2.SCHEMATIC DIAGRAM



60 Hz SYNCHRO AND REFERENCE TRANSFORMER DIAGRAMS

The mechanical outline is the same for the synchro input transformer (24126) and the reference input transformer (24133), except for the pins. Pins for the reference transformer are shown in parenthesis ( ) below. An asterisk (*) indicates that the pin is omitted.

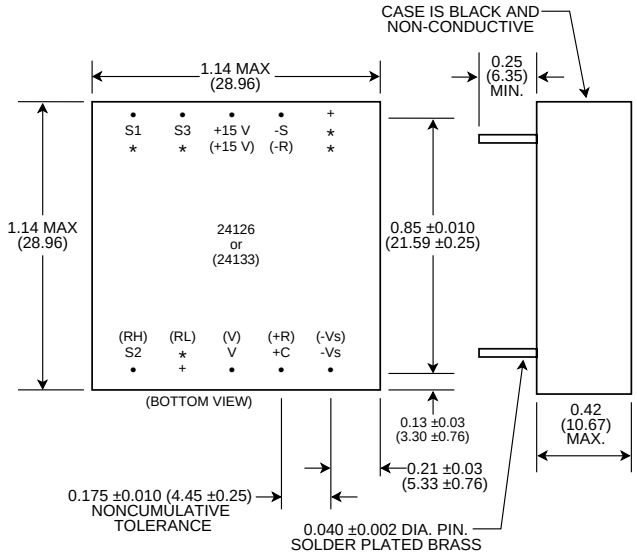


FIGURE 22. TRANSFORMER MECHANICAL OUTLINES

ORDERING INFORMATION

XX-1459XXX-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 2 = ±5.2 Minutes
- 4 = ±2.6 Minutes
- 5 = ±1.3 Minutes (16 Bit only)

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Input:
- 1 = 11.8/400 Hz (SD and RD only)
- 2 = 90/400 Hz (SD only)
- 3 = 90/60 Hz (SD only)
- 4 = Direct/400 Hz (XD only)
- 5 = Direct/60 Hz (XD only)

Package:
- D = DIP
- F = Flat Pack (Consult factory for availability.)

Resolution:
- 5 = Programmable (14 or 16 Bits)
- 6 = 14 Bit
- 7 = 16 Bit

Input Type:
- RD = Resolver Input
- SD = Synchro Input
- XD = Direct Input

*Standard DDC Processing with burn-in and full temperature test — see table below.

STANDARD DDC PROCESSING		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

TRANSFORMER ORDERING INFORMATION

Reference and signal transformers for the voltage follower buffer input converters must be ordered separately from the following table:

TYPE	FREQ.	REF. VOLTAGE	L-L VOLTAGE	PART NUMBERS	
				REF. XFMR	SIGNAL XFMR
Synchro	400 Hz	115 V	90 V	21049	21045*
Synchro	400 Hz	26 V	11.8 V	21049	21044*
Resolver	400 Hz	115 V	90 V	21049	21048*
Resolver	400 Hz	26 V	26 V	21049	21047*
Resolver	400 Hz	26 V	11.8 V	21049	21046*
Synchro†	60 Hz	115 V	90 V	24133-1 24133-3	24126-1 24126-3

* The part number for each 400 Hz synchro or resolver isolation transformer includes two separate modules as shown in the outline drawings.

† 60 Hz synchro transformers are available in two temperature ranges:
1 = -55°C to +105°C
3 = 0°C to +70°C

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Southeast - Tel: (703) 450-7900, Fax: (703) 450-6610
West Coast - Tel: (714) 895-9777, Fax: (714) 895-4988
Europe - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
Asia/Pacific - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
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