

1 Megabit 3.3V Static RAM 128K x 8-Bit

Features

- High-speed access times
Com'l: 12, 15, 17 and 20 ns
Ind'l: 15, 17 and 20 ns
- Low power operation (typical)
 - PDM31024SA
 - Active: 200 mW
 - Standby: 50 mW
- Single +3.3V ($\pm 0.3V$) power supply
- TTL-compatible inputs and outputs
- Packages
 - Plastic SOJ (300 mil) - TSO
 - Plastic SOJ (400 mil) - SO
 - Plastic TSOP - T

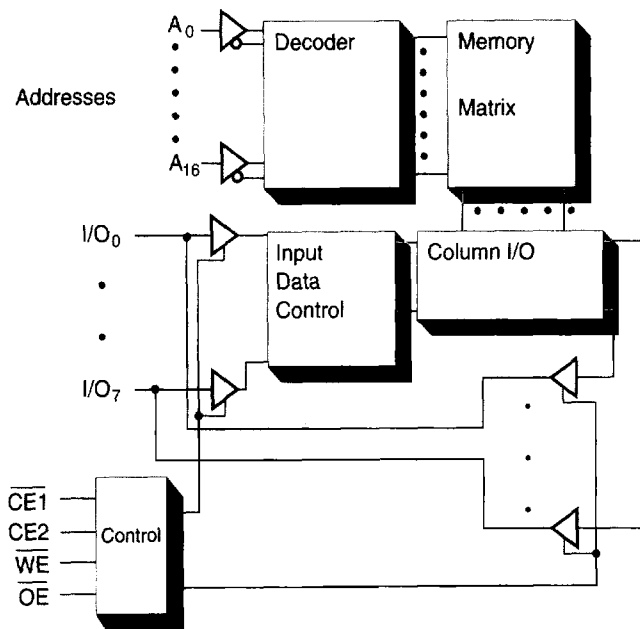
Description

The PDM31024 is a high-performance CMOS static RAM organized as 131,072 x 8 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing is accomplished when the write enable ($\overline{WE}$) and chip enable $\overline{CE1}$ inputs are both LOW and chip enable CE2 input is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ and $\overline{OE}$ are both LOW.

The PDM31024 operates from a single +3.3V power supply and all the inputs and outputs are fully TTL-compatible.

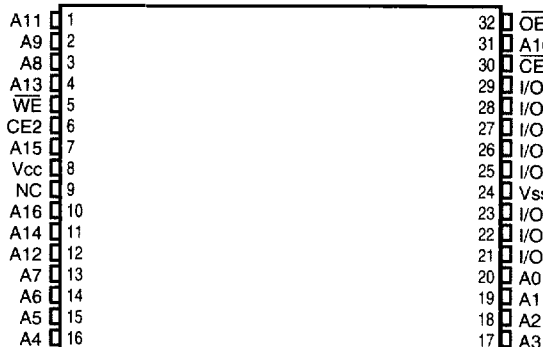
The PDM31024 is available in a 32-pin 300-mil and 400-mil plastic SOJ and a 32-pin plastic TSOP package.

Functional Block Diagram

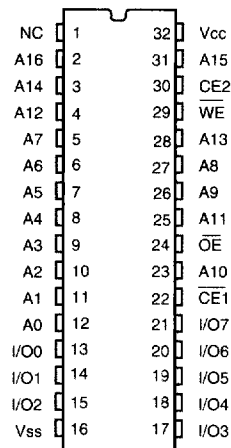


Pin Configuration

TSOP



SOJ



Pin Description

Name	Description
A16-A0	Address Inputs
I/O7-I/O0	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input
WE	Write Enable Input
CE1, CE2	Chip Enable Inputs
NC	No Connect
Vcc	Power (+3.3V)
Vss	Ground

Truth Table⁽¹⁾

$\overline{OE}$	WE	CE1	CE2	I/O	MODE
X	X	H	X	Hi-Z	Standby
X	X	X	L	Hi-Z	Standby
L	H	L	H	D _{OUT}	Read
X	L	L	H	D _{IN}	Write
H	H	L	H	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l.	Ind.	Unit
V _{TERM}	Terminal Voltage with Respect to V _{SS}	-0.5 to +4.6	-0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA
T _J	Maximum Junction Temperature ⁽²⁾	125	125	°C

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form: $T_j = T_a + P \cdot \theta_{ja}$ where T_a is the ambient temperature, P is average operating power and θ_{ja} the thermal resistance of the package. For this product, use the following θ_{ja} values:

SOJ: 72° C/W

TSOP: 95° C/W

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics ($V_{CC} = 3.3V, \pm 0.3V$)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = \text{Max.}, V_{IN} = V_{SS} \text{ to } V_{CC}$	Com'l/ Ind.	-5	5	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{Max.},$ $CE1 = V_{IH} \text{ and } CE2 = V_{IL}$ $V_{OUT} = V_{SS} \text{ to } V_{CC}$	Com'l/ Ind.	-5	5	μA
V_{IL}	Input Low Voltage			-0.3 ⁽¹⁾	0.8	V
V_{IH}	Input High Voltage			2.2	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min.}$ $I_{OL} = 10 \text{ mA}, V_{CC} = \text{Min.}$		—	0.4 0.5	V V
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$		2.4	—	V

NOTE: 1. $V_{IL}(\text{min}) = -3.0V$ for pulse width less than 20 ns

Power Supply Characteristics

Symbol	Parameter	-12	-15		-17		-20		Unit
		Com'l.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I_{CC}	Operating Current $CE1 = V_{IL} \text{ and } CE2 = V_{IH}$ $f = f_{MAX} = 1/t_{RC}$ $V_{CC} = \text{Max.}$ $I_{OUT} = 0 \text{ mA}$	130	120	120	120	120	110	110	mA
I_{SB}	Standby Current $CE1 = V_{IH} \text{ and } CE2 = V_{IL}$ $f = f_{MAX} = 1/t_{RC}$ $V_{CC} = \text{Max.}$	40	35	35	35	35	30	30	mA
I_{SB1}	Full Standby Current $CE1 \geq V_{HC} \text{ and } CE2 \leq V_{LC}$ $f = 0$ $V_{CC} = \text{Max.},$ $V_{IN} \geq V_{CC} - 0.2V \text{ or } \leq 0.2V$	10	10	15	10	15	10	15	mA

NOTES: All values are maximum guaranteed values.

 $V_{LC} \leq 0.2V, V_{HC} \geq V_{CC} - 0.2V$ Capacitance⁽¹⁾ ($T_A = +25^\circ C, f = 1.0 \text{ MHz}$)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE: 1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	2.5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

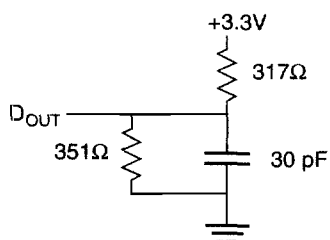


Figure 1. Output Load Equivalent

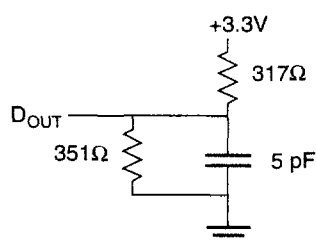
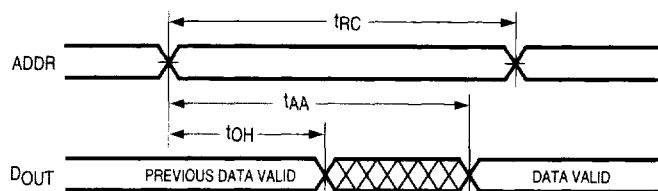
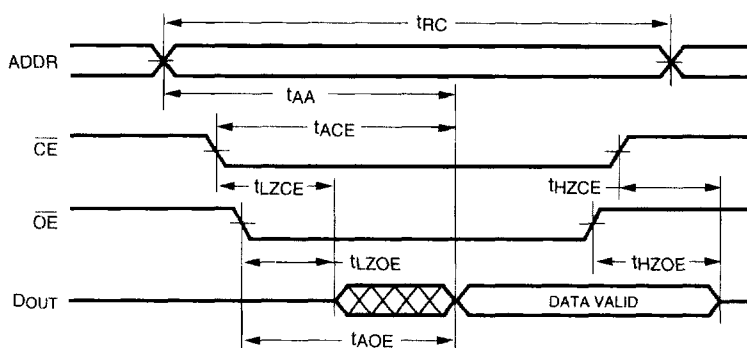


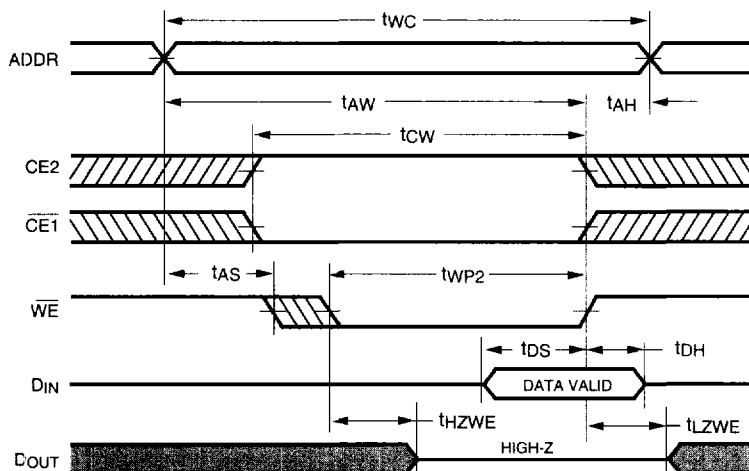
Figure 2. Output Load Equivalent
(for t_{LZCE} , t_{HZCE} , t_{LZWE} , t_{HZWE} , t_{LZOE} , t_{HZOE})

Read Cycle No. 1^(4, 5)Read Cycle No. 2^(2, 4, 6)

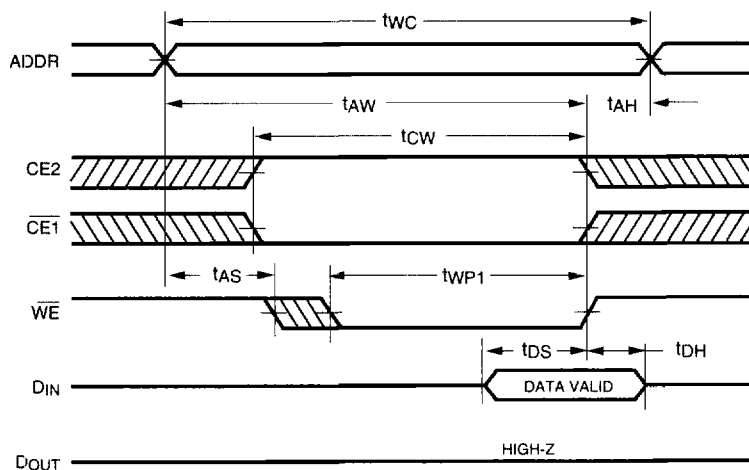
AC Electrical Characteristics

Description		-12		-15		-17		-20		
READ Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ cycle time	t_{RC}	12		15		17		20		ns
Address access time	t_{AA}		12		15		17		20	ns
Chip enable access time	t_{ACE}		12		15		17		20	ns
Output hold from address change	t_{OH}	4		4		4		4		ns
Chip enable to output in low $Z^{(1,3)}$	t_{LZCE}	5		5		5		5		ns
Chip disable to output in high $Z^{(1,2,3)}$	t_{HZCE}		6		7		7		8	ns
Chip enable to power up time ⁽³⁾	t_{PU}	0		0		0		0		ns
Chip disable to power down time ⁽³⁾	t_{PD}		12		15		17		20	ns
Output enable access time	t_{AOE}		7		8		8		10	ns
Output Enable to output in low $Z^{(1,3)}$	t_{LZOE}	0		0		0		0		ns
Output disable to output in high $Z^{(1,3)}$	t_{HZOE}		6		6		6		6	ns

Write Cycle No. 1 (Write Enable Controlled)

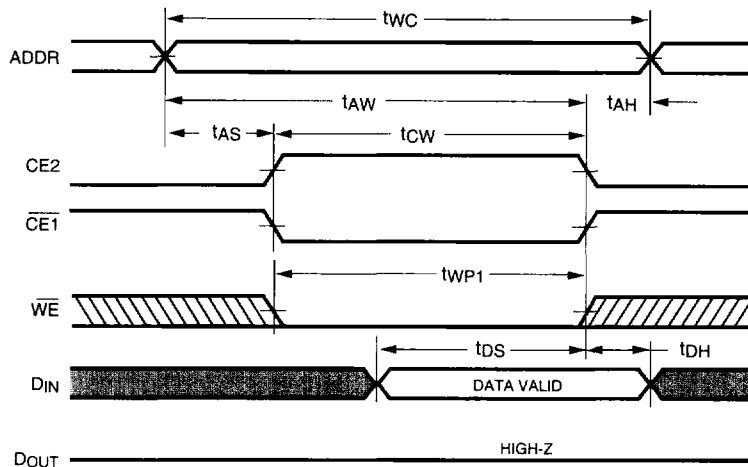


Write Cycle No. 2 (Write Enable Controlled)



NOTE: Output Enable ($\overline{OE}$) is inactive (high)

Write Cycle No. 3 (Chip Enable Controlled)



NOTE: Output Enable ($\overline{OE}$) is inactive (high)

AC Electrical Characteristics

Description		-12		-15		-17		-20		
WRITE Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
WRITE cycle time	t_{WC}	12		15		17		20		ns
Chip enable active time	t_{CW}	10		11		12		13		ns
Address valid to end of write	t_{AW}	10		11		12		13		ns
Address setup time	t_{AS}	0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		ns
Write pulse width	t_{WP1}	10		11		12		13		ns
Write pulse width	t_{WP2}	11		12		13		14		ns
Data setup time	t_{DS}	7		7		8		8		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write disable to output in low $Z^{(1,3)}$	t_{LZWE}	0		0		0		0		ns
Write enable to output in high $Z^{(1,3)}$	t_{HZWE}		7		7		7		8	ns

NOTES: (For two previous Electrical Characteristics tables)

1. The parameter is tested with $CL = 5$ pF as shown in Figure 2. Transition is measured ± 200 mV from steady state voltage.
2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} .
3. This parameter is sampled.
4. $\overline{WE}$ is high for a READ cycle.
5. The device is continuously selected. All the Chip Enables are held in their active state.
6. The address is valid prior to or coincident with the latest occurring Chip Enable.

7

Ordering Information

XXXXX	X	XX	X	X	X	
Device Type	Power	Speed	Package Type	Process Temp. Range	Preferred Shipping Container	
						Blank Tubes
						TR Tape & Reel
						TY Tray
						Blank Commercial (0° to +70°C)
						i Industrial (-40°C to +85°C)
						A Automotive (-40°C to +105°C)
						SO 32-pin 300-mil Plastic SOJ
						32-pin 400-mil Plastic SOJ
						T 32-pin Plastic TSOP
						12 Commercial Only
						15
						17
						20
						SA /S Standard Power
						PDM31024 - (128Kx8) Static RAM

Faster Memories for a FasterWorld™