FEATURES

- 64K x 4 Static RAM with Common I/O
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 15 ns maximum
- Low Power Operation
  Active: 265 mW typical at 45 ns
  Standby: 10 mW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 71258/61298, Cypress CY7C194/196
- Package Styles Available:
  - 24/28-pin Plastic DIP
  - 24/28-pin Sidebraze, Hermetic DIP
  - 24/28-pin CerDIP
  - 24/28-pin Plastic SOIC
  - 24/28-pin Plastic SOJ

DESCRIPTION

The **L7C194, L7C195,** and **L7C196** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 65,536 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C194 has a single active-low Chip Enable. The L7C195 has a single Chip Enable and an Output Enable. The L7C196 has two Chip Enables and a separate Output Enable. These devices are available in five speeds with maximum access times from 15 ns to 45 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 265 mW (typical) at 45 ns. Dissipation drops to 100 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C194, L7C195, and L7C196 consume only 1.5 mW (typical) at 3 V, allowing effective battery backup operation.

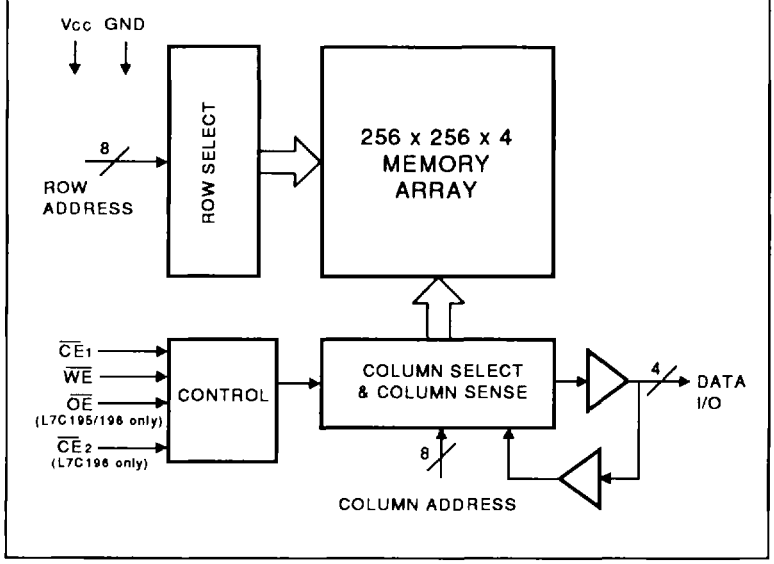
The L7C194, L7C195, and L7C196 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{15}. For the L7C194 and L7C195, reading from a designated location is accomplished by presenting an address and driving $\overline{CE}_1$ low while $\overline{WE}$ remains high. For the L7C196, both $\overline{CE}_1$ and $\overline{CE}_2$ must be low. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{OE}$ is high, or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C194, L7C195, and L7C196 can withstand an injection current of up to 200 mA on any pin without damage.

L7C194/195/196 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Military	−55°C to +125°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Military	−55°C to +125°C	$2.0\ V \le V_{CC} \le 5.5\ V$

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -4.0$ mA, $V_{CC} = 4.5$ V	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 8.0$ mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Current	$GND \le V_{IN} \le V_{CC}$	−10		+10	µA
I_{OZ}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$, $\overline{CE} = V_{CC}$	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			−350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		20	40	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		2	10	mA
I_{CC4}	V_{CC} Current, Data Retention	$V_{CC} = 3.0$ V (Note 9)		500	5000	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, $V_{CC} = 5.0$ V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

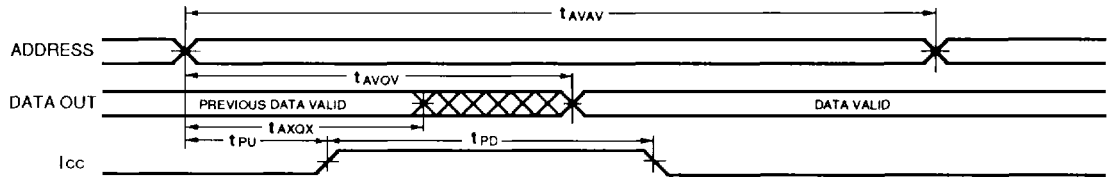
			L7C194/195/196-					
Symbol	Parameter	Test Condition	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	55	75	100	125	160	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

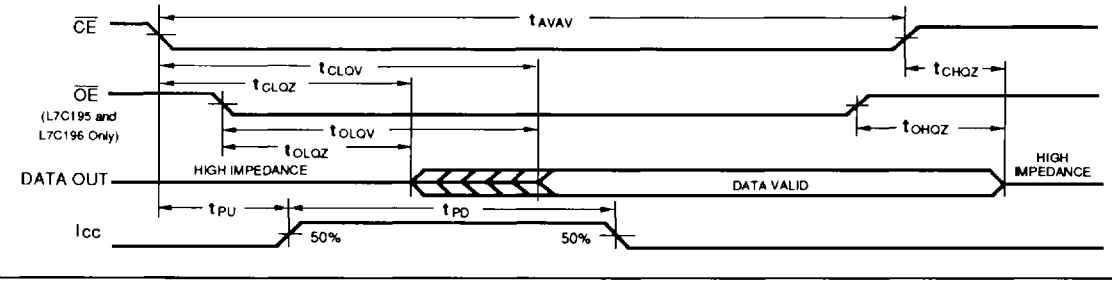
Read Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C194/195/196- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tAVAV	Read Cycle Time	45		35		25		20		15	
tAVQV	Address Valid to Output Valid (13, 14)		45		35		25		20		15
tAXQX	Address Change to Output Change	3		3		3		3		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3	
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		15		10		8		8
tOLQV	Output Enable Low to Output Valid		20		15		12		10		8
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0	
tOHQZ	Output Enable High to Output High Z (20, 21)		15		12		10		8		5
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		45		35		25		20		20
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0	

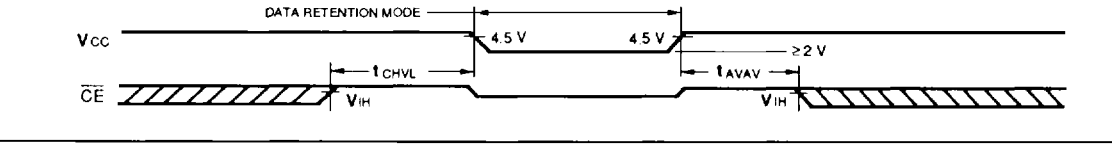
Read Cycle — Address Controlled (Notes 13, 14)



Read Cycle — $\overline{CE}$/$\overline{OE}$ Controlled (Notes 13, 15)



Data Retention

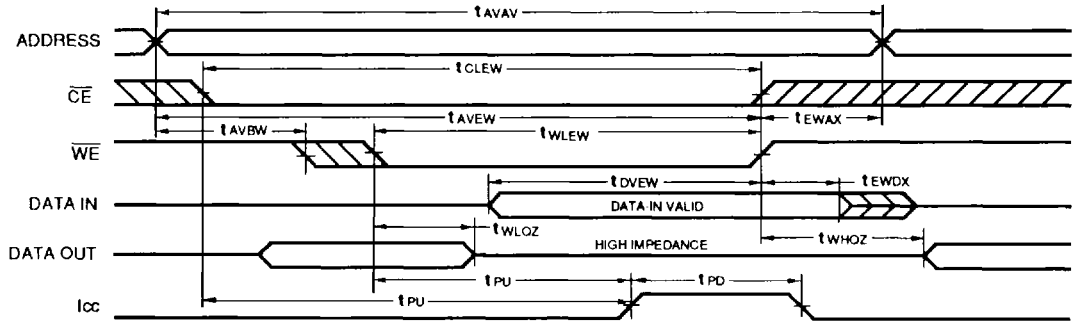


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

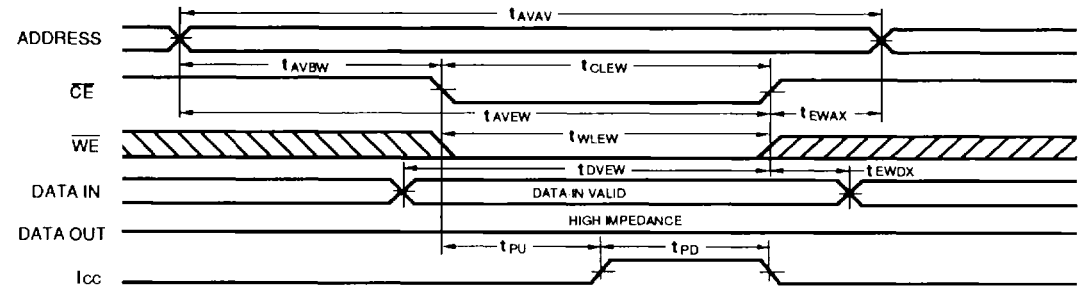
WRITE CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C194/195/196- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tAVAV	Write Cycle Time	40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	30		25		15		15		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	30		25		15		15		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		20		15		15		12	
tDVEW	Data Valid to End of Write Cycle	15		15		10		10		7	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		15		10		7		7		5

WRITE CYCLE — $\overline{WE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}^* \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}^* \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}^* = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}^*$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}^*$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}^*$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}^*$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}^*$ going low, the output remains in a high impedance state.

18. If $\overline{CE}^*$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}^*$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}^*$ active).

c. Transition on any address line ($\overline{CE}^*$ active).

d. Transition on any data line ($\overline{CE}^*$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}^*$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

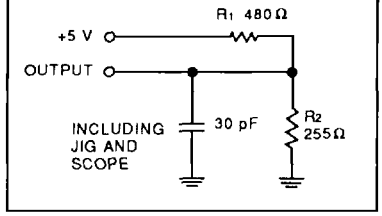


FIGURE 1b.

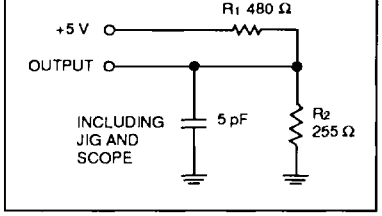
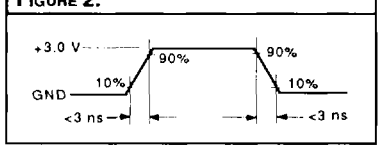


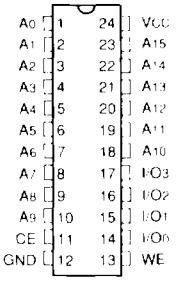
FIGURE 2.

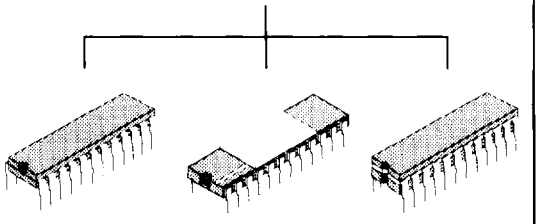


* For the L7C196, $\overline{CE}$ refers to the logical AND of $\overline{CE}_1$ and $\overline{CE}_2$.

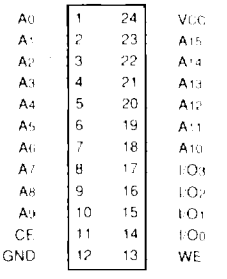
L7C194 — ORDERING INFORMATION

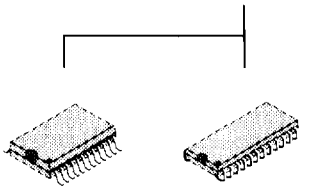
24-pin
(0.3" wide)





24-pin

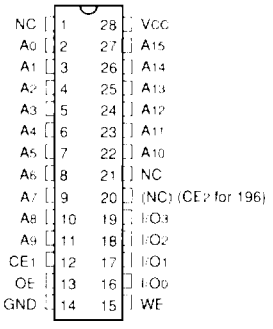


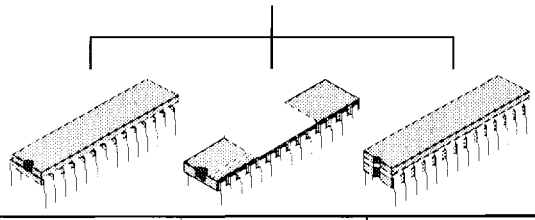


Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic SOIC (.340"— V1)	Plastic SOJ (.300"— W1)	
	0°C to +70°C — Commercial Screening					
45 ns	L7C194PC45	L7C194DC45	L7C194CC45	L7C194VC45	L7C194WC45	
35 ns	" " 35	" " 35	" " 35	" " 35	" " 35	
25 ns	" " 25	" " 25	" " 25	" " 25	" " 25	
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20	
15 ns	" " 15	" " 15	" " 15	" " 15	" " 15	
12 ns						
	–55°C to +125°C — Commercial Screening					
45 ns		L7C194DM45	L7C194CM45			
35 ns		" " 35	" " 35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns						
12 ns						
	–55°C to +125°C — Extended Screening					
45 ns		L7C194DME45	L7C194CME45			
35 ns		" " 35	" " 35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns						
12 ns						
	–55°C to +125°C — MIL-STD-883 Compliant					
45 ns		L7C194DMB45	L7C194CMB45			
35 ns		" " 35	" " 35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns						
12 ns						

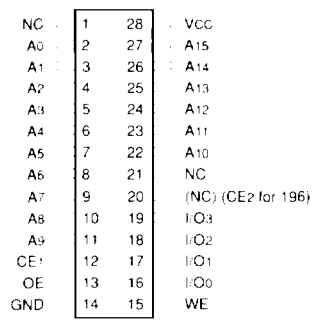
L7C195/196 — ORDERING INFORMATION

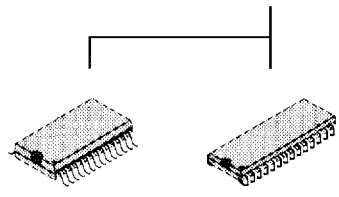
28-pin
(0.3" wide)





28-pin





Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	CerDIP (C5)	Plastic SOIC (.340"— V2)	Plastic SOJ (.300"— W2)	
	0°C to +70°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns	L7C195PC / L7C196PC — 45, 35, 25, 20, 15	L7C195DC / L7C196DC — 45, 35, 25, 20, 15	L7C195CC / L7C196CC — 45, 35, 25, 20, 15	L7C195VC / L7C196VC — 45, 35, 25, 20, 15	L7C195WC / L7C196WC — 45, 35, 25, 20, 15	
	–55°C to +125°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C195DM / L7C196DM — 45, 35, 25, 20	L7C195CM / L7C196CM — 45, 35, 25, 20			
	–55°C to +125°C — Extended Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C195DME / L7C196DME — 45, 35, 25, 20	L7C195CME / L7C196CME — 45, 35, 25, 20			
	–55°C to +125°C — MIL-STD-883 Compliant					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C195DMB / L7C196DMB — 45, 35, 25, 20	L7C195CMB / L7C196CMB — 45, 35, 25, 20			