GoldStar
GOLDSTAR ELECTRON CO., LTD.

GMM7401000S/SG-60/70/80
1,048,576 WORDS × 40 BIT
GMM7402000S/SG-60/70/80
2,097,152 WORDS × 40 BIT
CMOS DYNAMIC RAM MODULE

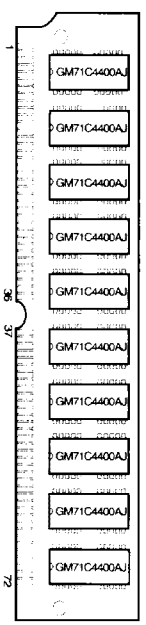
Description

The GMM7401000S/SG is a 1M×40 bits dynamic RAM MODULE which is assembled 10 pieces of 1M×4 bit DRAMs in 20/26 pin SOJ package on single side the printed circuit board with decoupling capacitors.

The GMM7402000S/SG is a 2M×40 bits dynamic RAM MODULE which is assembled 20 pieces of 1M×4 bit DRAMs in 20/26 pin SOJ package on both sides the printed circuit board with decoupling capacitors.

These are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. These provide common data inputs and outputs.

GMM7401000S/SG (Single side)
GMM7402000S/SG (Both side)



Features

- 72 pins Single In-Line Package
  - —GMM740XXXXS: Tin-Lead Plate
  - —GMM740XXXXSG: Gold Plate
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM74000S/SG-60	60	15	110	40
GMM74000S/SG-70	70	20	130	45
GMM74000S/SG-80	80	20	150	50

- Low Power
  Active
  - — 1M×40: 6,050/5,500/4,950 mW(MAX)
  - — 2M×40: 6,160/5,610/5,060 mW(MAX)

  Standby
  - — 1M×40: 55 mW(CMOS level: MAX)
  - — 2M×40: 110 mW(CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden Refresh
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16 ms

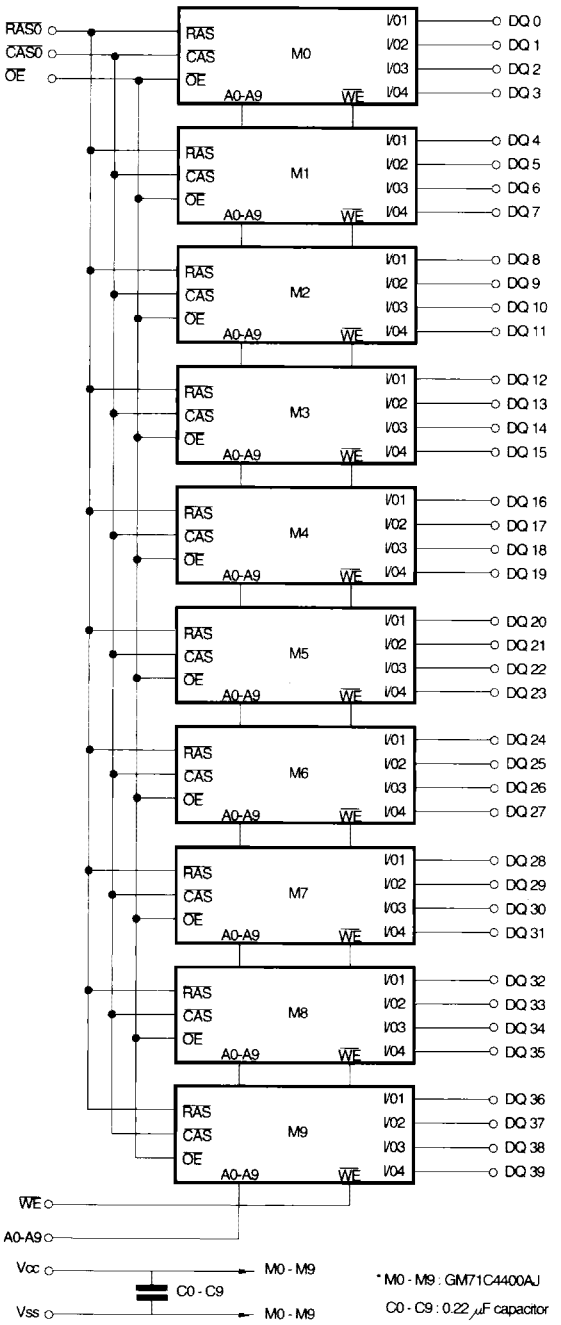
Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	19	$\overline{OE}$	37	DQ_{33}	55	DQ_{11}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	$\overline{CAS_0}$	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	NC	59	V_{CC}
6	DQ_2	24	DQ_6	42	NC	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	$\overline{CAS_1}$ *1	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS_0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS_1}$ *1	63	DQ_{14}
10	V_{CC}	28	A_7	46	DQ_{37}	64	DQ_{31}
11	NC	29	DQ_{36}	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{CC}	48	V_{SS}	66	DQ_{38}
13	A_1	31	A_8	49	DQ_8	67	PD_1
14	A_2	32	A_9	50	DQ_{24}	68	PD_2
15	A_3	33	NC	51	DQ_9	69	PD_3
16	A_4	34	NC	52	DQ_{25}	70	PD_4
17	A_5	35	DQ_{34}	53	DQ_{10}	71	DQ_{39}
18	A_6	36	DQ_{32}	54	DQ_{26}	72	V_{SS}

Note 1. In case of GMM7401000S/SG these are not connected.

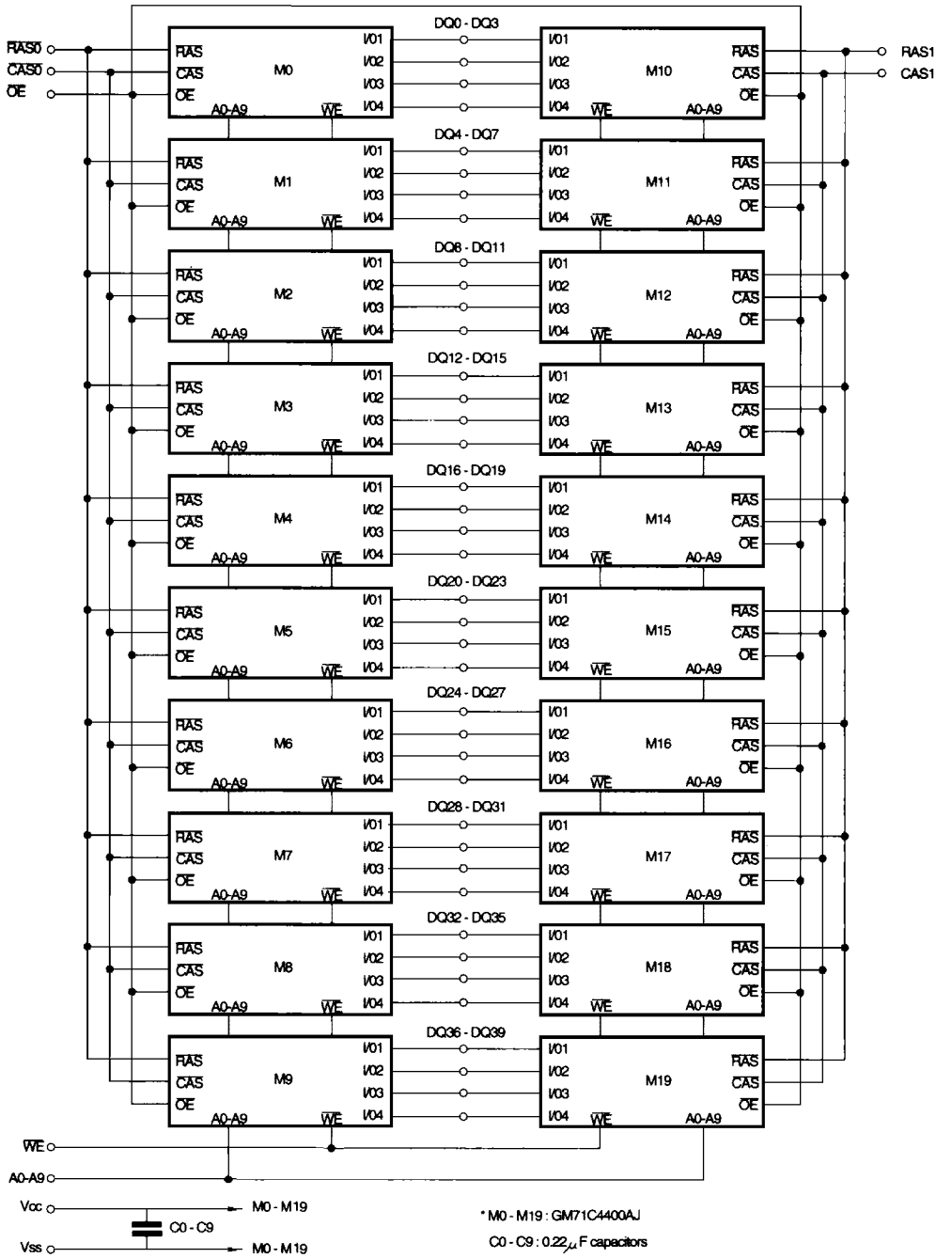
Block Diagram

• GMM7401000S/SG



Block Diagram

- **GMM7402000S/SG**



Pin Description

Pin	Function	Pin	Function
$A_0 \sim A_9$	Address Inputs	PD1 ~ PD4	Presence Detect
$DQ_0 \sim DQ_{39}$	Data Input/Output	V_{CC}	Power (+5V)
$\overline{RAS0}$, $\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS0}$, $\overline{CAS}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Read/Write Enable	$\overline{OE}$	Output Enable

Presence Detect Pins

• **GMM7401000S/SG**

Pin	60ns	70ns	80ns
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

• **GMM7402000S/SG**

Pin	60ns	70ns	80ns
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

Absolute Maximum Ratings*[1]

Symbol	Parameter	Values	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature	-55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0 ~ 7.0	V
V_{CC}	Power Supply Voltage	-1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	10/20*[2]	W

*Note: 1. Stress greater than above under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. GMM7402000S/SG

Recommended DC Operating Conditions ($T_A = 0 \sim 70°C$)

Symbol	Parameter	MIN	TYP	MAX	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	–	6.5	V	1
V_{IL}	Input Low Voltage	-1.0	–	0.8	V	1

Note: 1. All voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		GMM7401000S/SG		GMM7402000S/SG		Unit	Note
			Min	Max	Min	Max		
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	V_{CC}	2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	1100	—	1120	mA	1,2
		70ns	—	1000	—	1020		
		80ns	—	900	—	920		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	20	—	40	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	1100	—	1120	mA	2
		70ns	—	1000	—	1020		
		80ns	—	900	—	920		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	1100	—	1120	mA	1,3
		70ns	—	1000	—	1020		
		80ns	—	900	—	920		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} - 0.2V)		—	10	—	20	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	1100	—	1120	mA	
		70ns	—	1000	—	1020		
		80ns	—	900	—	920		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	50	—	100	mA	1
$I_{I(L)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 7V$) All Other Pins Not Under Test = 0V		-100	100	-200	200	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 7V$)		-10	10	-20	20	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, T_A = 25°C, f = 1MHz)

Symbol	Parameter	GMM7401000S/SG		GMM7402000S/SG		Unit	Notes
		Min	Max	Min	Max		
C_{I1}	Input Capacitance (A0 ~ A9)	—	85	—	130	pF	1
C_{I2}	Input Capacitance ($\overline{WE}$, $\overline{OE}$)	—	85	—	160	pF	1,2
C_{I3}	Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$)	—	85	—	90	pF	1,2
C_{I4}	Input Capacitance ($\overline{CAS0}$, $\overline{CAS1}$)	—	85	—	90	pF	1,2
CDQ_I	I/O Capacitance	—	20	—	25	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C, Notes 1, 14)

Refer to the GM71C4400A/AL Data Sheet for Timing Waveforms.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read/Write or Write Cycle Time	110	—	130	—	150	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	16	—	16	—	16	ms	

Read Cycle

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	20	ns	3,4
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	0	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	ns	
t_{OFF}	Output Buffer Turn-off Time	—	15	—	20	—	20	ns	6

Write Cycle

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	10	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	20	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	ns	11

Refresh Cycle

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	50	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	—	45	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	45	—	ns	

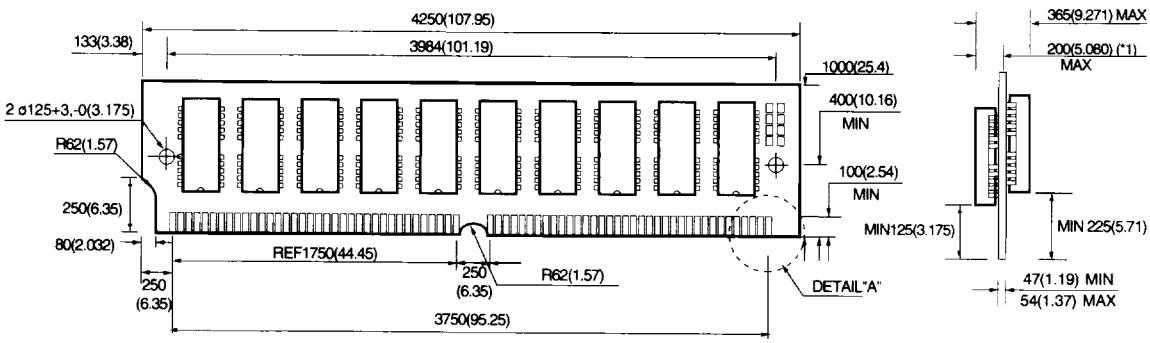
Notes :

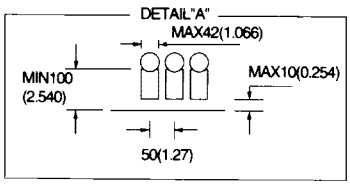
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, is not rrestrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Package Dimensions

GMM7401000S/SG(*1)
GMM7402000S/SG

Unit: mil (mm)





Tolerance : ±5(0.127) Unless otherwise Specified.