88EM8080/88EM8081

LED Power Supply Controller for Flyback Converters with Power Factor Correction

Datasheet

Customer Use

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Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary Information	Technical Publication: 0.xx

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PRODUCT OVERVIEW

The Marvell® 88EM8080/88EM8081 device is a high performance LED power supply controller for flyback converters with output regulation and power factor correction. The 88EM8080/8081 control algorithm uses Average Current Mode Control (ACMC) for power factor correction (PFC) in LED lighting applications with low harmonic distortion and good noise immunity. The Marvell proprietary adaptive loop control achieves high power factor under high input voltage and low load conditions. Through Marvell's innovative digital signal processing (DSP) solution, the LED controller with the PFC function provides the customer with the smallest package, the lowest system cost, the lowest total harmonic distortion (THD) and the best power factor for LED lighting applications.

Both devices work at fixed frequencies, 88EM8080 at 60kHz while 88EM8081 at 120kHz. The IC operates under Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) or both combined together operating in Mixed Mode. The internal voltage loop compensation and current loop control guarantee system stability and thus reduce the exernal component count and costs.

The 8-pin SOIC package further facilitates the application design process by saving board space. The resultant simple system design and minimum cost makes 88EM8080/88EM8081 the ideal choice for LED applications with PFC. Figure 1 shows a reference schematic for a universal isolated LED driver with PFC using the 88EM8080/88EM8081 device.

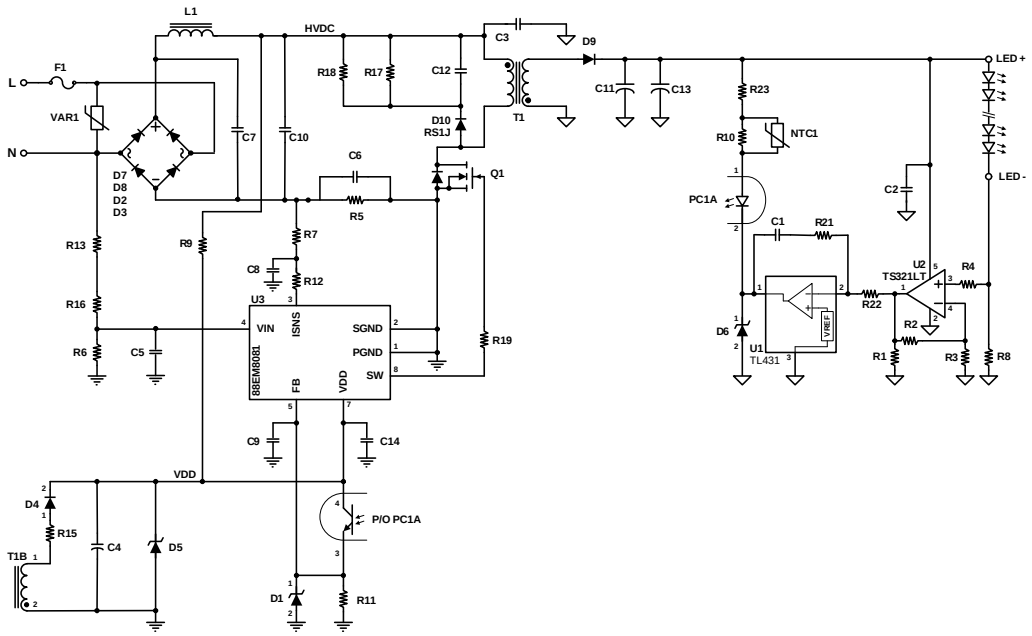
General Features

- **Mixed Mode – CCM and DCM operation**
- **Average current mode control**
- **Adaptive control loop achieves high power factor and low THD for a wide range of voltage and load conditions**
- **Adaptive over current protection for universal voltage**
- Fixed switching frequency
- 1.2A (typical) driver capability
- Minimal external components required
- Under voltage lockout (UVLO)
- Over voltage protection (OVP)
- Thermal shutdown
- Input line frequency range from 45Hz to 65Hz

Applications

- LED home and facility lighting
- LED street lamps

Figure 1: Universal Isolated LED Driver with PFC



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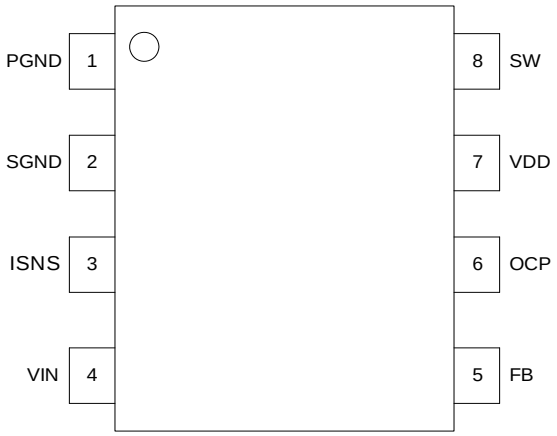

1.2 Pin Descriptions

Table 1: Pin Definitions

Pin #	Pin Name	Pin Type	Pin Description
1	PGND	GND	Power Ground
2	SGND	GND	Signal Ground
3	ISNS	Input	Current Sense
4	VIN	Input	Voltage Input
5	FB	Input	Feedback
6	OCP	Input	Over Current Protection
7	VDD	Supply	IC Supply Voltage
8	SW	Output	Switch

Table 2: Pin Descriptions

Pin #	Pin Name	Pin Function
1	PGND	**Power Ground** • Connected to the source of the primary MOSFET. • The PCB trace from the power ground to the source of the primary MOSFET must be kept as short as possible. • To avoid any switching noise interruption on signal processing, PGND and SGND remain seperate inside the IC.
2	SGND	**Signal Ground** • Must be connected to the power ground with the Kelvin sensing connection (typically connected to the source of the external MOSFET) so that SGND has dedicated trace and connections and provides clean signal integrity. • To avoid any switching noise interruption on signal processing, SGND and PGND remain seperate inside the IC.
3	ISNS	**Current Sense** • Used for current shaping and for over current protection. • Sense resistor varies for different loads. Examples - 0.15Ω at 120W rated load and 0.6Ω for 30W rated load.
4	VIN	**Voltage Input** • Connects to resistance divider at input AC line “phase” to GND. Voltage applied is a half rectified sine wave scaled down by the input resistance divider. • Voltage input pin is a high impedance input pin. An impedance of 2M (typical) is recommended to be designed from the input AC “phase” to GND for the VIN resistor dividor network to reduce the standby power. Higher impedance is preferred with the right PCB design on this pin signal. • This voltage input after comparing with an internal threshold reference is used to detect the zero-cross location of the input sine wave and is also used to synthesize (regenerate) the input sine wave. This regenerated sine wave is used for the current reference. • Brown-out protection function is also provided by this pin. A resistor devider with a 100:1 ratio from the highside resistor to the lowside resistor is corresponding to a “brown-out protection” input voltage of 50V (RMS). Increasing that ratio will increase the “brown-out voltage”. Brown-out voltage is determined by R_6, R_{13} and R_{16} as shown in Figure 1. Refer to Section 5.2 for further understanding.
5	FB	**Feedback** • The output voltage of 100% rated value is scaled to 2.5V at the FB Pin. • Transition from soft-start to normal regulation is at 87.5% rated V_{FB}. When FB pin voltage exceeds V_{FB_OVP}, the IC shuts down the SW pin driver pulse. SW pin driver pulse recovers when FB pin falls below the reference voltage, V_{FB_REG}. • There is another OVP latch threshold ($V_{FB\_OVP\_LATCH}$) of 3.77V on the FB pin. When FB exceeds $V_{FB\_OVP\_LATCH}$, latched over voltage shutdown occurs until another VDD power on resets the latch. • The effective resistance between FB and GND is 200k (typical).
6	OCP	**Over Current Protection** • Used to turn off the MOSFET when it is pulled as logic low

Table 2: Pin Descriptions

Pin #	Pin Name	Pin Function
7	VDD	**IC Supply Voltage** • Nominal voltage is 12V and the Under Voltage Lock Out (UVLO) occurs when $V_{DD} < V_{DD\_UVLO}$ and the IC is turned off. • The IC is turned on whenever $V_{DD} > V_{DD\_ON}$ (typ. 11.9V). • The maximum voltage on VDD is 16V. • VDD should be clamped by a zener for protection in the system design. Refer to Table 4 for more details.
8	SW	**Switch** • PWM gate signal for the switch. • It should be connected to the gate of external MOSFET through a gate resistor.

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2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings[1]

NOTE: Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Units
V_{DD}	Power Supply (Voltage to PGND=SGND)	-0.3	18	V
V_{Isns}	Voltage at ISNS pin	-0.5	0.5	V
V_{OCP}	Voltage at OCP pin	-0.3	5.5	V
V_{VIN}	Voltage at VIN pin	-0.3	5.5	V
V_{FB}	Voltage at FB pin	-0.3	5.5	V
I_{SW}	Driver Current (Instantaneous Peak)		2	A
θ_{JA}	Thermal Resistance		156.5	°C/W
T_A	Operating Ambient Temperature Range[2]	-40	85	°C
T_J	Maximum Junction Temperature		125	°C
T_{STOR}	Storage Temperature Range	-65	150	°C
V_{ESD}	ESD Rating[3]		2	kV

1. Exceeding the absolute maximum rating may damage the device.
2. Specifications over the -40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.
3. Devices are ESD sensitive. Handling precautions recommended. Human Body model, 1.5kΩ in series with 100pF.

2.2 Electrical Characteristics

Table 4: Electrical Characteristics

NOTE: A 12V supply voltage is applied and the ambient temperature (T_A) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD} Supply						
V_{DD}	Supply Voltage		7.0	12	16	V
V_{DD_ON}	V_{DD} Power On Threshold			11.9		V
V_{DD_UVLO}	V_{DD} Power Off Threshold (UVLO)	After V_{DD} is powered up and running		7.0		V
$V_{DD\_UVLO\_HYS}$	V_{DD_UVLO} Hysteresis		4.8		5	V
I_{DD_QST}	V_{DD} Quiescent Current[1]	V_{DD} = 12V		95		µA
I_{DD_OP}	V_{DD} Operating Current	V_{DD} = 12V; C_{Gate} = 1nF F_{SW} = 118kHz V_{IN}=0		5.2		mA
Thermal Shutdown						
T_{SD}	Thermal Shutdown			150		°C
T_{SD_HYS}	Hysteresis for Thermal Shutdown		25			°C
Output Gate Driver						
V_{G_HI}	Minimum Gate High Voltage[2]	V_{DD} = 12V C_{Gate} = 1nF Sourcing 500mA	10.0			V
V_{G_LO}	Maximum Gate Low Voltage[3]	V_{DD} = 12V C_{Gate} = 1nF Sinking 500mA			2.0	V
R_{DSON}	Gate Drive Resistance	Sourcing 120mA T=25°C		2.4		Ω
	Gate Drive Resistance	Sinking 120mA T=25°C		2.0		Ω
I_{SW_PK}	Driver Peak Current	C_{Gate} = 10nF V_{DD} = 12V		1.2		A
t_R	Rise Time	C_{Gate} = 1 nF		35		ns
		C_{Gate} = 10 nF		125		ns
t_F	Fall Time	C_{Gate} = 1 nF		35		ns
		C_{Gate} = 10 nF		145		ns
D_{MAX}	Maximum Duty Cycle				88	%

Table 4: Electrical Characteristics (Continued)

NOTE: A 12V supply voltage is applied and the ambient temperature (T_A) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
D_{MIN}	Minimum Duty Cycle[4]		3			%
Feedback/Overvoltage						
V_{FB_REG}	Normal Regulation Reference	IC powered on		2.55		V
V_{FB_OVP}	Over Voltage Protection Threshold	At 120% of V_{FB_REG}.		3.04		V
$V_{FB\_OVP\_HYS}$	Over Voltage Protection Hysteresis			0.49		V
$V_{FB\_OVP\_LATCH}$	Over Voltage Protection Latch			3.77		V
Current Sensing and Current Protection[5]						
V_{IOVER_TH1}	Over Current Threshold Zone 1[6]	Peak value of half-sine voltage at V_{IN}: $1.26<V_{IN}<1.89V_{pk}$[7]		397		mV
V_{IOVER_TH2}	Over Current Threshold Zone 2[5]	Peak value of half-sine voltage at V_{IN}: $1.89<V_{IN}<2.59V_{pk}$[8]		329		mV
V_{IOVER_TH3}	Over Current Threshold Zone 3[5]	Peak value of half-sine voltage at V_{IN}: $2.59< V_{IN}<3.43V_{pk}$[9]		269		mV
V_{IOVER_TH4}	Over Current Threshold Zone 4[5]	Peak value of half-sine voltage at V_{IN}: $3.43<V_{IN}<3.85V_{pk}$[10]		202		mV
V_{IOVER_CYC}	Cycle by cycle current protection logic input (OCP pin) threshold for SW on[11]			1.68		V
88EM8080 Switching Frequency Oscillator						
F_{SW}	Frequency (Average Mode)			59		kHz
88EM8081 Switching Frequency Oscillator						
F_{SW}	Frequency (Average Mode)			118		kHz

1. V_{DD} Quiescent Current: V_{DD} power supply current before V_{DD} first time reaches V_{DD_ON}.

2. Considering the voltage drop on the internal driver MOSFET during current sourcing.

3. Considering the voltage drop on the internal driver MOSFET during current sinking.

4. If the duty cycle is less than 3% from the DSP calculations, one PWM cycle is skipped and this duty-cycle value is added to the next PWM duty cycle calculation.

5. To achieve almost constant power limit for the universal input range, current protection self-adjusts thresholds in four zones of input voltage levels. A margin of 50% compared to the rated current is considered for the threshold current values.

6. Threshold of negative voltage drop across R_{sns} due to instantaneous current

7. With input divider ratio of 1/100, these values are equivalent to 90 V_{rms}<V_{line}<135 V_{rms}. (Section 5.2, equation (1))

8. With input divider ratio of 1/100, these values are equivalent to 135 V_{rms}<V_{line}<185 V_{rms}. (Section 5.2, equation (1))

9. With input divider ratio of 1/100, these values are equivalent to 185 V_{rms}<V_{line}<245 V_{rms}. (Section 5.2, equation (1))

10. With input divider ratio of 1/100, these values are equivalent to 245 V_{rms}<V_{line}<275 V_{rms}. (Section 5.2, equation (1))

11. OCP falling threshold for V_{IOVER_CYC} is 1V with a hysteresis of 0.68V.

3 Functional Description

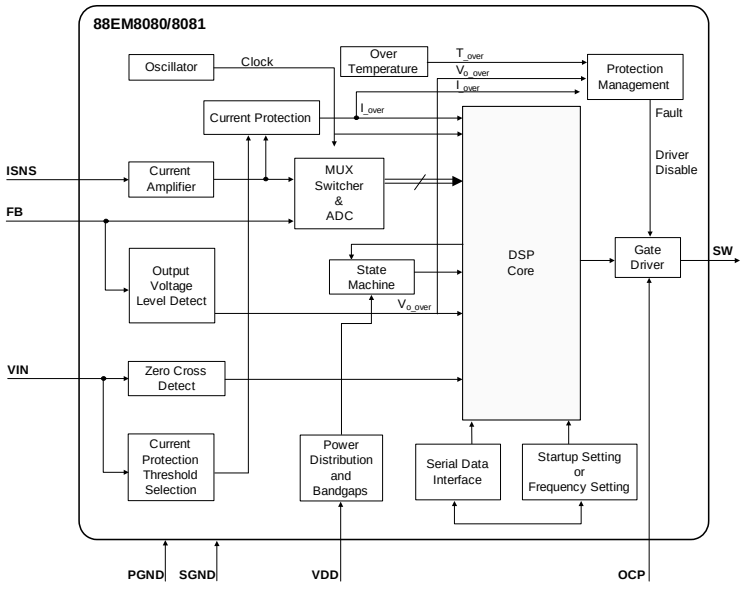
3.1 Overview

The 88EM8080/88EM8081 is a high-performance power factor correction controller for single stage flyback LED lighting applications with a minimum number of components at a low cost. The following section outlines the functions of various input and output signals of the 88EM8080/88EM8081 device as listed below in Table 5 .

Table 5: Functional Summary

Section	Pin Name	Function
Section 3.2	VDD	Bias power for IC
Section 3.3	PGND/SGND	Power and signal ground is the return for power and signals
Section 3.4	SW	Gate drive output
Section 3.5	VIN	Input voltage sensing and brown-out protection
Section 3.6	FB	Inverting input of an internal error amplifier used for regulation of output voltage / current
Section 3.7	ISNS	Input current sensing used for providing PFC and for adaptive over current protection
Section 3.7.3	OCP	Over current protection used for cycle by cycle protection

Figure 3: Top Level Block Diagram



Note

- I_{over}, V_{o_over}, and T_{over} are the over current, over voltage, and over temperature signals respectively.

3.2 VDD – Bias Power Input

The controller needs bias power which is recieved through the VDD and PGND pins. The nominal voltage for the VDD pin is around 12 Volts and the IC will start switching as long as the VDD voltage exceeds the V_{DD_ON} Power-on threshold described in Table 4, Electrical Characteristics, on page 16. The PWM switched output at the SW pin is available after the IC is switched on. Once powered up and switching has started, the VDD voltage can reach as low as 7 Volts (typical), at which point the IC is switched off. This 7 volt threshold is the under voltage lockout (UVLO) value. Once VDD goes below the UVLO threshold voltage, VDD must climb back to the V_{DD_ON} threshold to start switching once again. The maximum voltage needs to be less than 16 volts which provides some margin from an absolute maximum VDD voltage rating of 18 Volts. When the IC is not switching (less than 12 volts before turn-on and less than 7 volts after turn-on), the 88EM8080/88EM8081 draws very little quiescent current which has a typical rating of 95µA. During switching, the operating current from the VDD source is around 5.2mA.

From a circuit design point of view, bias can be provided initially from the rectified low frequency AC input. Once the IC starts switching, bias power can be derived from the high frequency part of the circuit. As an example, an auxiliary winding on the flyback transformer can be used to provide this high frequency power. It is necessary to rectify the high frequency AC from the auxiliary winding and to have necessary filtering to reduce the high frequency ripple at the VDD pin. This approach of providing high frequency bias power after turn-on will improve the efficiency of the bias power circuitry in the steady state. It should be noted that during startup, at the instant of switching, the current drawn by the chip increases from 95µA to 5.2mA (typical). This sudden step load of bias power will tend to decrease the VDD voltage. If the VDD voltage falls below 7 volts due to this reason, the IC will go through another starting cycle. To prevent this hiccup, adequate energy storage (capacitor) needs to be provided. The capacitors across VDD and PGND will help to keep the VDD voltage above 7 volts.

Care is also needed in the design of bias power circuit from the rectified low frequency AC side. If a simple resistance is used to charge the capacitor across VDD and PGND, the turn-on time could be longer. Variations in the bias circuit design may be accommodated to meet the specified turn-on time.

The under voltage lockout (UVLO) feature can be used to shut off the IC during a fault condition by forcing the VDD voltage to go below 7 volts. If the fault is removed, VDD voltage can be allowed to increase to VDD_ON and the IC will go through a new starting cycle.

3.3 PGND and SGND

The 88EM8080/88EM8081 has separated the power ground pin (PGND) and signal ground pin (SGND) inside the IC to avoid any noise interruption during signal processing. The PGND pin should be connected to the primary MOSFET source pin and the connection trace should be as short as possible. The SGND must be connected to the PGND through a Kelvin sensing connection trace to achieve a clean signal ground.

3.4 SW – Switched PWM Output for Gate Drive

The SW pin is the PWM output pin for the IC. The IC has an internal totem pole drive circuit to drive the gate of an external power MOSFET through this SW pin. A gate resistor is recommended to provide damping in the external drive circuit and to minimize the parasitic ringing. The PWM output gate drive capibility is 1.2A (typical). If necessary, additional drive circuitry along with speed up circuitry can be added to the SW pin output for very high power levels.

3.5 VIN – Input Voltage Sensing

The PFC function is implemented by sensing the input current waveform and forcing the average of the input current to follow the input voltage sinusoidal waveform. A resistor divider is used between AC input and a primary reference ground to sense the input voltage. The primary reference ground is connected to the 88EM8080/88EM8081 IC reference ground and to the source pin of the external switching MOSFET Q1 as in Figure 1, Universal Isolated LED Driver with PFC, on page 3. The output of the resistor divider which is a half sinusoidal waveform is the input to the VIN pin. By sensing the input voltage waveform at the VIN pin, the controller can generate its own internal sinusoidal reference at the same frequency as the input. This is done by having an internal DC threshold (0.72 Volts), a comparator and a zero-cross detection circuit. The details of the calculations are described in Section 5.2.

It is recommended to use a high impedance divider network between the AC line to reference AC ground to sense the input voltage at the VIN pin. This will help to reduce the no load input power and will improve the efficiency in general. Due to the VIN pin being a high impedance input pin, a 10nF (typical) decoupling noise capacitor between it and ground is required.

3.5.1 Brown-out Protection

VIN pin is also used for the brown-out protection function. A resistor divider of 100:1 ratio from the high voltage side corresponds to a brown-out protection input voltage of around 50V RMS for the defined internal threshold of 0.72 Volts. Increasing the high voltage divider turns ratio will increase brown-out protection voltage.

3.6 FB – Output Voltage / Current Feedback

The 88EM8080/88EM8081 has an internal current loop and output voltage/current loop to implement the PFC and the output voltage/current regulating function. FB pin is the inverting input of a voltage error amplifier with 2.5 volts as the internal reference voltage. For steady state operation 100% of required output voltage/current is scaled to 2.5V at the feedback pin by external circuitry. For output current regulation, the much smaller voltage across the load current sensing resistor could be amplified to be 2.5V and then applied to the FB pin.

During startup, when FB pin is below 87.5% of the reference voltage, the PFC controller operates in soft-start mode. The internal voltage error amplifier switches over to normal regulation phase once the FB pin voltage reaches 87.5% of the reference value.

3.6.1 FB – Over Voltage Protection (OVP)

Over voltage protection is implemented through the FB pin. When the FB pin voltage exceeds VFB_OVP threshold voltage (refer to Table 4, Electrical Characteristics, on page 16), the IC is switched off and no PWM output is available at SW pin of the IC.

3.6.2 FB – Regulation

3.6.2.1 Output Current Regulation - Isolated Output

The general application for 88EM8080/88EM8081 is for LED current control. The LED current is passed through a series sense resistor and the voltage across that resistor is proportional to the LED current. This sense resistor needs to be very small to limit the power dissipation in the resistor. The sensed voltage is then amplified to have 2.5V at the full load current. It is applied to the TL431 type of device where the error voltage between the amplified voltage and TL431 device reference (2.5V) is amplified. An optocoupler can be used to pass the error information to the feedback pin FB on the primary side. In addition the primary current is sensed and the average current is adjusted to be sinusoidal (in phase with AC input Voltage). The amplitude of the primary current is adjusted to make the secondary LED current constant at the desired level. Because this is a single stage PFC there will be second harmonic ripple at the output. Output capacitors are added to reduce the output second harmonic ripple and also the high frequency switching ripple. The proportional and integral compensation within the IC make the system stable. The over voltage protection at the output can be achieved by clamping the output of TL431.

It is well known that CTR of an optocoupler varies with temperature and there is a CTR variation among different units of the same optocoupler. An NTC circuit can be designed to help reduce the effect of variation of CTR. The entire circuit design of the NTC circuit is provided in Section 5.3.5.

It is important to note that the IC has internal compensation for the loop stability.

3.6.2.2 Output Current Regulation - Non-isolated Output

The application is similar to the isolated example (Section 3.6.2.1) except there is no optocoupler. The LED current is passed through a series sense resistor and the voltage across that resistor is proportional to the LED current. This sense resistor needs to be very small to limit the power dissipation in the resistor. The sensed voltage is then amplified to be 2.5V at the full load current. To reduce the number of components the amplifier can be eliminated. In this case, a higher valued sense resister should be used to get the sense voltage equal to 2.5V at full load. It is to be noted that this will reduce the over all efficiency of the LED driver.

To have over voltage protection, the output voltage also can be sensed and diode or'ed to the output of the current sensing circuit. Initially voltage loop takes over because the LED load needs a minimum voltage to turn on. The voltage from the current sensing side is designed to be higher than the voltage from voltage sensing diode during normal operation. Also the voltage sensing helps to limit the output voltage, if one of the LEDs becomes open for any reason. The proportional and integral compensation within the IC make the system stable.

3.6.2.3 Output Voltage Regulation - Isolated Output

The output voltage is sensed through a divider resistor and a TL431 type of device can be used to amplify the error voltage from a reference voltage. An optocoupler can be used to pass the error information to the feedback pin FB on the primary side for isolating the output. In addition, the primary current is sensed and the average current is adjusted to be sinusoidal (in phase with AC input Voltage). The amplitude of the primary current is adjusted to make the secondary voltage constant at the desired level. Because this is a single stage PFC there will be second harmonic ripple at the output. Output capacitors are added to reduce the output second harmonic ripple and also the high frequency switching ripple. The proportional and integral compensation within the IC make the system stable. The over voltage protection at the output can be achieved by clamping the output of TL431.

It is well known that Current Transfer Ratio (CTR) of an optocoupler varies with temperature and there is also a CTR variation among different units of the same optocoupler. An NTC circuit can be designed to help reduce the effect of variation of CTR.

It is important to note that the IC has internal compensation for the loop stability. There is no need for external compensation.

3.6.2.4 Output Voltage Regulation - Non-isolated Output

When non-isolated, an opto-isolator is not necessary. The output voltage is sensed through the output divider and the output of the divider is connected directly to the feedback pin FB. The IC then controls the output voltage in the same way as for the isolated case. It is important to note that the IC has internal compensation for the loop stability.

3.7 ISNS – Current Sensing / Over Current Protection

3.7.1 ISNS – Peak Current Sensing

The 88EM8080/88EM8081 LED driver provides power factor correction (PFC) in addition to providing regulation. Regarding the PFC function, the average input current is varied to be proportional to the input voltage. This way the average input current will be sinusoidal. This input current is the same as the primary MOSFET current in a flyback circuit. Therefore, the IC can sense the MOSFET current and then use average current mode control to implement the PFC function. The voltage across the resistor in series with MOSFET (connected between MOSFET source pin and bridge diode negative DC terminal) is used as primary current sensing signal. The primary MOSFET source pin is grounded to apply a PWM signal between the gate and the source. The current sense signal in series MOSFET source therefore becomes negative with respect to ground. The IC uses this negative signal for input current control to provide the PFC function.

3.7.2 ISNS – Average Current Mode Control

The voltage across the primary current sense resistor is proportional to the peak value of switching current. An RC filter can be used to provide the average current. The output of the RC filter is then applied to ISNS pin. The internal current loop adjusts the duty cycle so that average current is sinusoidal. The amplitude of the sinusoidal current is adjusted by the external voltage/current loop to achieve constant output load voltage/current.

3.7.3 ISNS – Adaptive Over Current Protection

The average current signal at the output of the RC filter is also used for over current protection. The IC has an internal current comparator with four different internal thresholds for current protection on ISNS pin as the input voltage signal varies. The input current varies inversely with the AC input voltage. There are four different OCP thresholds at four different input voltage ranges. The different thresholds; V_{IOVER_TH1}, V_{IOVER_TH2}, V_{IOVER_TH3} and V_{IOVER_TH4} are detailed in Table 4, Electrical Characteristics, on page 16. With these four adaptive over current protection steps the IC provides almost constant power protection over the entire AC input voltage range.

3.7.4 OCP – Cycle by Cycle Over Current Protection

The voltage across the primary current sense resistor is proportional to the peak value of switching current. This voltage can be used for cycle by cycle over current protection by the OCP pin. When the OCP pin is pulled low the IC will shut down and there is no switched output signal at SW pin.

3.8 Mixed Modes of Operation

The 88EM8080/88EM8081 controller operates in Continuous Conduction Mode (CCM) or Discontinuous Mode (DCM) modes of operation. The transformer primary inductance and the load determine the modes of operation. The CCM mode will have lower peak current than the discontinuous mode of operation. At high power levels CCM is recommended because of reduction of copper losses in the transformer and also the conduction losses in the primary MOSFET. In addition CCM could reduce the input filter size. DCM mode may be recommended at lower power levels to reduce the turn-on switching losses and the Primary FET losses due to reverse recovery time and charge of the output diode.

3.9 Compensation and Adaptive Control Loop

The LED current control is a feedback control system. The bandwidth of the voltage loop for the single stage LED feedback control system has to be much less than twice the line frequency to provide a high power factor and low THD. The entire feedback system needs to be designed for high power factor and low THD at low line (90-132VAC) and high line (180-264VAC). Marvell has an internal proportional and integral gain control feature for the voltage loop due to Marvell's DSP Control Technology. This means by sensing the input voltage, the IC sets PI control automatically to change the bandwidth for different AC input line ranges. This innovative adaptive feature will help achieve low THD and high power factor at all lines and loads. Because of this proportional and integral control within the IC, no external compensation is required for non-isolated outputs. Minimal external compensation is required for isolated outputs mainly for the compensation on the error amplifier (TL431) at the secondary side. This compensation network provides enough attenuation at 120Hz so that the second harmonic ripple voltage from the sensed current signal is attenuated and not amplified.

3.10 Over Temperature Protection

The 88EM8080/88EM8081 IC has an internal over temperature sensing circuit. On over temperature, the fault detection signal shuts off the PWM switching output at the SW pin.

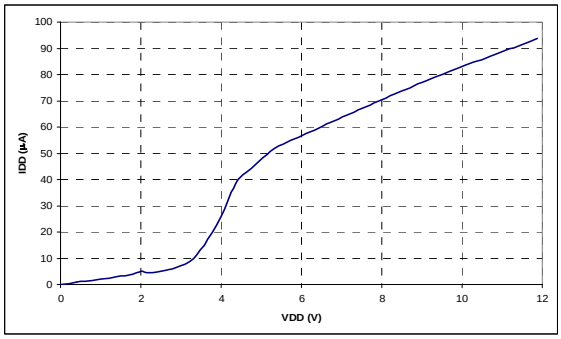
4 Functional Characteristics

The following applies unless otherwise noted: V_{IN} = 60Hz half-wave sinusoidal from 0V to the peak voltage (V_{PK}) given in the test conditions of each graph. T_A = 25°C.

All measurement readings are typical.

4.1 V_{DD} Characteristics

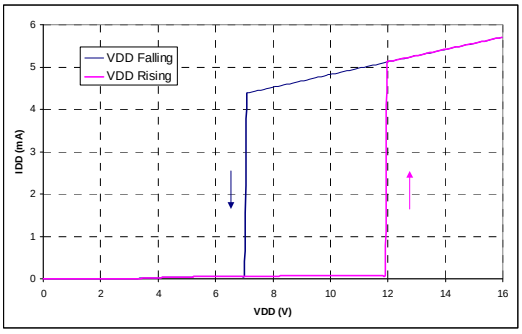
Figure 4: I_{DD} Quiescent (I_{DD_QST}) vs. V_{DD}



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- V_{FB} = 0V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

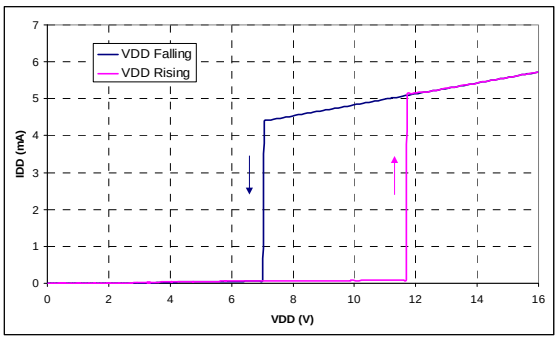
Figure 5a: I_{DD} vs. V_{DD} (V_{DD_ON})



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 0V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

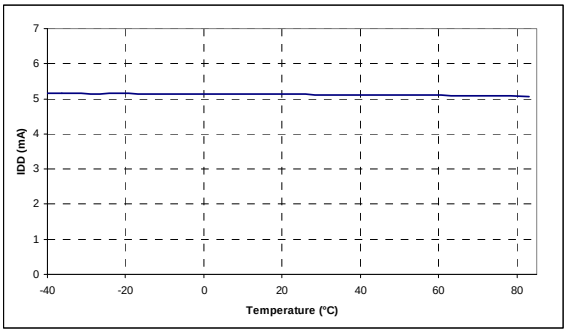
Figure 5b: I_{DD} vs. V_{DD} (V_{DD_ON})



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 2.4V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

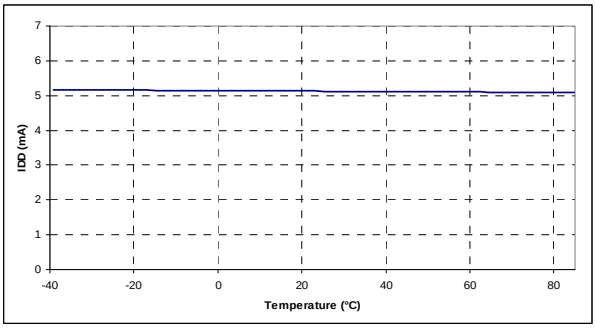
Figure 6a: I_{DD} Operation (I_{DD_OP}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 0V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

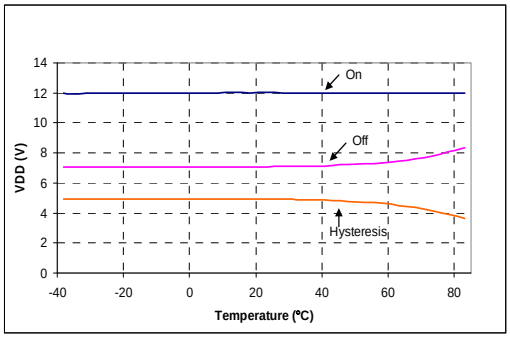
Figure 6b: I_{DD} Operation (I_{DD_OP}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 2.4V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

Figure 7: V_{DD} On/Off vs. Temperature

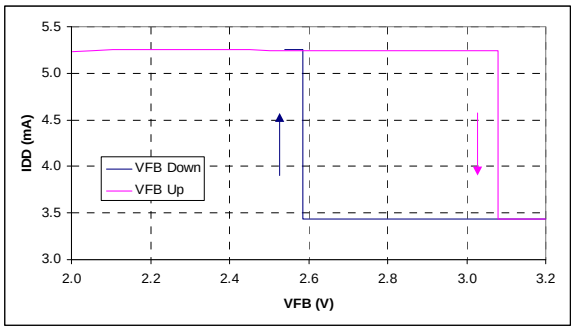


Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- F_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

4.2 V_{FB} Characteristics for Over Voltage Protection

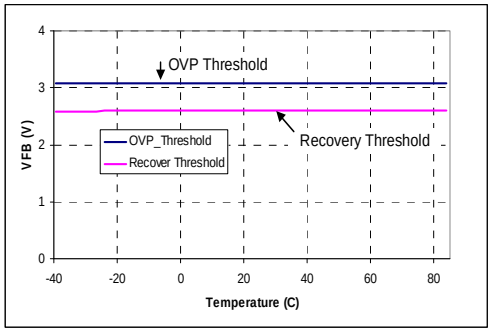
Figure 8: I_{DD} vs. V_{FB}



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

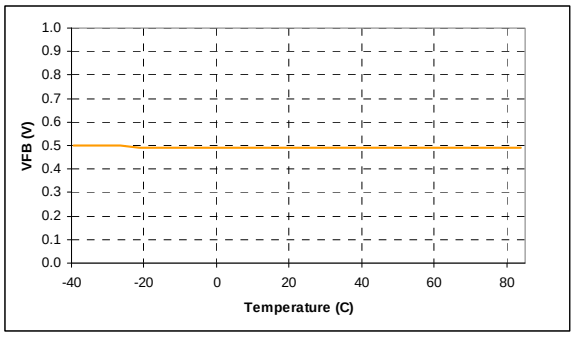
Figure 9: V_{FB_OVP} vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

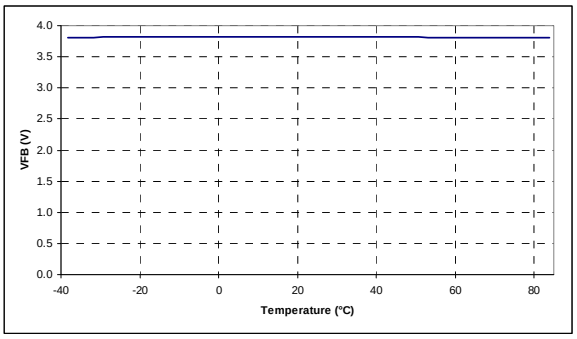
Figure 10: V_{FB_OVP} Hysteresis vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

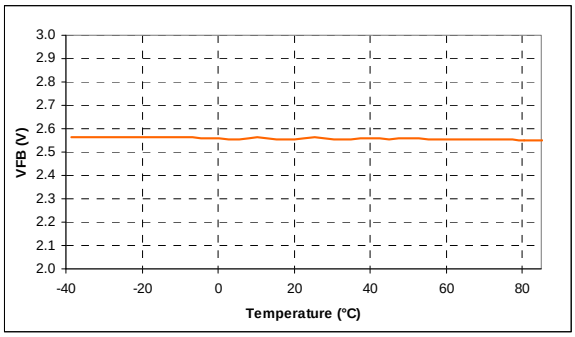
Figure 11: $V_{FB\_OVP\_LATCH}$ vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

Figure 12: Normal Regulation Reference (V_{FB_REG}) vs. Temperature

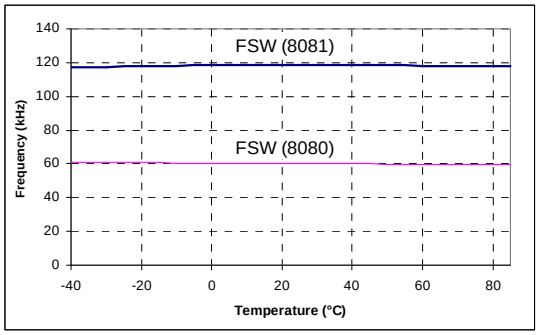


Test Conditions:

- V_{DD} = 12V
- V_{IN} = 2V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

4.3 Switching Frequency Characteristics

Figure 13: Switching Frequency vs. Temperature

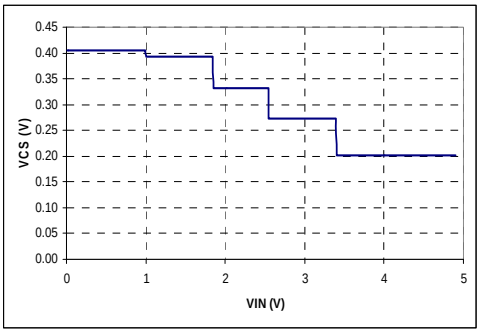


Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

4.4 Over Current Threshold Characteristics

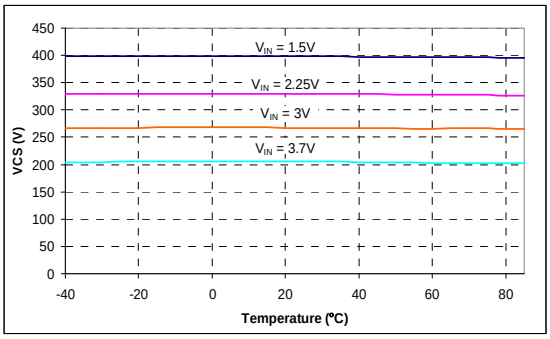
Figure 14: Over Current (V_{IOVER}) vs. Input Voltage V_{IN} Peak Value)



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 118kHz
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

Figure 15: Over Current (V_{IOVER}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 118kHz
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

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5 Design and Applications Information

5.1 Overview

The 88EM8080/88EM8081 is a PWM controller for LED applications with PFC. Flyback topology is used to simplify the two stage (front-end PFC and output stages) design to a single stage that includes Power Factor Correction (PFC) and regulation of the output. Compared to the two stage structure, a single stage with PFC is a more cost effective solution for LED lighting applications. The following sections provide guidelines for the application design, component selection, and board layout in order to improve LED application performance with PFC based on the flyback topology.

The 88EM8080/88EM8081 IC control algorithm uses Average Current Mode Control for power factor correction applications with low harmonic distortion and good noise immunity. The IC senses the output current and forces it to follow the reference LED current matching the design requirements. The chip also senses the primary current and forces the average signal of the primary current to follow the sinusoidal current reference, therefore achieving power factor correction. This is possible because the bandwidth of the outer current/voltage loop is much smaller than twice the line frequency. This IC implements the adaptive loop control so that the LED power supply achieves high power factor even under high input voltage and low load conditions. The device also provides strong gate drive capability of 1.2A (typical).

There are four analog input signals and one logic output signal for the 88EM8080/88EM8081 controller.

1. Input voltage signal at VIN pin is a half sinusoidal waveform. It is fed into the VIN pin through the input voltage resistor divider. This is for the line frequency zero-cross detection for PFC. Using the zero-crossing detector, the IC can predict the input sinusoidal waveform. The design of the input voltage divider and the design equations for the prediction of input sinusoidal voltage are described in the following Section 5.2.The signal at the VIN pin also provides brown-out protection because of the minimum VIN voltage requirement. This brown-out protection is described in Section 5.2.1.
2. Input signal at FB pin is the output feedback signal through the output voltage resistor divider plus the compensation. For LED current control, LED current is sensed and fed back to FB pin. An optocoupler can be used for isolation, if necessary. This signal helps to obtain output voltage regulation.
3. Input current sensing signal is derived from the sensing resistor to the ISNS pin. This is for the average current mode control to achieve a good sinusoidal current waveform and high power factor. This average current signal is also used for over current protection.
4. Input over current protection (OCP) signal is a logic signal instead of an analog signal. It is used to shut down the output at the SW pin when pulled low for cycle by cycle current limiting.

The output signal from the 88EM8080/88EM8081 is the PWM gate drive signal from the SW pin. The switching frequency on the 88EM8080 device is fixed to 60kHz while the 88EM8081 is fixed to 120kHz. *Refer to the 88EM8080/88EM8081 Application Note located on Marvell.com for more application details.*

The advantages of this device operating under Mixed Mode Control when compared to Critical Transition Mode are shown in Table 6.

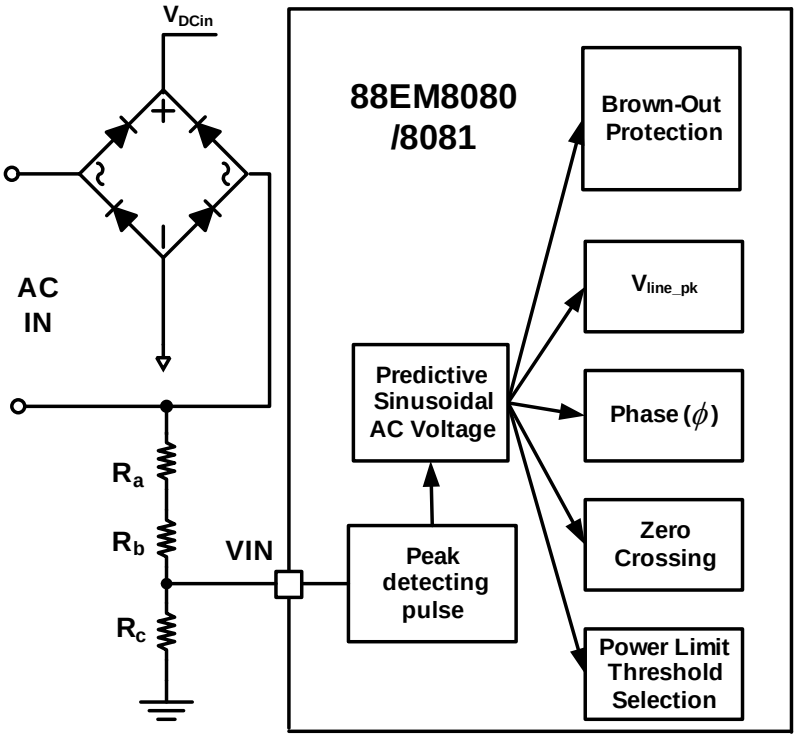
Table 6: Comparison between Critical Transition Mode and Mixed Mode Controls

Critical Transition Mode Control	Mixed Mode – CCM/DCM Control
High peak current on switch	Low peak current on switch
High diode peak current at secondary side	Low diode peak current at secondary side
Variable switching frequency with lowest switching frequency at peak input voltage	Fixed switching frequency
Big transformer	Small transformer
Difficult to achieve high power	Easy to achieve high power
High cost	Low cost

5.2 Input Voltage Resistor Divider on VIN Pin

Accurate peak detection signal and zero-cross detection for regenerating the input sinusoidal voltage is the most important issue for a proper current shaping and total harmonic distortion (THD) improvement. A peak detecting pulse is generated after comparing the VIN sinusoidal signal to an internal threshold reference of 0.72V (typical) as shown in Figure 17. If the threshold reference is too high, near the peak area, the calculation may lose accuracy because of the low slope. On the other hand, if the threshold reference is too low, there could be an error on zero-cross detection due to the possible distortions near the zero-crossing. For a universal input voltage range (85Vac~270Vac) the optimum accuracy would be achieved if the threshold level is around 30° of the line cycle.

Figure 16: Internal Block for Zero-cross Detection, Brown-out Protection



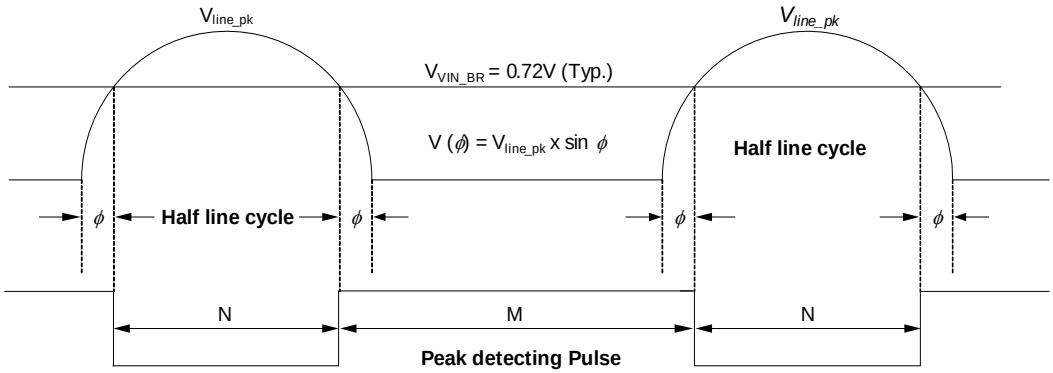
The values for the sensing resistors R_a, R_b, and R_c in Figure 16 are selected to get proper sinusoidal AC voltage, under voltage lockout, and peak voltage detection. If the values are too small there will be higher power loss and if they are too big there might be pickup noise on the VIN signal. The recommended values are shown in the following equation:

$$\frac{R_a + R_b}{R_c} = \frac{100}{1} = \frac{1.8M\Omega}{18k\Omega}$$ Equation (1)

Where $R_a + R_b$ is recommended to be 1.8MΩ and R_c is selected as 18kΩ. Knowing ($R_a + R_b$), R_a and R_b can be designed.

For this input voltage resistor divider, the appropriate combination based on the voltage / power rating of the resistors should also be considered.

Figure 17: Peak Detecting Signal for Predictive Sinusoidal AC Voltage



As can be seen in Figure 16, the internal peak detecting circuit generates peak detecting pulse through the inside comparator which has a threshold voltage of 0.72V and external AC sensing resistors of R_a, R_b and R_c. This pulse is processed in the DSP core to calculate the mid-point (peak point) and the zero-crossing point of the sinusoidal waveform. The phase angle of ϕ is calculated using the widths (M and N) of the high and low signals.

$$N = (\pi - 2\phi)$$ Equation (2)

$$M = (\pi + 2\phi)$$ Equation (3)

$$\phi = (M - N)/4$$ Equation (4)

Peak value of the sinusoidal waveform is calculated by the following equation:

$$V_{line\_pk} = V(\phi)/(\sin\phi)$$ Equation (5)

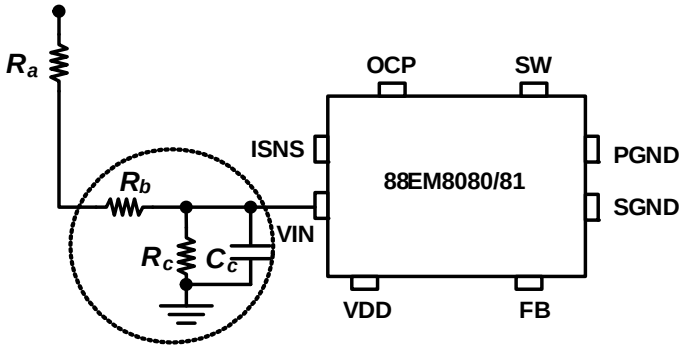
5.2.1 Brown-out Protection

The signal that appears on the VIN pin is a half sinusoidal voltage waveform and its peak value has to be higher than 0.72V for normal operation. Whenever the VIN voltage is less than 0.72V at the peak value, it is considered as a Brown-out condition. During the brown-out condition, the IC generates a low duty cycle of 6% to protect the system. For the design shown in equation (1) the brown-out protection occurs at the AC input of 50V RMS (72V peak, VIN=0.72V). To adjust the brown-out protection point, the resistance value of R_a, R_b and R_c can be changed.

5.2.2 Layout Guidelines

It is recommended that a 0.1nF–10nF capacitor (C_C) is connected between VIN and ground for noise immunity. The layout of R_b, R_c and C_C should be kept as close as possible to the VIN pin, as shown in Figure 18 to reduce noise pickup. R_a should be kept as close as possible to the high voltage input.

Figure 18: Input Voltage Resistor Divider Layout Guidelines



Keep layout of Rb, Rc and Cc as close as possible to VIN pin to keep high noise immunization

5.3 Output LED Current Control

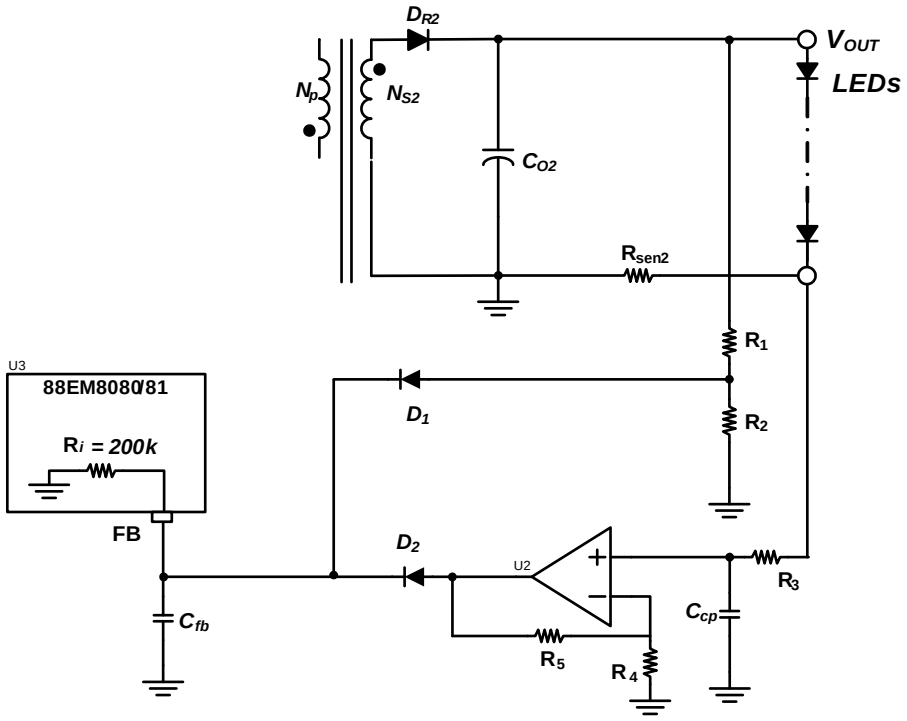
The brightness and color of a LED are functions of LED current. A constant current source driver for LED current therefore helps in control of brightness and color. The LED current is passed through a current sense resistor and the voltage across the sense resistor is used as a feedback signal for LED current control. Reference designs are presented in the following sections for isolated and non-isolated outputs for the control of LED current using Marvell 88EM8080/88EM8081 IC.

5.3.1 Non-isolated Output LED Current Control

Figure 19 shows a typical configuration for non-isolated output LED current control. LED current is sensed by the resistor R_{sen2}. The voltage across R_{sen2} is amplified by an amplifier U2. The output of the operational amplifier is connected to FB pin through a diode D_2. A voltage loop is also added for voltage regulation at no load. The two feedback loops (output voltage and output current) are implemented in an OR structure through D_1 and D_2.

During startup, the output voltage increases and must reach certain level before the LED current can flow. The output voltage is fed back through the resistor divider (R_1 and R_2) and the diode D_1. R_1 and R_2 are designed to limit the output voltage during startup (with no LED current) and when the LED string is open.

Figure 19: Non-Isolated Feedback Loop Schematic



5.3.1.1 R_1 and R_2 Resistor Divider Design

The following equation can be used for the design of R_1 and R_2.

$$\frac{\frac{V_{OUT\_MAX}}{R_1} - V_{D1}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{200}} = V_{REF} \qquad \text{Equation (6)}$$

Where V_{OUT_MAX} is the output over voltage regulation point during starting or under a no load condition, R_1 and R_2 are in kΩ, V_{D1} is the voltage drop of the diode D_1 and V_{REF} is the reference voltage inside the 88EM8080/88EM8081 IC. The nominal value of V_{REF} is 2.5V.

This equation takes into account of the internal leakage at FB pin. The leakage at the FB pin is equivalent to a 200k Resistor. Because the forward current of diode D_1 is less (less than 25mA) the voltage drop V_{D1} is about 0.1V to 0.3V depending on the diode and the temperature of the diode. It should be noted that under steady state conditions the current loop should be active and not the voltage loop. Therefore care must be taken in selection of R_2 to make sure that the voltage at the cathode of D_1 is less than the voltage at the cathode of D_2 under steady state conditions.

5.3.1.2 RC Filter Design

In single stage PFC LED applications, the output has twice the line frequency ripple which may trigger the OVP function through the voltage at the FB pin. An RC filter defined by R_3 and C_{cp}, is designed to filter the twice the line frequency ripple embedded in the feedback signal. The cutoff frequency of the RC filter should be much lower than twice the line frequency. The following equation (7) is used for the design of R_3 and C_{CP}.

$$\frac{1}{2\pi R_3 C_{cp}} \ll 100Hz \qquad \text{Equation (7)}$$

In some situations the output current will be very low and the output capacitance could be selected to be a high value. In this case, twice the line frequency ripple at the output will be very low and this RC filter may not be necessary.

5.3.1.3 Design of Operational Amplifier Circuit

The DC Gain of the non-inverting amplifier circuit is based on the following equation:

$$K_{U2} = \left(1 + \frac{R_5}{R_4}\right) \qquad \text{Equation (8)}$$

However, the average current through the LED is controlled by the following equation:

$$I_{AVG} \times R_{sen2} \times (K_{U2}) - V_{D2} = V_{REF} \qquad \text{Equation (9)}$$

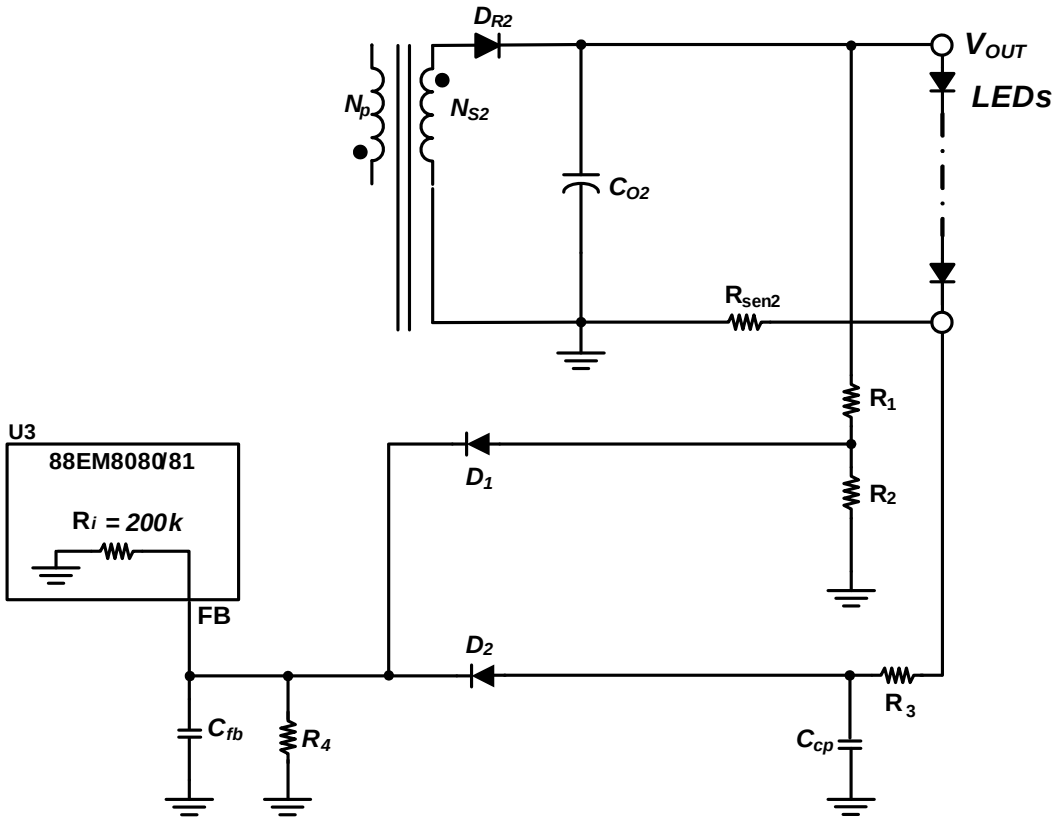
Where, I_{AVG} is the average LED current, V_{D2} is the voltage drop on the diode D_2 and K_{U2} is the DC gain of the operational amplifier circuit. From equation (9) the required K_{U2} can be determined.

R_5 and R_4 are designed from equation (8).

5.3.2 Low-Cost LED Current Control with Non-isolated Output

One can have a cost effective design by not having the operational amplifier in the output current feedback loop. The circuit is shown in Figure 20.

Figure 20: Low-cost, Non-isolated LED Current Control



In this case, the voltage across R_{sen2} is directly connected to VFB pin through the filter R_3 and C_{CP} and the diode D_2 but without the operational amplifier U2. Also it should be noted that R_{sen2} has to be selected so that the voltage across it is higher than 2.5V (by a diode drop) under steady state conditions. Because of this condition, R_{sen2} will be of a higher value than when the operational amplifier is present and there will be a significant power loss in the R_{sen2} resistor. The efficiency of this LED driver circuit will be lower than that of application circuit in Figure 19, Non-Isolated Feedback Loop Schematic, on page 35.

The following equation can be used for the design of R_3 in addition to equation 7.

$$(I_{AVG} \times R_{sen2}) - V_{D2} = V_{REF}\left(1 + \frac{R_3}{R_4} + \frac{R_3}{200}\right) \quad \text{Equation (10)}$$

Where, I_{AVG} is the average LED current, V_{D2} is the voltage drop on the diode D_2, V_{REF} is the internal reference of the 88EM8080/88EM8081 IC, and resistors R_3 and R_4 are in kΩ.

The following equation can be used for the design of R_1 and R_2.

$$V_{OUT\_MAX} = V_{REF}\left(1 + \frac{R_1}{200} + \frac{R_1}{R_2} + \frac{R_1}{R_4}\right) + V_{D1}\left(1 + \frac{R_1}{R_2}\right) \quad \text{Equation (11)}$$

Where, V_{OUT_MAX} is the maximum output voltage, VD1 is the voltage drop on the diode D1, and resistors R_1, R_2 and R_4 are in kΩ.

A reference design for a cost effective non-isolated LED driver is presented in Section 5.7.

5.3.3 LED Current Control with Isolated Output

The typical isolated output current control is shown in Figure 21.

Figure 21: Isolated LED Current Control

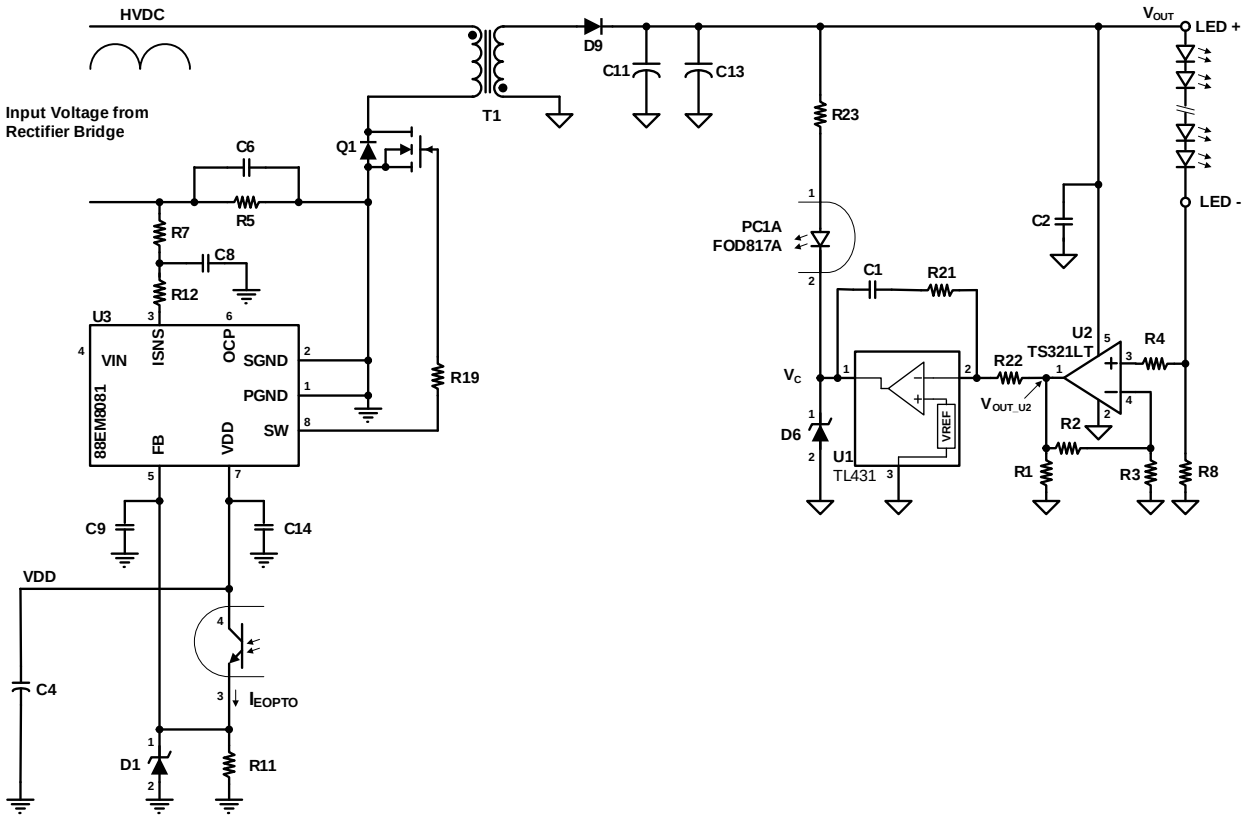


Figure 21 shows a typical configuration for LED current control when the output is isolated from the AC input. The current through the LED also passes through the resistor R8 and the voltage across R8 is used for output current sensing and for LED current control. In order to reduce the power dissipation in the current sensing resistor, R8 could be selected to be a low value such as 0.1Ω. The voltage across R8 at 500mA steady state current is 50mV.

This current sense voltage across R8 is amplified by the non-inverting amplifier U2 and is applied to the inverting input of the U1 circuit. Typically, the TL431 IC is used for U1. U2 is necessary to amplify the sense voltage to 2.5V at the steady state LED regulated current. This is because the non-inverting input of U1 has a reference voltage of 2.5V nominal. The U1 device is used to

generate an error voltage of V_C at the output after comparing the output voltage of U2 to the internal reference voltage of U1.

An optocoupler is connected between the output (LED+) and the U1 error voltage output through a resistor R23. The current through the optocoupler is a function of error voltage at the output of TL431and is varied until the output voltage of U2 is equal to U1 reference voltage of 2.5V.

The current through the opto-transistor and resistor R11 is proportional to the opto-diode current by a factor of current transfer ratio of the optocoupler. The voltage across R11 is applied as input to FB pin. Therefore, the voltage at the FB pin is a function of the error voltage output of U1.The voltage at the FB pin controls the duty cycle of the drive signal to the external MOSFET Q1. The switching current of Q1 is sensed by the voltage across resistor R5. At steady state conditions the FB pin voltage will be 2.5V which is equal to the nominal value of internal reference for 88EM8080/88EM8081 IC.

The voltage across R5 is filtered and the filtered voltage is proportional to the average current. The duty cycle is varied so that the average of the input current through the ISNS pin follows the AC Input voltage. The amplitude of the AC sinusoidal input current is varied to adjust the output voltage, therefore adjusting the LED current until the output voltage of U2 equals the reference voltage of U1 (2.5V, typical).

During startup, the FB pin voltage is zero and the duty cycle at the SW pin is 6% (typical). Soft start is provided until feedback voltage reaches 2.1V which is 87.5% of the reference voltage of U3 (2.5V, typical). During the time the voltage at FB pin rises to 2.1V, the internal current reference increases linearly. The internal current reference determines how fast the power is delivered to the secondary side in addition to other circuit parameters. Therefore the soft start time is the duration for internal current reference to raise linearly. When the FB pin reaches 2.1V, the internal feedback loop starts closed loop operation to eventually reach steady state. It is to be noted that LEDs will not conduct until the voltage across them reaches a minimal value. This means the LED load is open circuited during startup. The voltage across the output capacitors C11 and C13 is zero initially at starting. The output capacitors C11 and C13 will get charged rather quickly and the output voltage could overshoot the steady state value. During starting condition when LEDs are not conducting or if the LED string is open circuited, the output voltage across the LED string may go higher than the normal steady state value and the zener D6 will be conducting. The output voltage of U1 is equal to the zener voltage. Once the LEDs starts conducting the output voltage of U1 starts decreasing and will come to a steady state value at which point the voltage across D6 will be much lower than the zener conduction voltage.

If the ambient temperature is increased, the CTR of the optocoupler will become less, then more current through the optodiode becomes necessary for LED current regulation. This means the output voltage of TL431 will be lower than the steady state voltage at the lower ambient. If the ambient is decreased, TL431 voltage will be higher than the steady state voltage at the higher ambient. The design of the TL431 should be such that the zener diode D6 should not conduct during normal operation at any temperature. In addition the output voltage of TL431 cannot go below 2.5V for any reason during steady state operation.

5.3.4 Isolated LED Current Control - Circuit Design

The relation between output current signal and the reference voltage of U1 is provided by the following equation:

$$V_{REFU1} = \frac{R_2 + R_3}{R_3} \times I_{LEDavg} \times R_8$$ Equation (12)

Where V_{REFU1} is the TL431 reference voltage and is equal to 2.5V nominal, I_{LEDavg} is the average current through the LED.

R_8 is selected to be a low value so that the power dissipation is minimum. For the reference design it is 0.1Ω.

One can select R_2 and R_3 from the above equation after selecting R_8 since V_{REFU1} is equal to 2.5V.

C11 and C13 are selected so that the second harmonic ripple at the output is reasonable.

The Zener diode D_1 is selected to be 4.7V so that the voltage at the FB pin cannot exceed the rated maximum voltage for the FB pin.

The output voltage of U1 error amplifier (V_C), and the secondary side optocoupler diode current are related by the following equation:

$$I_{sf} = \frac{V_O - V_{FD} - V_C}{R_{23}}$$ Equation (13)

Where V_{FD} is the forward voltage drop of opto-coupler diode and is about 1V.

V_C is also related to the FB pin voltage or the reference voltage of U3 by the following equation:

$$\frac{V_O - V_{FD} - V_C}{R_{23}} \times CTR \times R_{11} = V_{FB\_REG}$$ Equation (14)

Where V_{FB_REG} is the reference voltage of U3 and CTR is the current transfer ratio of optocoupler.

At steady state no load condition, the secondary side error amplifier enters into positive saturation status because of no current feedback signal. Therefore, the output voltage V_C increases to the maximum clamp voltage V_{ZD6} as pointed out in the previous section. V_{ZD6} should be higher than normal operation voltage of V_C to keep enough margin. Then the no load output voltage will increase until the FB pin voltage reaches 2.5V. The following equation can be used to calculate the no load output voltage.

$$\frac{V_{O\_NOLOAD} - V_{FD} - V_{ZD6}}{R_{23}} \times CTR \times R_{11} = V_{FB\_REG}$$ Equation (15)

V_{O_NOLOAD} is also equal to the maximum voltage when the LED string is broken or when the sense line is open.

The following equation is provided to calculate the output over voltage protection point.

$$\frac{V_{O\_OVP} - V_{FD} - V_{ZD6}}{R_{23}} \times CTR \times R_{11} = V_{FB\_OVP}$$ Equation (16)

At OVP condition the error amplifier output voltage increases to V_{ZD6}. It is pointed out that the primary FB pin voltage reaches the OVP threshold V_{FB_OVP} (which is about 3V) when the output voltage increases to OVP level. This OVP condition can occur with a low output capacitance and high output ripple.

The steady state output at no load can also be calculated using the following equation which depends on the normal operation voltage V_C of the TL431 error amplifier at nominal full load condition and V_{ZD6}.

$$V_{O\_NOLOAD} = (V_O + V_{ZD6} - V_C) \quad \text{Equation (17)}$$

It is important to note that V_C varies with temperature and will also vary from unit to unit of the optocoupler.

The transfer function of TL431 amplifier circuit is:

$$H(S) = \frac{V_C(S)}{V_{OUT\_U2}(S)} = \frac{1 + s \times C_1 \times R_{21}}{s \times R_{22} \times C_1} \quad \text{Equation (18)}$$

Where V_{OUT_U2} is the output voltage of the amplifier U2 as shown in Figure 21. The values of C_1, R_{21} and R_{22} are selected in such a manner that there is enough DC gain for the average current feedback signal. At the same time there should be enough attenuation at 120Hz so that the second harmonic ripple voltage from the sensed current signal is attenuated and not amplified. Therefore the low frequency zero should be placed far below twice the line frequency (<20Hz).

5.3.5 NTC Compensation Circuit Design

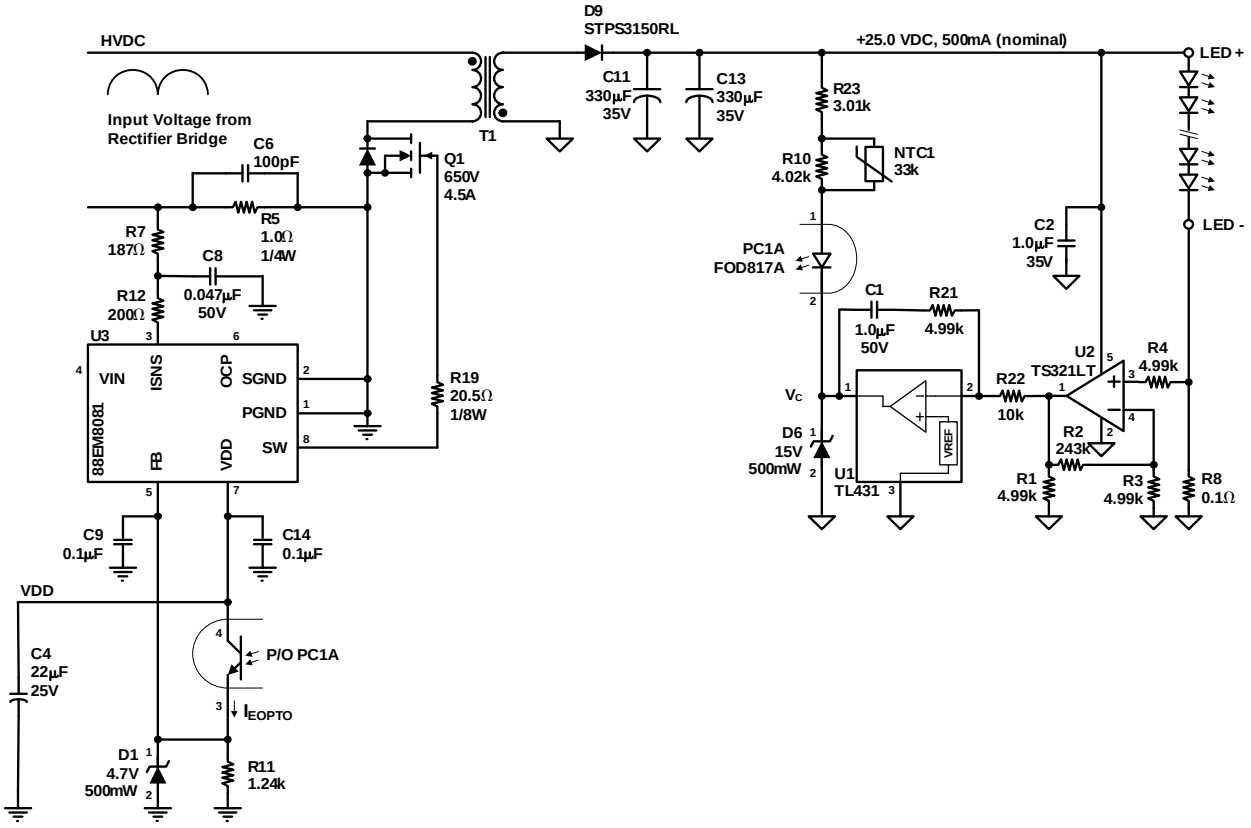
The secondary side error amplifier output voltage V_C varies between the maximum value V_{ZD6} and the minimum value 2.5V (U1 (TL431) minimum supply voltage). From equation (13) it can been seen that the variation of V_C depends on the tolerance of R_{11} and R_{23} value, V_{FB} reference voltage and CTR value of optocoupler.

But the CTR value of optocoupler has a wide variation from unit to unit and also with temperature. For example, the relative CTR of FOD817 form Fairchild changes from 105% to 55% with ambient temperature from 0ºC to 110ºC. If ambient temperature increases, the CTR of optocoupler decreases, which results in a lower value for V_C. When ambient temperature is over 110ºC, the V_C voltage could reach the minimum limit value of 2.5V. Then the power system will be out of regulation. It is pointed out that 0ºC and 110ºC are selected for illustration only.

At 0ºC V_C would increase from the value at room temperature. If it is high enough zener D_6 would conduct and the power system is out of regulation.

In order to keep V_C at a reasonable range (below zener D_6 Voltage and above 2.5V with a margin) a NTC compensation circuit, shown in Figure 22, is introduced. An actual reference design is shown for illustration of NTC compensation. This compensation circuit is composed of a NTC resistor NTC1, resistor R10 and R23 instead of resistor R23 only.

Figure 22: Isolated LED Current Control with NTC Compensation



5.3.5.1 Design Equations

With NTC compensation circuit, the total equivalent resistance decreases when ambient temperature increases and will compensate for the variation of the CTR with temperature and maintain V_C at a narrow range. Similar effect takes place when the ambient temperature is decreased.

The following two equations at 25ºC and 110ºC ambient temperature condition are used for selection of resistors R10 and R23 values.

$$\frac{V_O - V_{FD} - V_{C\_25}}{R_{23} + \frac{R_{NTC1\_25} \times R_{10}}{R_{NTC1\_25} + R_{10}}} \times CTR\_25 \times R_{11} = V_{FB\_REF} \quad \text{Equation (19)}$$

$$\frac{V_O - V_{FD} - V_{C\_110}}{R_{23} + \frac{R_{NTC1\_110} \times R_{10}}{R_{NTC1\_110} + R_{10}}} \times CTR110 \times R_{11} = V_{FB\_REF} \quad \text{Equation (20)}$$

Where, R_{NTC1_25} and R_{NTC1_110} are the resistance value of NTC1 at 25ºC and 110ºC ambient temperature. CTR_25 and CTR_110 are the CTR values of optocoupler at 25ºC and 110ºC ambient temperature and V_{C_25} and V_{C_110} are the actual output voltages of U1 amplifier at 25ºC and 110ºC ambient temperatures.

In the following, V_C is assumed to be constant at 25ºC and 100ºC for the selection of resistors R10 and R23. Once the resistors are selected, the variation of V_C at 25ºC and 100ºC can be calculated.

$$V_{C\_25} = V_{C\_110} = V_C \quad \text{Equation (21)}$$

$$A = \frac{V_{FB\_REF}}{R_{11} \times (V_O - V_{FD} - V_C)} \quad \text{Equation (22)}$$

$$B = CTR\_110 - CTR\_110 \quad \text{Equation (23)}$$

$$C = R_{NTC1\_25} + R_{NTC1\_110} \quad \text{Equation (24)}$$

$$D = R_{NTC\_25} - R_{NTC\_110} \quad \text{Equation (25)}$$

$$E = B + A \times D \quad \text{Equation (26)}$$

$$F = 4 \times E \times B \times R_{NTC1\_25} \times R_{NTC1\_110} \quad \text{Equation (27)}$$

R10 can then be calculated from the following equation:

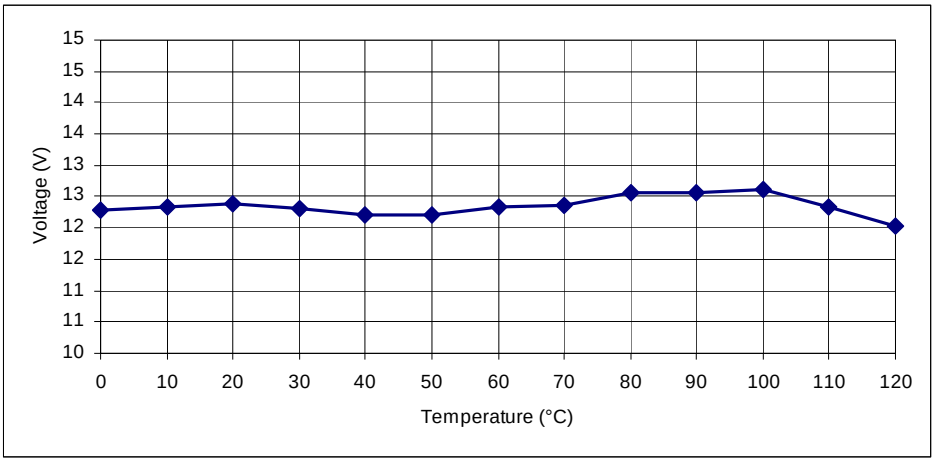
$$R_{10} = \frac{-BC + \sqrt{(BC)^2 - F}}{2E}$$ Equation (28)

R23 can then be calculated from the following equation:

$$R_{23} = \frac{CTR\_25}{A} - \frac{R_{10} \times R_{NTC1\_25}}{R_{10} + R_{NTC1\_25}}$$ Equation (29)

Marvell provides an Excel spread sheet tool for the required NTC compensation circuit selection to meet design requirements. The selection of a different value for NTC part, will provide diffent values for R10 and R23. The Excel spread sheet tool will help calculate variation of V_C with temperature. The designer can then select a suitable NTC value to minimize the variation of V_C. Figure 23 shows the variation of V_C with temperature for a 25V, 500mA output design with 33K NTC part. It is evident that the variation of V_C voltage is small when ambient temperature changes from 0ºC to 120ºC. This clearly shows that the NTC compensation circuit can be used effectively to compensate for the tolerance of the components and also for the wider variation of CTR of the optocoupler. A reference design for an isolated LED driver is presented in Section 5.8.

Figure 23: The Error Amplifier Output Voltage (V_C) vs. Temperature



5.3.5.2 Simplified Engineering Design Procedure

In the previous section, by assuming $V_{C\_25} = V_{C\_110}$, values for resistors R23 and R10 are estimated by solving the two simulataneous equations 18 and 19.

The simplified procedure can be used to get the estimates of R23 and R10. The steps are as follows.

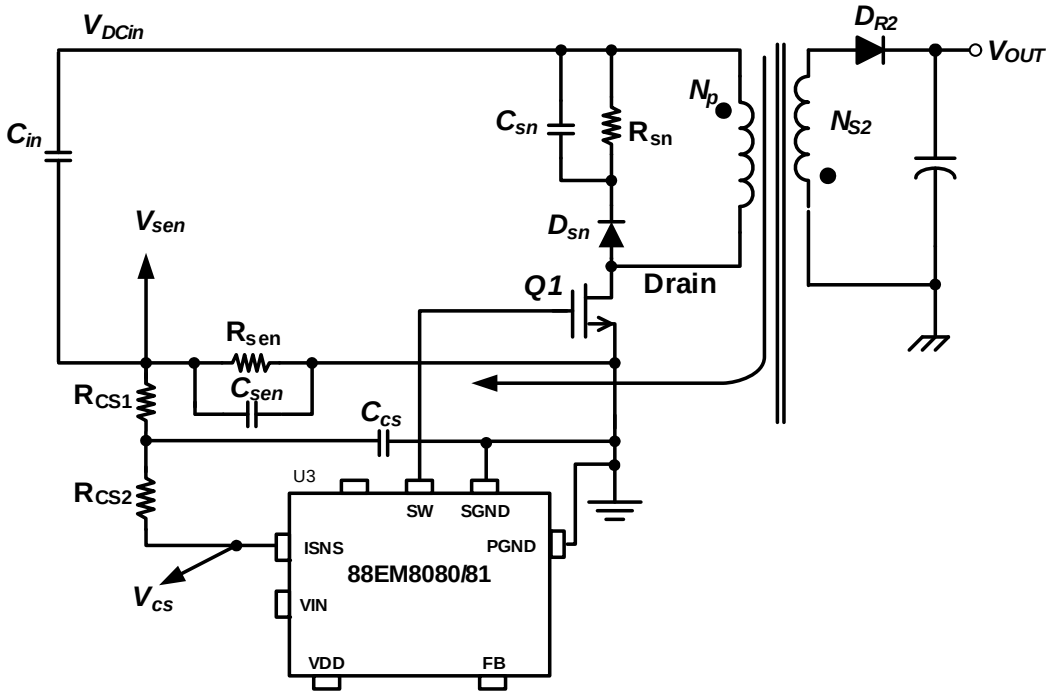
1. Knowing the zener value of D6, one can estimate V_{C_25}. For example, if D6 is a 15V zener, one can choose 11 Volts for V_{C_25}. This provides 4V nominal margin for the zener not to conduct.
2. Once V_{C_25} is known, equation 18 is solved to get the estimate for (R_C) = $R_{23} + \frac{R_{NTC1\_25} \times R_{10}}{R_{NTC1\_25} + R_{10}}$
3. Assuming $R_{23} = \frac{R_C}{2}$ and $R_{10} = \frac{R_C}{2}$ to get the value of R23 and R10.
4. An NTC can be selected such that, R_{NTC1_25} is about 5-10 times the value of R10 and R_{NTC1_25} is about 1/5 - 1/10 the value of R10.
5. V_{C_110} can then be calculated from equation 19.
6. V_{C_110} should be in the allowable range for the U2 (TL431) and no conduction for zener D6. For this example, the voltage range for V_{C_110} should be around 5V to 10V. This will satisfy the minimum requirement for V_C (not less than 2.5V) with a margin.
7. This process can be repeated until V_{C_110} is in the allowable range.

5.4 Current Sensing and Over Current Protection

5.4.1 Current Sensing Through ISNS Pin

The current sensing circuit is illustrated in Figure 24. The voltage drop on the current sense resistor should be kept very small in order to reduce the power consumption on the sense resistor. In flyback topology, the drain to source current flows through the transformer primary, MOSFET and current sense resistor (R_{sen}). The average current mode control single stage solution uses two signals: the peak current signal to avoid the transformer saturation including a short circuit condition, and the average current sense signal to achieve PFC operation. The voltage drop (V_{sen}) across resistor (R_{sen}) represents the flyback peak current signal. The voltage of (V_{CS}), after R_{CS} and C_{CS} low pass filter, represents the average current signal of the primary side of the flyback converter.

Figure 24: Current Sensing Circuit



The resistor (R_{sen}) should be designed as the example in Table 7 where R_{sen} is designed for a 60W power supply.

Table 7: Current Sensing Circuit

Input Power	P_{in}	60W
Minimum input voltage	V_{in_min}	85V
Maximum average input current	$I_{in\_max} = \sqrt{2} \times \frac{P_{in}}{V_{in\_min}}$	1A
Over current threshold Zone 1	V_{IOVER_TH1}	0.39V
Over current margin	I_{Margin}	30%
Current sensing resistor calculation	$R_{sns} = \frac{V_{IOVER\_TH1}}{i_{in\_max} \times (1 + I_{margin})}$	0.30Ω
Current sensing resistor selection	R_{sns}	0.30Ω

Table 8 shows the reference value of the current sensing resistor for different input power levels. In the practical design, the current sensing resistor value could be fine tuned around the value shown in the table based on the specification and the primary inductance of the flyback transformer.

Table 8: Current Sensing Resistor Selection Reference

Input Power (W)	10	30	60	120
Current Sensing Resistor (Ω)	1.0 - 2.0	0.50 - 0.70	0.25 - 0.35	0.12 - 0.15

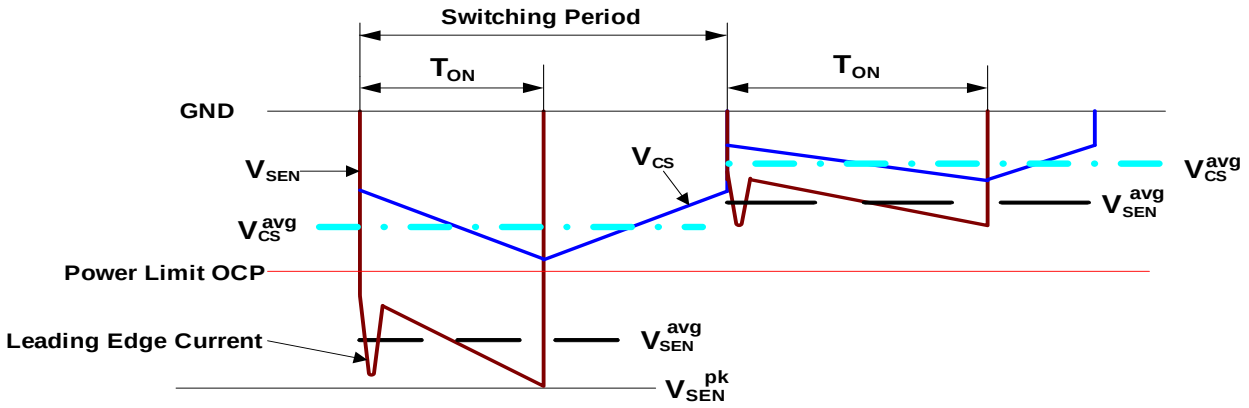
5.4.2 Average Current Signal and Over Power Limitation

The peak current is sensed as the voltage across the sense resistor. To convert flyback peak current into an average current signal, an RC filter is required as described in the previous section. Figure 25 shows how the addition of the filter will result in an average current signal. This average current signal, V_{cs} is fed back onto the ISNS pin and used to achieve a sinusoidal current waveform by an internal current control loop. It is also used to achieve power limitation. The corner frequency of the RC filter is recommended approximately 1/10~1/6 of the switching frequency. The recommended value for R_{cs1} is 187Ω, R_{cs2} is 200Ω. R_{cs1} and R_{cs2} are used for the purpose of blocking excessive negative and surge voltages. A single stage PFC operates at 120kHz (typical) using the 88EM8081 device. C_{cs} is designed as 47nF which results in a corner frequency of 18Hz. The corner frequency of the low pass filter is defined by the following equation;

$$f_{corner} = \frac{1}{2\pi R_{cs1} C_{cs}} \qquad \text{Equation (30)}$$

U3 is designed to perform over power limitation according to different over current thresholds as shown in Table 4, Electrical Characteristics, on page 16. The adaptive over current and hence adaptive over power protection feature is described in Section 3.7.3

Figure 25: Current Sensing and Over Current Protection Waveforms



5.4.3 Peak Current and Average Current Relationship

The relationship between the flyback peak and the average current signals is derived in this section. Figure 25 explains this in detail.

The peak to peak ripple current through the Rsen resistor is given by the following equation.

$$\Delta I_{ins} = \frac{V_{line} \times D}{L_m \times f_s}$$ Equation (31)

The average current sensing signal across Rsen during the MOSFET switching on time is...

$$V_{sen}{}^{avg} = V_{senpk} - \frac{\Delta I_{ins}}{2} \times R_{sen}$$ Equation (32)

The average current sensing signal during the whole switching cycle can be calculated as

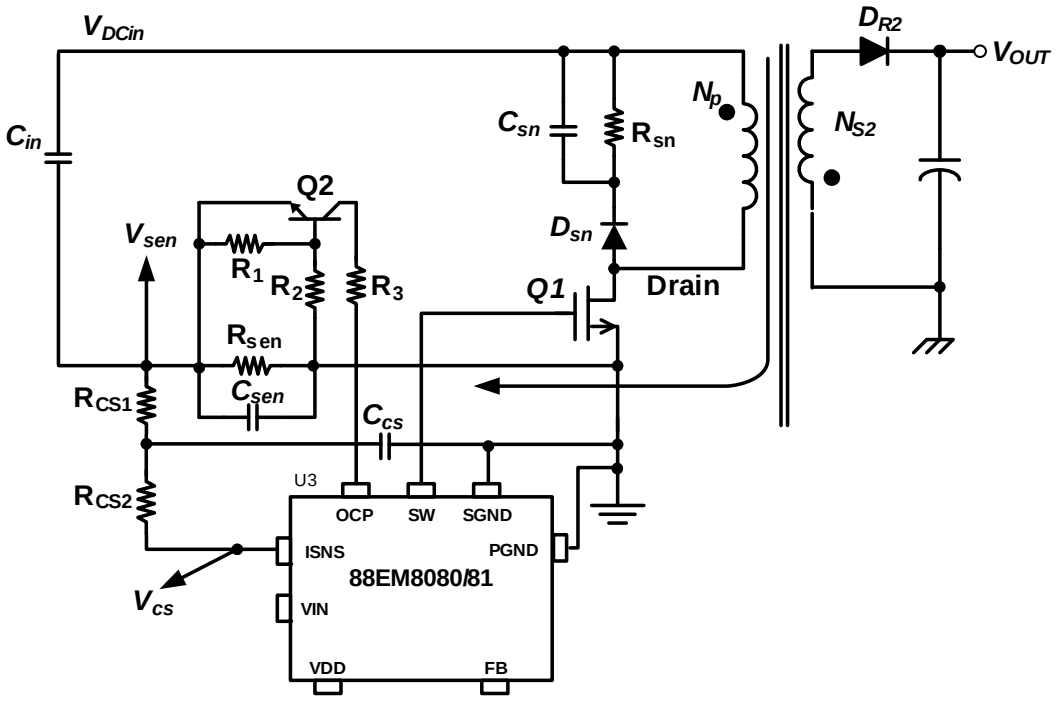
$$V_{cs}{}^{avg} = V_{sen}{}^{avg} \times D$$ Equation (33)

5.4.4 Cycle by Cycle Current Protection through OCP Pin

The voltage across Rsen and the OCP pin are used for cycle by cycle over current protection. This protection helps to avoid the transformer saturation. A circuit consisting of an NPN transistor Q2 with a low base to emitter parasitic capacitance is recommended for the design as shown in Figure 26. The sensing voltage through R_{sen} should trigger and turn on the transistor Q2 during the over current condition. Q2 then pulls the OCP pin to low and turns off the gate signal to the external MOSFET.

For the design of the protection circuit a -2mV/°C (typical) temperature coefficient of V_{be} should be considered. The lowest voltage (V_{be}) will be set at the junction temperature of 80°C.

Figure 26: Current Sensing and Cycle by Cycle Over Current Protection Circuit



At 80°C, the base to emitter volage can be calcuated from the following equation

$$V_{be} \cong 0.65V - 2mV \times (80 - 25) = \ 0.54V$$ Equation (34)

The highest V_{be} voltage occurs when the junction temperature is -25°C.

$$V_{be} \cong 0.65V - 2mV \times (-25 - 25) = \ 0.75V$$ Equation (35)

The voltage V_{be} should have tolerance margin to select the resistor, R_{sen}. R_{sen} can be selected from the following equation.

$$R_{sen} \leq \frac{0.50V}{I_{ds}^{peak}}$$ Equation (36)

The minimum saturation current point of I_{lim} for the transformer should satisfy:

$$I_{lim} = \frac{0.75V}{R_{sen}} \times \frac{(R_1 + R_2)}{R_1}$$ Equation (37)

I_{lim} should have enough margins considering transformer saturation condition at lower ambient temperature.

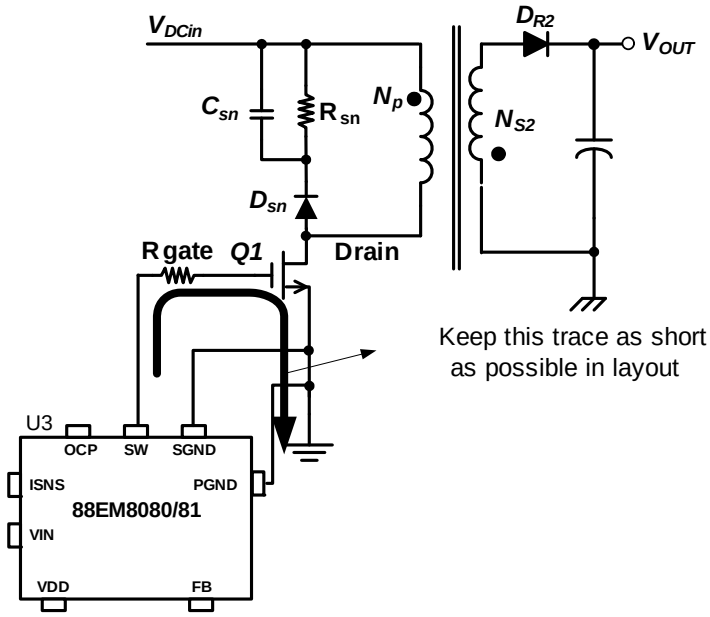
R_1 and R_2 act as voltage dividers to setup the right current limitation threshold. R_2 controls base current of the transistor Q2. R_1 helps to discharge the parasitic capacitance of the transistor. The value of R_1 is recommended as 500~2kΩ, R_2 as 500~2kΩ and R_3 as 10kΩ where R3 is connected between the collector of Q2 and OCP.

A capacitor in parallel with the R_{sns} resistor is used to filter the noise for this OCP circuit to function properly. When the MOSFET turns on, external C_{OSS} of the MOSFET starts discharging. This causes the leading edge spikes of current and increases switching loss. Figure 25 shows that this spike of current causes unwanted over current protection. This phenomenon can be avoided by adding one capacitor, C_{sen}. The leading edge current timing is less than 300ns (typical). C_{sen} is recommended to have a value of 0.22µF/25V. The capacitive reactance of C_{sen} should be far less than R_{sen} for proper filtering of this leading edge current spike.

5.5 SW Pin to MOSFET Gate

The 88EM8080/88EM8081 provides a 1.2A (typical) drive current, which is the strongest driver capability in comparison with the other similar part on the market. A gate resistor of about 20Ω is used between the SW pin and the gate of the external MOSFET. The gate driver loop is subject to fast rise and the layout trace should be kept as short as possible in order to minimize the parasitic inductance, as shown in Figure 27.

Figure 27: SW Pin Layout Guidelines



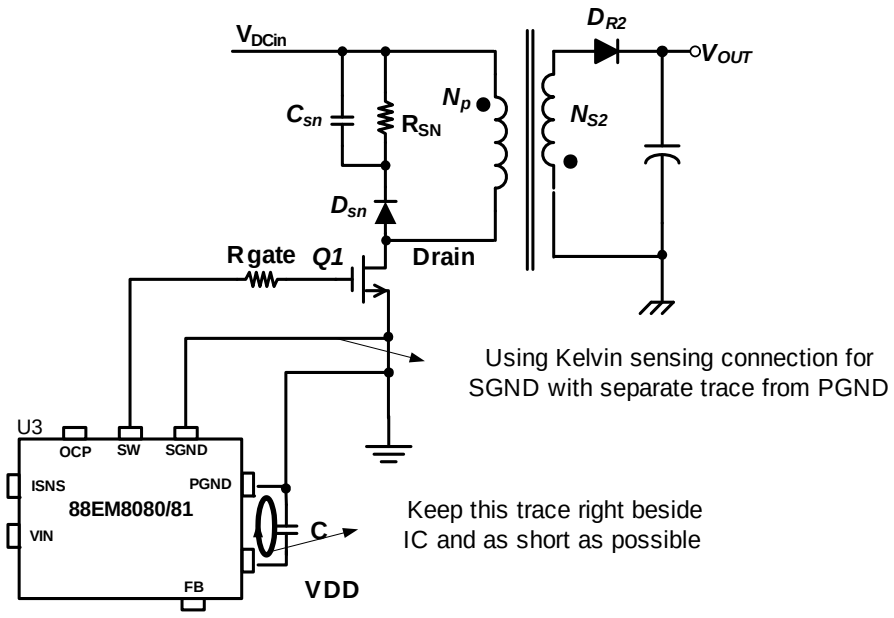
5.6 VDD, Signal (SGND) and Power (PGND) Grounds

VDD is the IC power supply pin. It has a typical value of 12V and a maximum operating voltage of 16V. A Zener diode circuit below 16V is recommended to guarantee that the voltage on VDD will not go any higher than 16V. The IC starts switching when VDD reaches 12V. The IC continues to switch as long as the VDD is higher than V_{DD_UVLO}, which is 7V (typical). An electrolytic capacitor 22µF (typical) is recommended between VDD and ground to keep VDD above 7V during startup. After startup, the bias transformer winding takes over and provides enough energy to power the IC. The description of these functions can be found in Section 3.2.

A 0.01-0.1µF ceramic capacitor is strongly recommended to be placed between the VDD and IC ground with the layout trace as close to the IC as possible. This capacitor is used for decoupling the noise to VDD and to maintain the VDD voltage during the switching of the internal driver circuit.

SGND is directly connected to the system ground by a Kelvin connection trace. The system ground is the source of the MOSFET, as shown in Figure 28. PGND connects to the system ground separately and can not share the same trace with SGND. This is due to pulse current on PGND while driving the external MOSFET on and off. This pulse current produces pulse voltage drops on the PGND trace and may cause the current sensing signal to be distorted if the SGND shares the same trace. Figure 28 provides layout guidelines.

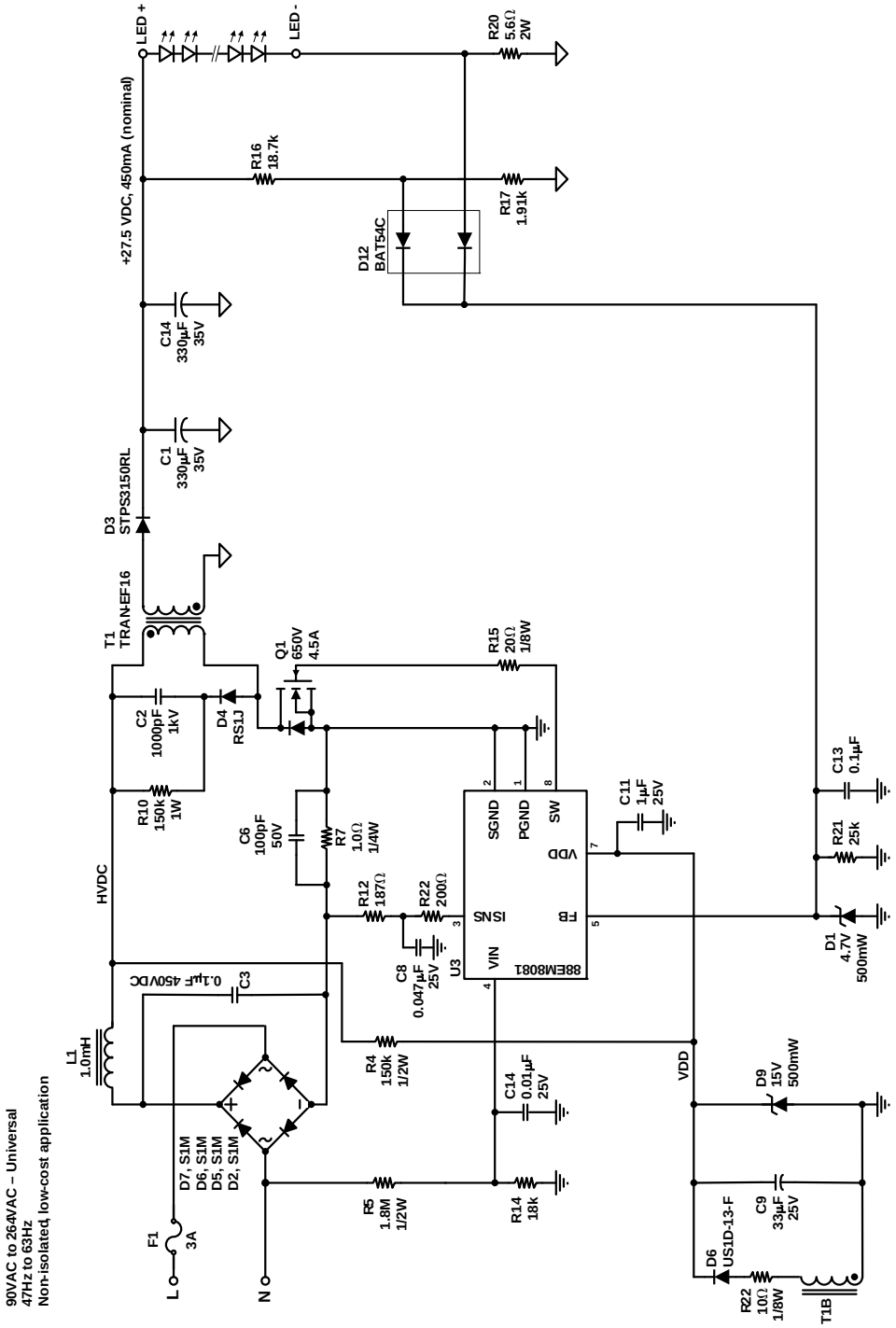
Figure 28: VDD Decoupling Capacitor and Ground Layout Guidelines



5.7 Non-isolated LED Driver

5.7.1 Non-isolated LED Driver Schematic

Figure 29: 1W Non-isolated LED Driver Schematic



5.7.2 Non-isolated LED Driver Description

This is a single stage non-isolated flyback LED driver with output regulation and PFC. The AC input is rectified by the diodes D2,D5,D6 and D7. Fuse F1 is used for AC input over current protection. Inductor L1 used for EMI filtering and also helps for input surge voltage protection. Resistors R5 and R14 provide the necessary voltage at VIN pin for AC Input voltage sensing. Transformer T1 is the flyback transformer and Mosfet Q1 is the primary switch which is driven by Marvell 88EM8080/81 PFC Controller through a gate resistor R15. Diode D4, Resistor R10 and capacitor C2 form the primary RCD clamp. Resistor R7 senses the primary current and provides the input to ISNS pin. Diode D3 is the flyback diode and capacitors C1 and C14 are the output capacitors. Resistor R4 provides the initial bias for the PFC controller from the rectified AC input. Auxiliary winding T1B provides the bias power after startup. Maximum output voltage protection is provided by resistors R16 and R17. The LED current is sensed as the voltage across the resistor R20. The sensed output voltage from the resistor divider network R16 and R17 and the voltage across resistor R20 are both or'ed through the D12 dual diode. The output of D12 is connected to FB pin. C13 is a decoupling capacitor. Zeners D9 and D1 are used for protection.

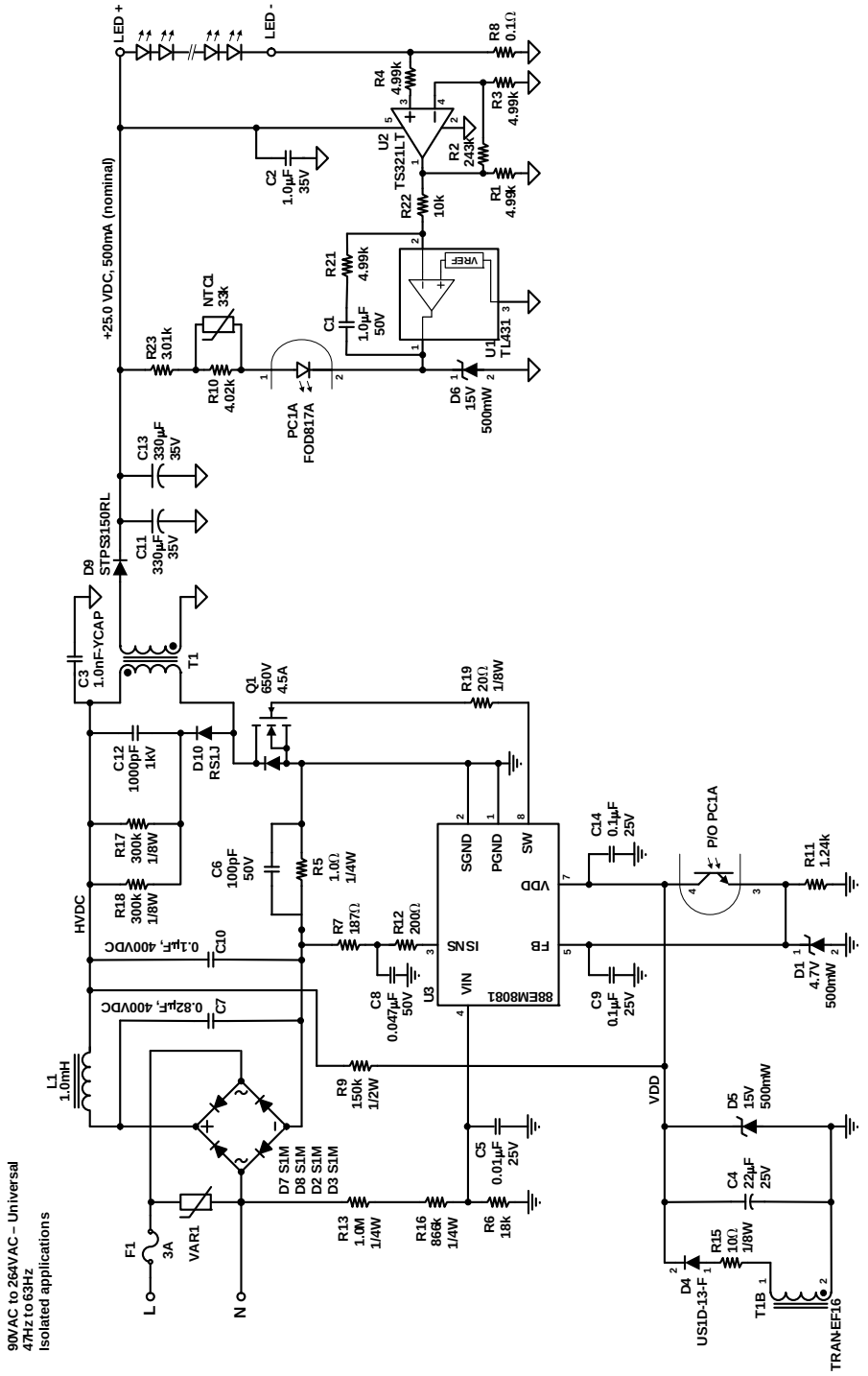
The key points for this design are:

- Output -- 27.5VDC at 450mA
- Universal Input – 90V to 264 VAC
- Dual diode for maximum output voltage protection and for sensing the LED current
- Small size, low cost
- Maximum over voltage protection at 31VDC (typical)
- No optocoupler and no external operational amplifier
- High power factor and low THD throughout the AC line, load and temperature ranges
- No external compensation

5.8 Isolated LED Driver

5.8.1 Isolated LED Driver Schematic

Figure 30: 12.5W Universal Isolated LED Driver Schematic



5.8.2 Isolated LED Driver Description

This is a single stage isolated flyback LED driver with output regulation and PFC. The AC input is rectified by the diodes D2,D3,D7 and D8. Fuse F1 is used for AC input over current protection. Inductor L1 used for EMI filtering and also helps for input surge voltage protection. Resistors R6, R13 and R16 provide the necessary voltage at VIN pin for AC Input voltage sensing. Transfirmer T1 is the flyback transformer and Mosfet Q1 is the primary switch which is driven by Marvell 88EM8080/81 PFC Controller through a gate resistor R19. Diode D10, Resistors R17,R18 and capacitor C12 form the primary RCD clamp. Resistor R5 senses the primary current and provides the input to ISNS pin. Diode D9 is the flyback diode and capacitors C11 and C13 are the output capacitors. Resistor R9 provides the initial bias for the PFC controller from the rectified AC input. A secondary winding T1B of transformer T1, resistor R15, diode D4 and capacitor C4 provides the bias power to VDD pin after starting. Output OVP protection is provided by Zener D6. The LED current is sensed as the voltage across the resistor R8. This sensed voltage is amplified by U2 and then used as the input to the error amplifier U1. The optodiode of PC1A opto coupler is connected to the output of the error amplifier through R23, R10 and the NTC1. The opto transistor of PC1A optocoupler is connected to VDD and R11. The voltage across the resistor R11 is connected to FB pin of the controller. Zeners D1, D5 and D6 are used for protection.

The key points for this design are:

- Output -- 25VDC at 500 mA
- Universal Input – 90V to 264 VAC
- High operating temperature range 0 C to 110 C
- Innovative NTC compensation circuit for stable operating point of the error amplifier throughout the temperature range
- Small size, low cost
- Over voltage protection around 27VDC
- High power factor and low THD throughout the AC line, load and temperature ranges
- High Efficiency

5.8.3 12.5W Universal Isolated LED Driver Test Results

A reference board has been built and tested. The following are the test results.

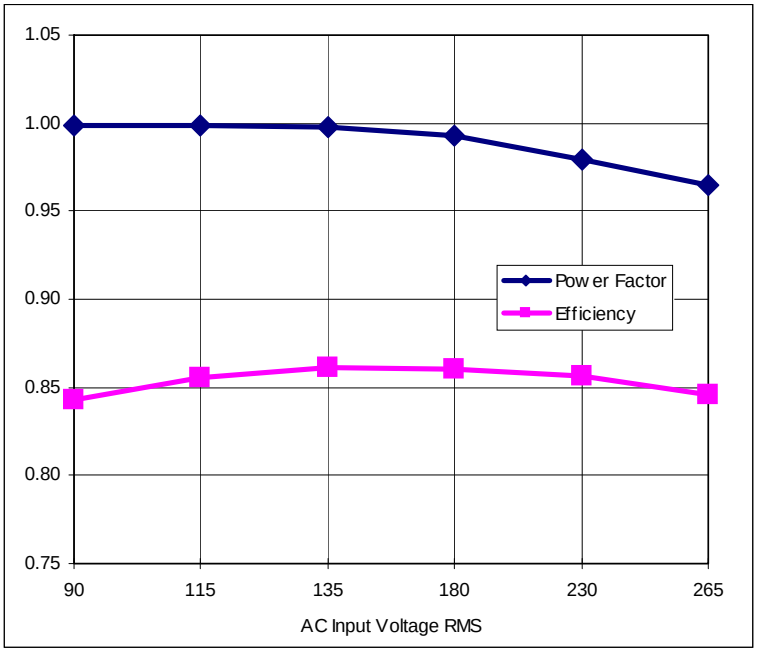
5.8.3.1 Efficiency and Power Factor

The following Table 9 and Figure 31 provides the efficiency, power factor and total harmonic distortion data at various AC input line voltages at full load LED current of 500mA (typical).

Table 9: Efficiency and Power Factor Test Results

Input Voltage (VAC)	Input Current (A)	Input Power (W)	Power Factor	THD	Output Voltage (V)	Output Current (A)	Output Power (W)	Efficiency (%)
90	0.17	15.272	0.999	3.00%	25.41	0.5064	12.87	84.26
115	0.133	15.04	0.999	2.92%	25.4	0.5068	12.87	85.59
135	0.113	14.95	0.998	2.97%	25.39	0.5072	12.88	86.14
180	0.0858	14.987	0.993	3.45%	25.39	0.5076	12.89	85.99
230	0.0684	15.074	0.979	7.00%	25.39	0.5082	12.90	85.60
265	0.0613	15.292	0.965	9.60%	25.39	0.5094	12.93	84.58

Figure 31: Efficiency, Power Factor



5.8.3.2 Start-up Waveforms

Output Voltage and Input Current waveforms were captured at 115AC and 230VAC at full load during start-up and are shown in Figure 32 and Figure 33

Figure 32: Start-up at 115VAC at Full Load

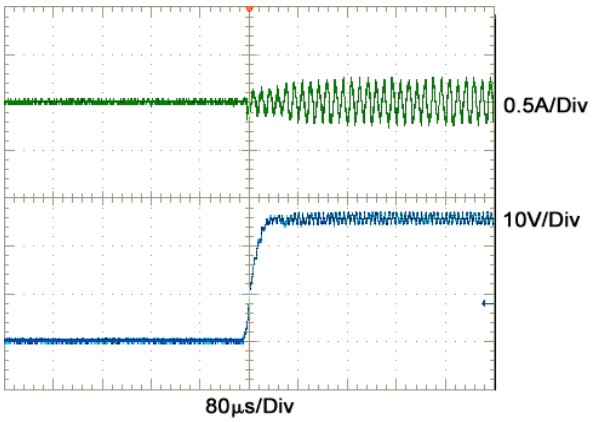
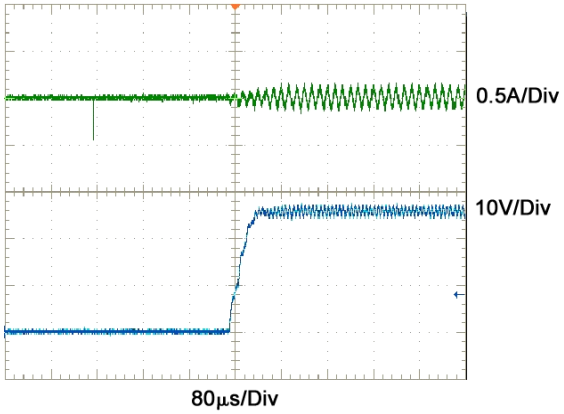


Figure 33: Start-up at 230VAC at Full Load



5.8.3.3 Steady State Waveforms

The steady state output voltage and input current waveforms were captured at 115VAC and 230VAC at full load and are shown in Figure 34 and Figure 35

Figure 34: **Steady State at 115VAC at Full Load**

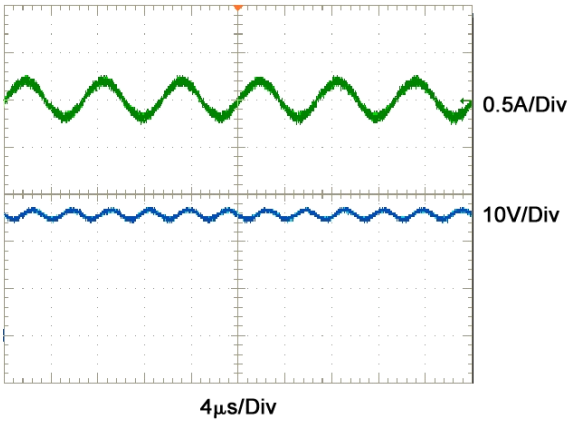
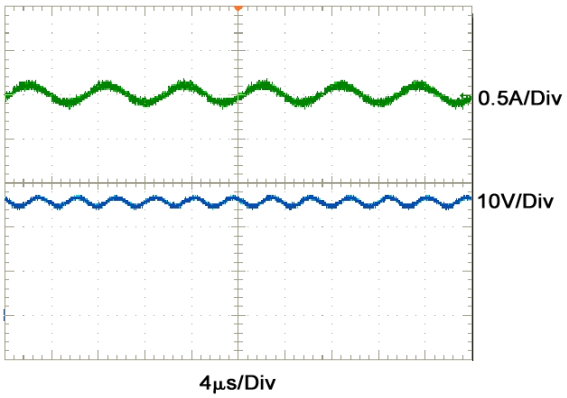
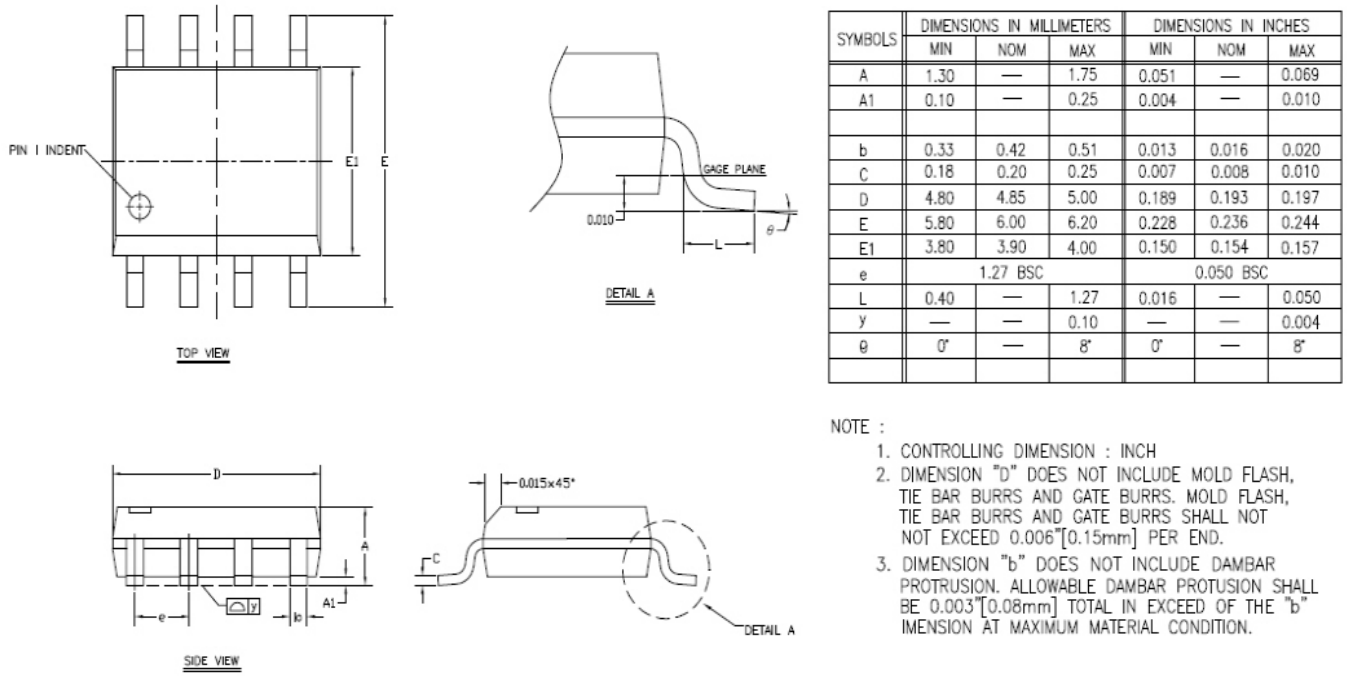


Figure 35: Steady State at 230VAC at Full Load



6.1 Mechanical Drawings

Figure 36: 8-Lead SOIC Mechanical Drawing



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.30	—	1.75	0.051	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
b	0.33	0.42	0.51	0.013	0.016	0.020
C	0.18	0.20	0.25	0.007	0.008	0.010
D	4.80	4.85	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
L	0.40	—	1.27	0.016	—	0.050
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

NOTE :
1. CONTROLLING DIMENSION : INCH
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT NOT EXCEED 0.006"[0.15mm] PER END.
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCEED OF THE "b" IMENSION AT MAXIMUM MATERIAL CONDITION.

Notes:

- All dimensions in mm.
- See Section 7, Part Order Numbering/Package Marking, on page 61 for package marking and pin 1 location.

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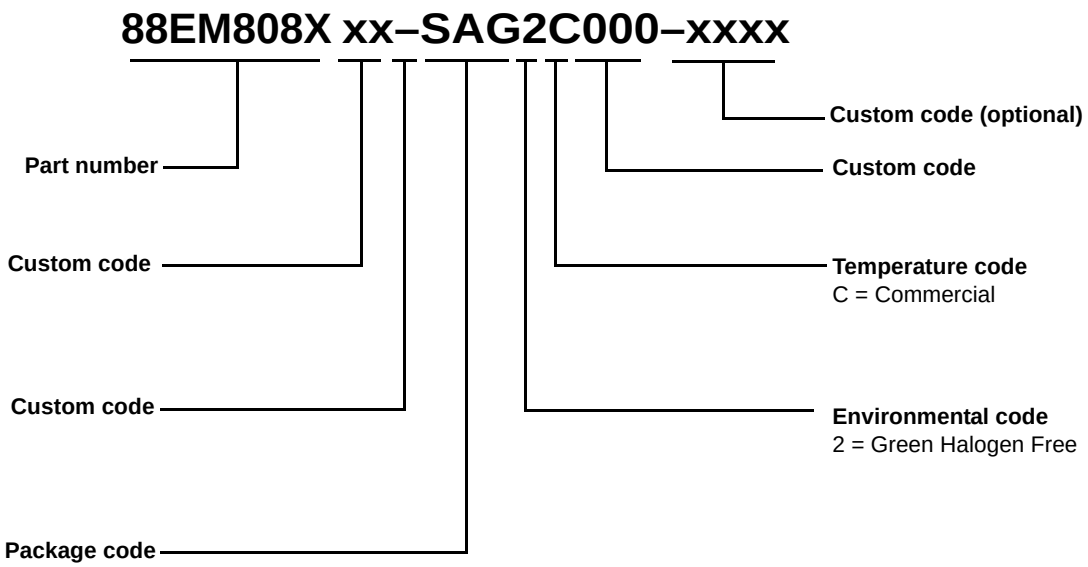
7 Part Order Numbering/Package Marking

7.1 Part Order Numbering

Figure 37 shows the part order numbering scheme. For complete ordering information, contact your Marvell FAE or sales representative.

Figure 37: Sample Ordering Part Number



The standard ordering part number for the respective solution is shown in Table 10.

Table 10: 88EM8080/88EM8081 Part Order Options[1]

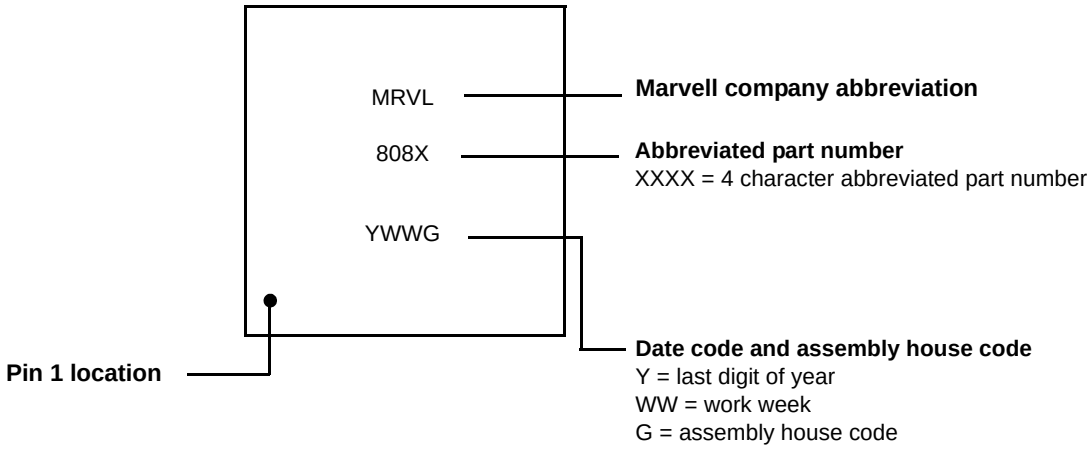
Package Type	Part Order Number
8-Pin SOIC	88EM8080xx-SAG2C000
8-Pin SOIC	88EM8080xx-SAG2C000-T (Tape and Reel)
8-Pin SOIC	88EM8081xx-SAG2C000
8-Pin SOIC	88EM8081xx-SAG2C000-T (Tape and Reel)

1. Please note that the 88EM8080 device is 60kHz and the 88EM8081 device is 120kHz.

7.2 Package Markings

Figure 38 shows a typical package marking and pin 1 location.

Figure 38: Package Marking



Note: The above example is not drawn to scale. Location of markings are approximate.

A Revision History

Table 11: Revision History

Document Type	Document Revision
Release	88EM8080/88EM8081 Rev. B
Reworked Sections: Functional Description and Application Information Revised Sections: • Product overview: added Universal schematic and removed other two • Signal Description:updated pin descriptions • Electrical Characteristics: updated EC table values • Functional Description: completely rewrote section (removed old content) • Application Information: completely rewrote section (reworked old content)	
Release	88EM8080/88EM8081 Rev. A
Changed 30W Isolated Schematic	
Release	88EM8080/88EM8081 Rev. –
First Release	

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