HEWLETT PACKARD

Hermetically Sealed Four Channel Low Input Current Optocoupler

Technical Data

6N140A
6N140A/883B
8302401EC

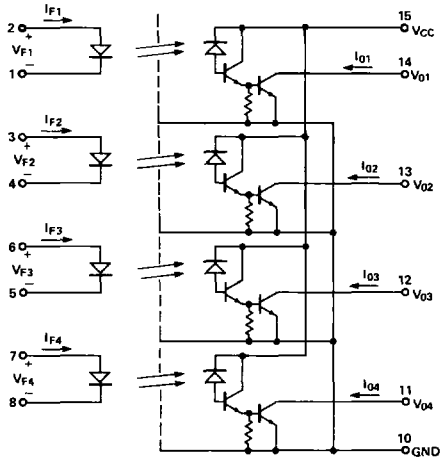
Features

- DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed 8-Pin Dual In-Line Package
- Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range
- MIL-STD-883 Class B Testing
- Internal Shield for Higher CMR
- Low Input Current Requirement: 0.5 mA
- High Current Transfer Ratio: 1500% Typical
- Low Output Saturation Voltage: 0.1 V Typical
- Low Power Consumption
- 1500 VDC Withstand Test Voltage
- High Radiation Immunity
- 6N138/9, HCPL-57XX, 67XX Function Compatibility

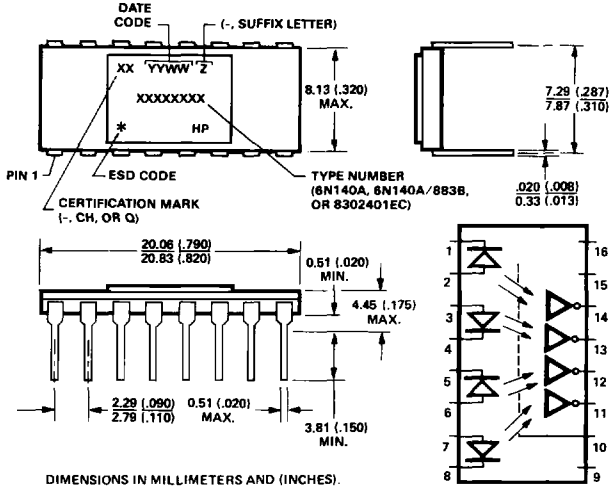
Applications

- Military/High Reliability Systems
- Isolated Input Line Receiver
- System Test Equipment Isolation
- Digital Logic Ground Isolation
- EIA RS-232C Line Receiver
- Microprocessor System Interface
- Current Loop Receiver
- Level Shifting
- Process Control Input/ Output Isolation

Schematic



Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).

HERMETIC OPTOCOUPLERS

Description

The 6N140A is an EIA registered hybrid microcircuit which is capable of operation over the full military temperature range from -55°C to +125°C and is electrically and functionally identical to the 6N140 part. It is an advanced replacement unit for the 6N140. The better performance results from an improved integrated bypass resistor which shunts photodiode and first stage leakage currents. All products within this family have this advanced feature and can be purchased as either a standard product (6N140A), with full MIL-STD-883 Class Level B testing (6N140A/883B) or as parts compliant to DESC Drawing 83024 as (8302401EC). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the DESC part number, or by adding Option 200 to the part number for non-DESC parts.

All three products are in sixteen-pin hermetic dual in-line packages. Each part contains four GaAsP light emitting diodes, each of which is optically coupled to a corresponding integrated high gain photon detector. The high gain output stage features an open collector output providing both lower output saturation voltage and higher speed operation than possible with conventional photodarlington type optocouplers. Also, the separate V_{CC} pin can be strobed low as an output disable or operated with supply voltages as low as 2.0 V without adversely affecting the parametric performance.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

These products have a 300% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS-232C data transmission systems. Compatibility with high voltage CMOS logic systems is assured by the 18 V V_{CC} and by the guaranteed maximum output leakage (IOH) at 18 V. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor optocouplers.

The test program performed on the 8302401EC is in compliance with DESC Drawing 83024. The electrical characteristics table shows Group A Subgroup testing requirements from this drawing.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level (Each Channel)	$V_{F,OFF}$		0.8	V
Input Current, High Level (Each Channel)	$I_{F,ON}$	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Output Current, I_O (each channel) ..... 40 mA
Output Voltage, V_O (each channel) ..... -0.5 to 20 V[1]
Supply Voltage ,V_{CC} ..... -0.5 to 20 V[1]
Output Power Dissipation (each channel) ..... 50 mW[2]
Peak Input Current (each channel, ≤ 1 ms duration) ..... 20 mA
Average Input Current, I_F (each channel) ..... 10 mA[3]
Reverse Input Voltage, V_R (each channel) ..... 5 V

Electrical Characteristics

Parameter	Sym.	Test Conditions	Group A[14] Sub-groups	Limits			Unit	Fig.	Note
				Min.	Typ.**	Max.			
Current Transfer Ratio	$h_{F(CTR)}$*	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1500		%	3	4, 5
		I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1000		%		4, 5
		I_F = 5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	200	500		%		4, 5
Logic Low Output Voltage	V_{OL}	I_F = 0.5 mA, I_{OL} = 1.5 mA, V_{CC} = 4.5 V	1, 2, 3		0.1	0.4	V	2	4
		I_F = 5 mA, I_{OL} = 10 mA, V_{CC} = 4.5 V	1, 2, 3		0.2	0.4	V		4
Logic High Output Current	I_{OH}*	I_F = 2 µA	1, 2, 3		0.001	250	µA		4
	I_{OHX}	V_O = V_{CC} = 18 V	1, 2, 3			250	µA		4, 6
Logic Low Supply Current	I_{CCL}*	I_{F1} = I_{F2} = I_{F3} = I_{F4} = 1.6 mA, V_{CC} = 18 V	1, 2, 3		1.7	4	mA		
Logic High Supply Current	I_{CCH}*	I_{F1} = I_{F2} = I_{F3} = I_{F4} = 0 mA, V_{CC} = 18 V	1, 2, 3		0.001	40	µA		
Input Forward Voltage	V_F*	I_F = 1.6 mA	1, 2		1.44	1.7	V	1	4
			3			1.8	V		4
Input Reverse Breakdown Voltage	BV_R*	I_R = 10 µA	1, 2, 3	5			V		4
Input-Output Insulation Leakage Current	I_{I-O}*	45% Relative Humidity, T = 25°C, t = 5 s, V_{I-O} = 1500 VDC	1			1.0	µA		7, 12
Capacitance Between Input-Output	C_{I-O}	f = 1 MHz, T_C = 25°C	4			4	pF		4, 8
Propagation Delay Time To Logic High At Output	t_{PLH}*	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5.0 V	9, 10, 11		6	60	µs	8	4
		I_F = 5 mA, R_L = 680 Ω, V_{CC} = 5.0 V	9		4	20	µs		4
			10, 11			30	µs		4
Propagation Delay Time To Logic Low At Output	t_{PHL}*	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5.0 V	9, 10, 11		30	100	µs	8	4
		I_F = 5 mA, R_L = 680 Ω, V_{CC} = 5.0 V	9		2	5	µs		4
			10, 11			10	µs		4
Common Mode Transient Immunity At Logic High Level Output	$\|CM_H\|$	I_F = 0, R_L = 1.5 kΩ $\|V_{CM}\|$ = 25 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	1000		V/µs	9	4, 9, 11, 15
Common Mode Transient Immunity At Logic Low Level Output	$\|CM_L\|$	I_F = 1.6 mA, R_L = 1.5 kΩ $\|V_{CM}\|$ = 25 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	1000		V/µs	9	4, 10, 11, 15

*JEDEC Registered Data.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics

T_A = 25°C, V_{CC} = 5 V Each Channel

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 VDC, T_A = 25°C		4, 8
Input-Input Insulation Leakage Current	I_{I-I}		0.5		nA	45% Relative Humidity, V_{I-I} = 500 VDC T_A = 25°C, t = 5 s		13
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I} = 500 VDC, T_A = 25°C		13
Capacitance (Input-Input)	C_{I-I}		1		pF	f = 1 MHz, T_A = 25°C		13
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.8		mV/°C	I_F = 1.6 mA		4
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0, T_A = 25°C		4

Notes:

1. Pin 10 should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 volts, will provide lowest total I_{O_H} over temperature.
2. Output power is collector output power plus one fourth of total supply power. Derate at 1.66 mW/°C above 110°C.
3. Derate I_F at 0.33 mA/°C above 110°C.
4. Each channel.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. I_F = 2 μA for channel under test. For all other channels, I_F = 10 mA.
7. Device considered a two-terminal device: Pins 1 through 8 are shorted together and pins 9 through 16 are shorted together.
8. Measured between the LED anode and cathode shorted together and pins 10 through 15 shorted together.
9. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
10. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
11. In applications where dV/dt may exceed 50,000 V μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector ICs from destructively high surge currents. The recommended value is

$$R_{CC} \approx \frac{1\ V}{0.6\ I_F\ (mA)}\ k\Omega$$

12. This is a momentary withstand test, not an operating condition.
13. Measured between adjacent input pairs shorted together, i.e., between pins 1 and 2 shorted together, and pins 3 and 4 shorted together, etc.
14. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
15. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified in Table I for all lots not specifically tested. Subgroup 9 shall be tested with every lot.

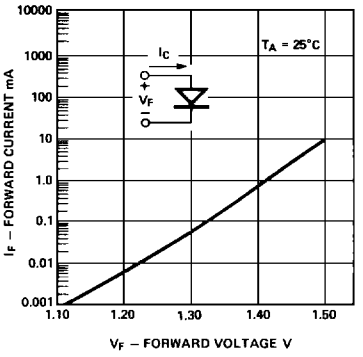


Figure 1. Input Diode Forward Current vs Forward Voltage.

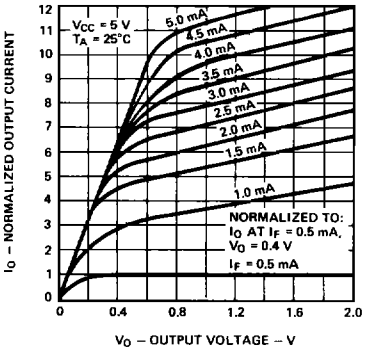


Figure 2. Normalized DC Transfer Characteristics.

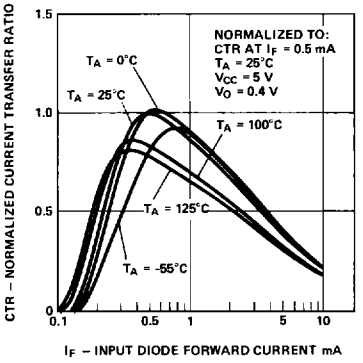


Figure 3. Normalized Current Transfer Ratio vs Input Diode Forward Current.

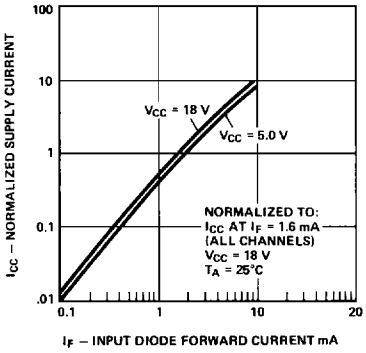


Figure 4. Normalized Supply Current vs Input Diode Forward Current.

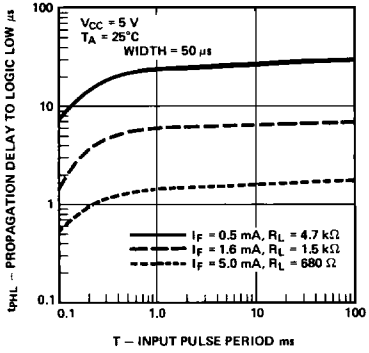


Figure 5. Propagation Delay to Logic Low vs Input Pulse Period.

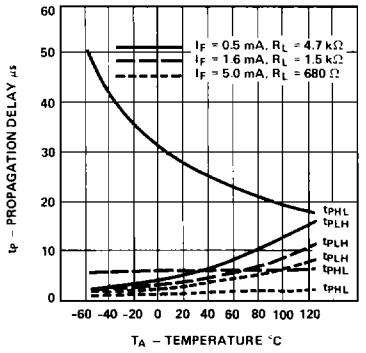


Figure 6. Propagation Delay vs Temperature.

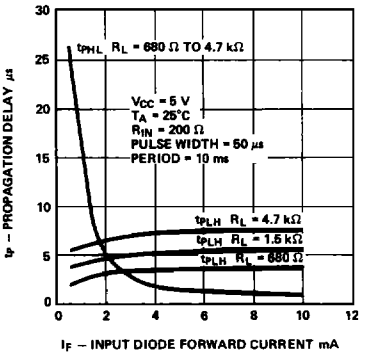


Figure 7. Propagation Delay vs Input Diode Forward Current.

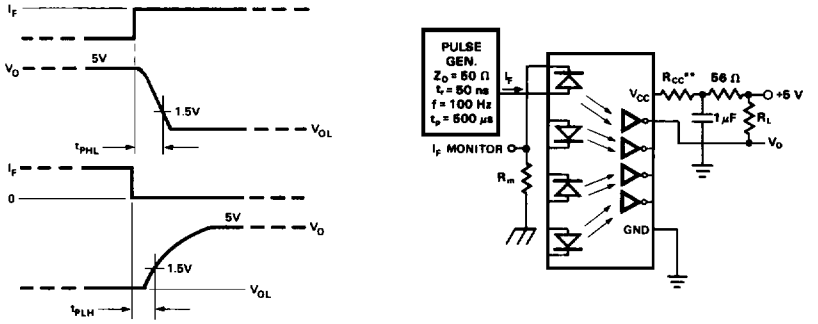


Figure 8. Switching Test Circuit (f, t_p not JEDEC registered).*

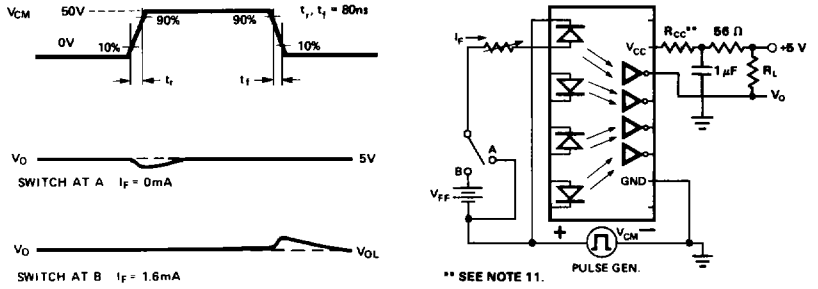


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

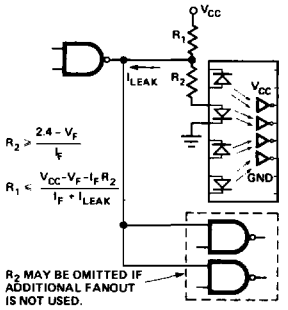


Figure 10. Recommended Drive Circuitry Using TTL Open-Collector Logic.

SMD 8302401EC and MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC drawings 83024 for an H.P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

6N140A/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.

Group A–See Electrical Characteristics Table.

Group B–No change.

Group C–No change.

Group D–Constant Acceleration–Condition A not E.

Part Numbering System

Commercial Product	Class B Product	SMD Product
6N140A	6N140A/883B	8302401EC

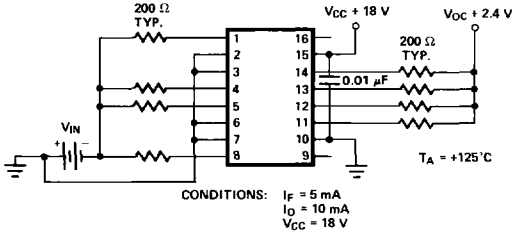


Figure 11. Operating Circuit for Burn-In and Steady State Life Tests.