Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... – 40 to + 85 °C
Storage temperature (T_{ST}) ..... – 65 to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) ..... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition ..... – 10 mA to + 10 mA
Absolute sum of all input currents during overload condition ..... | 100 mA |

Power dissipation ..... TBD

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 °C to 70 °C for the SAB-C501
T_A = – 40 °C to 85 °C for the SAF-C501

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except XTAL1, $\overline{EA}$, RESET)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	
Input high voltage to $\overline{EA}$, RESET	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA [2], I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C
Power supply current:					
Active mode, 12 MHz [7]	I_{CC}	–	21	mA	V_{CC} = 5 V, [4]
Idle mode, 12 MHz [7]	I_{CC}	–	4.8	mA	V_{CC} = 5 V, [5]
Active mode, 20 MHz [7]	I_{CC}	–	31.1	mA	V_{CC} = 5 V, [4]
Idle mode, 20 MHz [7]	I_{CC}	–	7.0	mA	V_{CC} = 5 V, [5]
Active mode, 40 MHz [7]	I_{CC}	–	56.5	mA	V_{CC} = 5 V, [4]
Idle mode, 40 MHz [7]	I_{CC}	–	12.5	mA	V_{CC} = 5 V, [5]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 ... 5.5 V [3]

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall bellow the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{GLCH}, t_{CHGL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = RESET= V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{GLCH}, t_{CHGL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

7) $I_{CC\ Max}$ at other frequencies is given by:
active mode: I_{CC} = 1.27 x f_{OSC} + 5.73
idle mode: I_{CC} = 0.28 x f_{OSC} + 1.45
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

AC Characteristics for SAB-C501-LN / C501-RN

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to 70 °C for the SAB-C501
T_A = – 40 °C to 85 °C for the SAF-C501

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values		Unit
		12 MHz Clock	Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz	

AC Characteristics for SAB-C501-L / C501-1R

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	30	–	$t_{CLCL} - 53$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics for SAB-C501-L20 / C501-1R20

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to 70 °C for the SAB-C501
T_A = – 40 °C to 85 °C for the SAF-C501

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	60	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	20	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	20	–	$t_{CLCL} - 30$	–	ns
ALE low to valid instr in	t_{LLIV}	–	100	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	25	–	$t_{CLCL} - 25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	115	–	$3t_{CLCL} - 35$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	75	–	$3t_{CLCL} - 75$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	40	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	47	–	$t_{CLCL} - 3$	–	ns
Address to valid instr in	t_{AVIV}	–	190	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C501 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C501-L20 / C501-1R20

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	200	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	200	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	20	–	$t_{CLCL} - 30$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	155	–	$5t_{CLCL} - 95$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	76	–	$2t_{CLCL} - 24$	ns
ALE to valid data in	t_{LLDV}	–	250	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	285	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	100	200	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	20	80	$t_{CLCL} - 30$	$t_{CLCL} + 30$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 45$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	200	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	10	–	$t_{CLCL} - 40$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 20 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	50	285.7	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	12	ns
Fall time	t_{CHCL}	–	12	ns

AC Characteristics for SAB-C501-L40 / C501-1R40

Advance Information

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to 70 °C for the SAB-C501
T_A = – 40 °C to 85 °C for the SAF-C501

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	$2\,t_{CLCL}-15$	–	ns
Address setup to ALE	t_{AVLL}	10	–	$t_{CLCL}-15$	–	ns
Address hold after ALE	t_{LLAX}	10	–	$t_{CLCL}-15$	–	ns
ALE low to valid instr in	t_{LLIV}	–	55	–	$4\,t_{CLCL}-45$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	10	–	$t_{CLCL}-15$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	60	–	$3\,t_{CLCL}-15$	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	25	–	$3\,t_{CLCL}-50$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	15	–	$t_{CLCL}-10$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	20	–	$t_{CLCL}-5$	–	ns
Address to valid instr in	t_{AVIV}	–	65	–	$5\,t_{CLCL}-60$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	– 5	–	– 5	–	ns

*) Interfacing the SAB-C501 to devices with float times up to 20ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C501-L40 / C501-1R40 (cont'd)

Advance Information

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	6 t_{CLCL} – 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	6 t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX2}	10	–	2 t_{CLCL} – 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	5 t_{CLCL} – 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	2 t_{CLCL} – 12	ns
ALE to valid data in	t_{LLDV}	–	150	–	8 t_{CLCL} – 50	ns
Address to valid data in	t_{AVDV}	–	150	–	9 t_{CLCL} – 75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	3 t_{CLCL} – 15	3 t_{CLCL} + 15	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	4 t_{CLCL} – 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	t_{CLCL} – 15	t_{CLCL} + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	t_{CLCL} – 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	7 t_{CLCL} – 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	t_{CLCL} – 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

Advance Information

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	285.7	ns
High time	t_{CHCX}	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	10	ns
Fall time	t_{CHCL}	–	10	ns

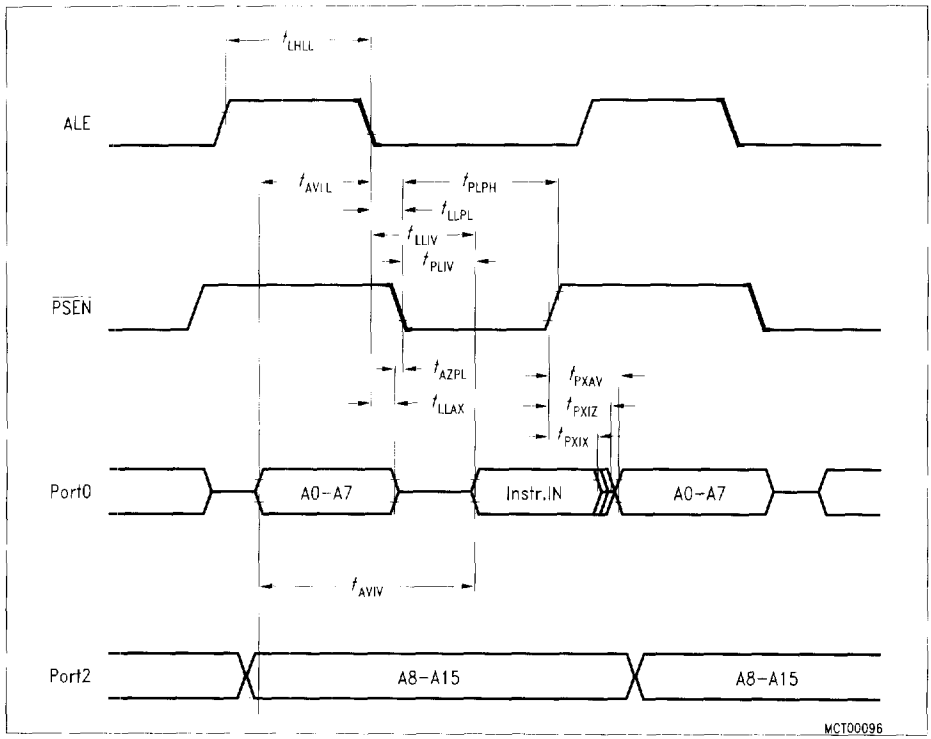


Figure 1
Program Memory Read Cycle

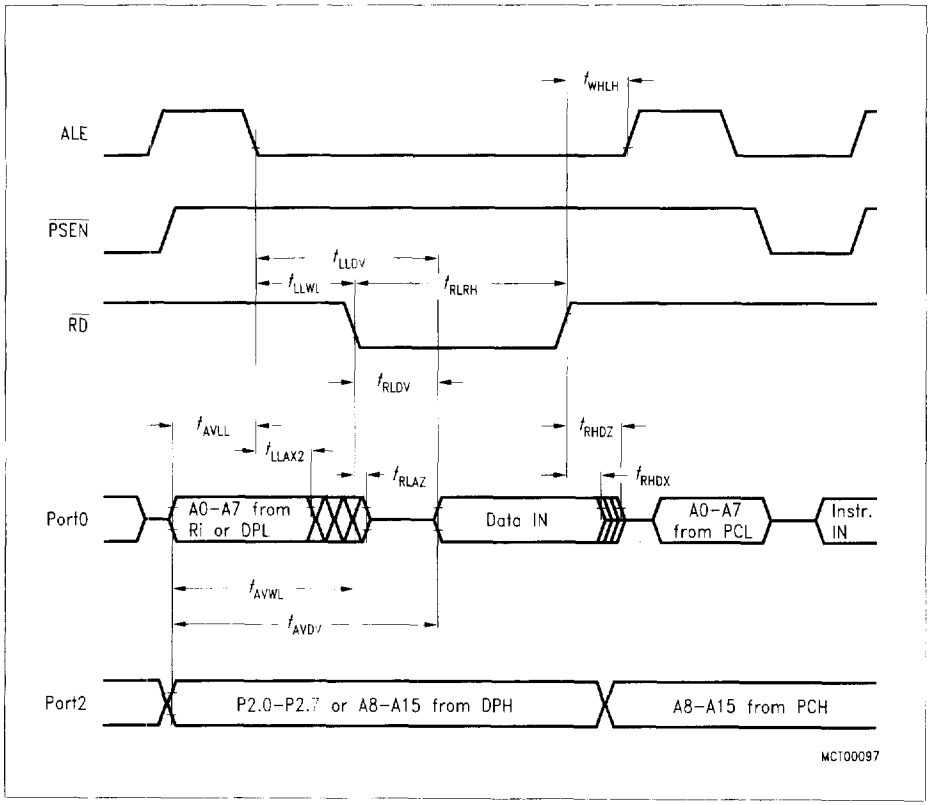


Figure 2
Data Memory Read Cycle

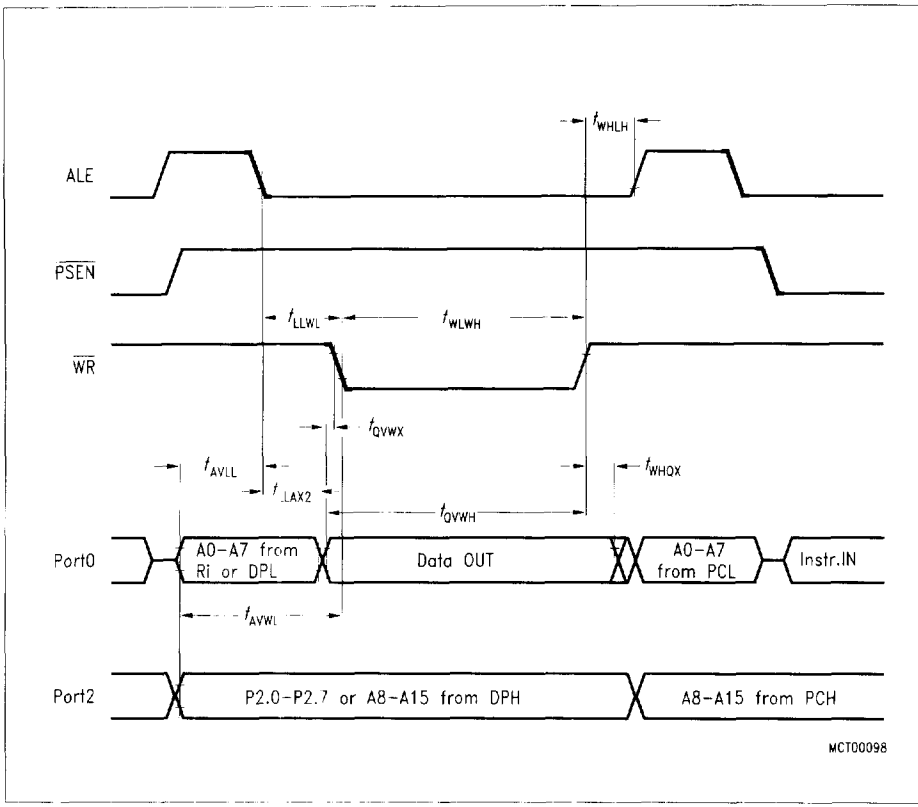
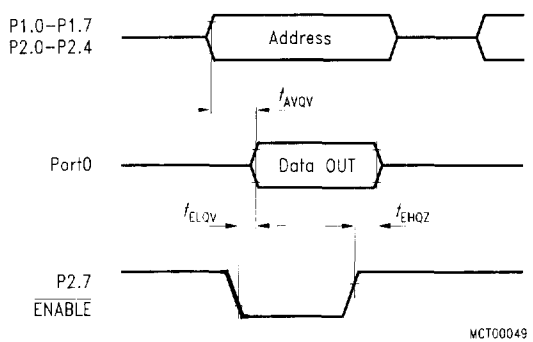


Figure 3
Data Memory Write Cycle

ROM Verification Characteristics for SAB-C501-1R

ROM Verification Mode 1

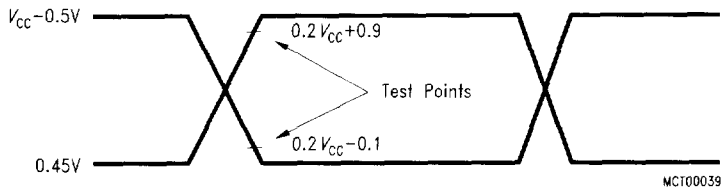
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0–P1.7=A0–A7
P2.0–P2.4=A8–A12
Data: P0.0–P0.7=D0–D7

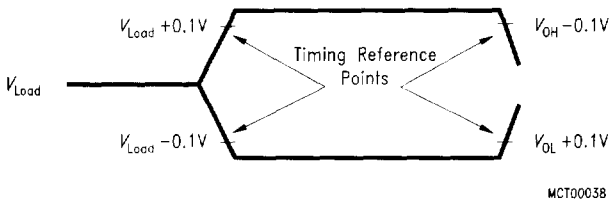
Inputs: P2.5–P2.6, $\overline{PSEN}=V_{SS}$
ALE, $\overline{EA}=V_{IH}$
RESET = V_{IH1}

Figure 4
ROM Verification Mode 1



AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 5
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs. I_{OL} / $I_{OH} \geq \pm 20$ mA.

Figure 6
AC Testing: Float Waveforms

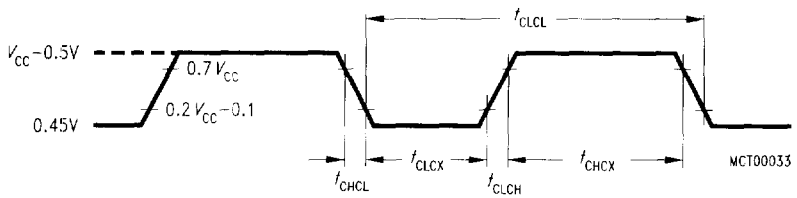


Figure 7
External Clock Cycle

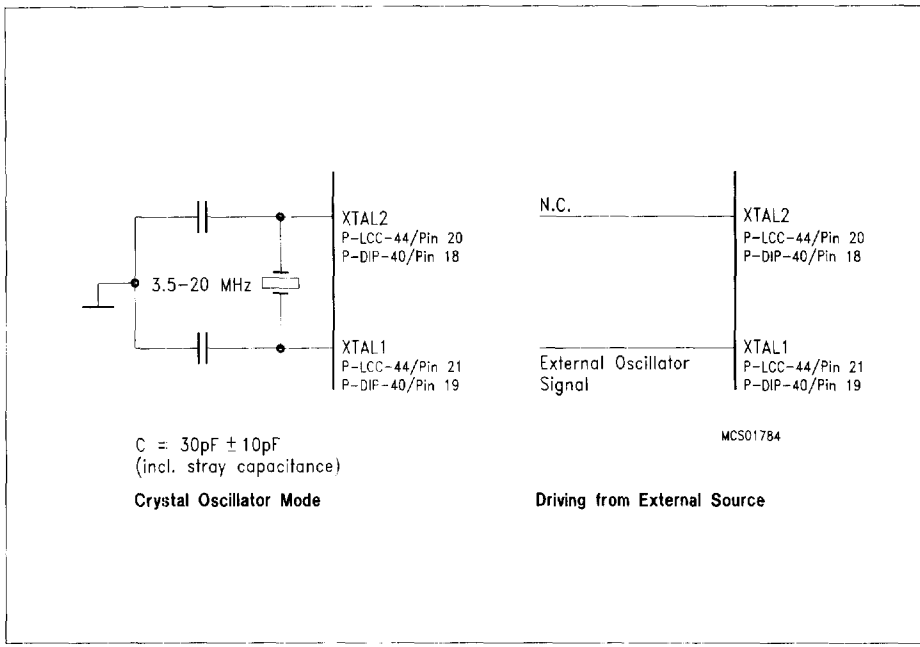


Figure 8
Recommended Oscillator Circuits