

# LC89971, 89971M

# **Multi-system CCD Delay Line**

## Overview

The LC89971 and LC89971M are CCD delay lines for multi television systems. They incorporate a comb filter for chrominance signal and a 1H delay line for luminance signal.

#### Structure

• NMOS + CCD

### **Functions**

- Two CCD shift registers (for chrominance and luminance signals)
- · CCD drive circuits
- CCD stage count switching circuit
- CCD signal adder
- · Auto-bias circuit
- Sync tip clamping circuit (luminance signal)
- Center-bias circuit (chrominance signal)
- · Sample-and-hold circuit
- PLL 4 × frequency multiplier
- fsc clock output circuit
- · RD voltage generator

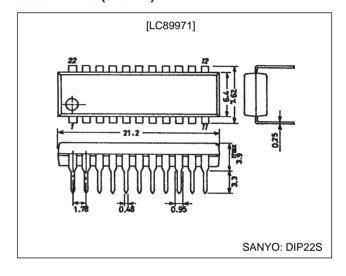
## **Features**

- 5 V single-voltage power supply
- Built-in PLL 4 × frequency multiplier circuit allows 4 fsc operation from an fsc (3.58 MHz) input.
- Control pin switchable to handle NTSC/M, PAL/GBI and PAL/M systems.
- Built-in chrominance signal crosstalk exclusion comb filter features high precision comb characteristics in an adjustment-free circuit.
- Built-in peripheral circuits allow applications to be constructed with a minimum number of external components.
- Positive-phase signal input/positive-phase signal output (luminance signal)

## **Package Dimensions**

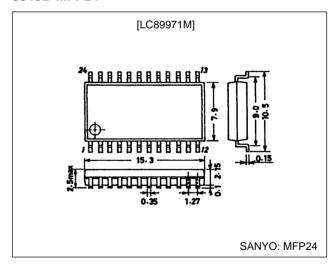
unit: mm

3059-DIP22S (375 mil)



unit: mm

#### 3045B-MFP24



## **Specifications**

## **Absolute Maximum Ratings at Ta = 25°C**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max		-0.3 to +6.0	V
Allowable power dissipation	Pd max	LC89971	1200	mW
	Pulliax	LC89971M	600	mW
Operating temperature	Topr		-10 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

## LC89971, 89971M

# Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}$		4.75	5.00	5.25	V
Clock input amplitude	V <sub>CLK</sub>		300	500	1000	mVp-p
Clock frequency	F <sub>CLK</sub>	Sine wave	_	3.579545	_	MHz
Clock signal input amplitude	V <sub>IN-C</sub>		_	350	500	mVp-p
Luminance signal input amplitude	V <sub>IN-Y</sub>		_	400	572	mVp-p

# Electrical Characteristics at $V_{DD}$ = 5.0 V, Ta = 25°C, $F_{CLK}$ = 3.579545 MHz, $V_{CLK}$ = 500 mVp-p

Parameter			Switch	states		O a madistica and		typ	max	Unit
	Symbol	SW1	SW2	SW3	SW4	Conditions	min			
	I <sub>DD-1</sub>	а	а	а	b			55	65	mA
Supply current	I <sub>DD-2</sub>	а	b	а	b	1	45			
	I <sub>DD-3</sub>	b	b	а	b					
Chrominance System Characteristics (with no Y-IN input)										
	V <sub>INC-1</sub>	а	а	а	b				2.8	V
Pin voltage (input)	V <sub>INC-2</sub>	а	b	а	b		2.0	2.4		
	V <sub>INC-3</sub>	b	b	а	b	2				
	V <sub>OUYC-1</sub>	а	а	а	b	_				
Pin voltage (output)	V <sub>OUTC-2</sub>	а	b	а	b		1.2	1.6	2.0	V
	V <sub>OUTC-3</sub>	b	b	а	b					
	G <sub>VC-1</sub>	а	а	а	b				+2	
Voltage gain	G <sub>VC-2</sub>	а	b	а	b	3	-2	0		dB
	G <sub>VC-3</sub>	b	b	а	b					
	C <sub>D-1</sub>	а	а	а	b	4	_	-40	-35	dB
Comb depth	C <sub>D-2</sub>	а	b	а	b					
	C <sub>D-3</sub>	b	b	а	b					
	L <sub>NC-1</sub>	а	а	а	b	5	-0.3	0.0	+0.3	dB
Linearity	L <sub>NC-2</sub>	а	b	а	b					
	L <sub>NC-3</sub>	b	b	а	b					
	L <sub>CK4C-1</sub>	а	а	а	b		_	10	50	mVrms
Clock leakage (4 fsc)	L <sub>CK4C-2</sub>	а	b	а	b					
	L <sub>CK4C-3</sub>	b	b	а	b	6				
	L <sub>CK1C-1</sub>	а	а	а	b	-				
Clock leakage (fsc)	L <sub>CK1C-2</sub>	а	b	а	b		_	0.8	1.5	mVrms
	L <sub>CK1C-3</sub>	b	b	а	b					
	N <sub>C-1</sub>	а	а	а	b					
Noise	N <sub>C-2</sub>	а	b	а	b	7	_	0.5	2.0	mVrms
	N <sub>C-3</sub>	b	b	а	b					
Output impedance	Z <sub>OC-1</sub>	а	а	а	a, b					
	Z <sub>OC-2</sub>	а	b	а	a, b	8	200	350	500	Ω
	Z <sub>OC-3</sub>	b	b	а	a, b					
	T <sub>DC-1</sub>	а	а	а	b			230		
0 H delay time	T <sub>DC-2</sub>	а	b	а	b	9	_		_	ns
	T <sub>DC-3</sub>	b	b	а	b					

Continued from preceding page.

Parameter			Switch	states		O andidiana	min	typ	max	Unit
	Symbol	SW1	SW2	SW3	SW3 SW4 Conditions	Conditions				
Luminance System Characteristi	cs (with no C-IN	11 or C-II	N2 input)							
Pin voltage (input)	V <sub>INY-1</sub>	а	а	а	b				2.5	V
	V <sub>INY-2</sub>	а	b	а	b		1.7	2.1		
	V <sub>INY-3</sub>	b	b	а	b	10				
	V <sub>OUTY-1</sub>	а	а	а	b	10			1.6	V
Pin voltage (output)	V <sub>OUTY-2</sub>	а	b	а	b		0.8	1.2		
	V <sub>OUTY-3</sub>	b	b	а	b					
	G <sub>VY-1</sub>	а	а	а	b					
Voltage gain	G <sub>VY-2</sub>	а	b	а	b	11	-2	0	+2	dB
	G <sub>VY-3</sub>	b	b	а	b					
	G <sub>FY-1</sub>	а	а	b	b					
Frequency responce	G <sub>FY-2</sub>	а	b	b	b	12	-2	0	+2	dB
	G <sub>FY-3</sub>	b	b	b	b					
	D <sub>GY-1</sub>	а	а	а	b		0	5	7	%
Differential gain	D <sub>GY-2</sub>	а	b	а	b	13				
	D <sub>GY-3</sub>	b	b	а	b					
	D <sub>PY-1</sub>	а	а	а	b		0	5		
Differential phase	D <sub>PY-2</sub>	а	b	а	b				7	deg
	D <sub>PY-3</sub>	b	b	а	b					
	L <sub>SY-1</sub>	а	а	а	b		37	40	43	%
Linearity	L <sub>SY-2</sub>	а	b	а	b	14				
	L <sub>SY-3</sub>	b	b	а	b					
	L <sub>CK4Y-1</sub>	а	а	а	b		_	10	50	mVrms
Clock leakage (4 fsc)	L <sub>CK4Y-2</sub>	а	b	а	b					
	L <sub>CK4Y-3</sub>	b	b	а	b	15				
	L <sub>CK1Y-1</sub>	а	а	а	b	15				
Clock leakage (fsc)	L <sub>CK1Y-2</sub>	а	b	а	b		_	0.8	1.5	mVrms
	L <sub>CK1Y-3</sub>	b	b	а	b					
	N <sub>Y-1</sub>	а	а	а	b					
Noise	N <sub>Y-2</sub>	а	b	а	b	16	_	0.5	2.0	mVrms
	N <sub>Y-3</sub>	b	b	а	b					
Output impedance	Z <sub>OY-1</sub>	а	а	а	c, b					Ω
	Z <sub>OY-2</sub>	а	b	а	c, b	17	250	400	550	
	Z <sub>OY-3</sub>	b	b	а	c, b					
	T <sub>DY-1</sub>	а	а	а	b		_	63.88	_	
Delay time	T <sub>DY-2</sub>	а	b	а	b	18	_	63.46	_	μs
	T <sub>DY-3</sub>	b	b	а	b		_	63.46	_	

## **Test Conditions**

- 1. Supply current with no signal input.
- 2. C-OUT voltage (center bias voltage) with no signal input.
- 3. Measure the C-OUT output with 350 mVp-p sine wave signals input to C-IN1 and C-IN2.

$$GVC = 20 log \frac{C\text{-}OUT output [mVp-p]}{350 [mVp-p]} [dB]$$

Test frequencies

GVC-1 4.431395 MHz (PAL/GBI)

GVC-2 3.571628 MHz (PAL/M)

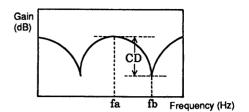
GVC-3 3.571628 MHz (NTSC/M)

4. Measure the comb depth from the C-OUT output with a 350 mVp-p sine wave signal of frequency fa input to C-IN1 and C-IN2 and with a frequency of fb input.

$$CD = 20 log \frac{C\text{-OUT output with fb input } [mVp\text{-}p]}{C\text{-OUT output with fa input } [mVp\text{-}p]} [dB]$$

Test frequencies

	fa	fb
CD-1	4.431395 MHz	4.435303 MHz (PAL/GBI)
CD-2	3.571628 MHz	3.575561 MHz (PAL/M)
CD-3	3.571628 MHz	3.575561 MHz (NTSC/M)



5. Measure the C-OUT output with a 200 mVp-p sine wave signal input to C-IN1 and C-IN2 and with 500 mVp-p sine wave signal input and calculate the difference in the gains.

$$LNC = 20 log \left( \frac{Output for a 500 \ mVp-p \ input \ [mVp-p]}{500 \ [mVp-p]} \ \middle/ \frac{Output for a 200 \ mVp-p \ input \ [mVp-p]}{200 \ [mVp-p]} \right) \ [dB]$$

Test frequencies

LNC-1 4.431395 MHz (PAL/GBI) LNC-2 3.571628 MHz (PAL/M) LNC-3 3.571628 MHz (NTSC/M)

6. Measure the 4 fsc (14.3 MHz) and fsc (3.58 MHz) components in the C-OUT output with no input.

7. Measure the noise in the C-OUT output with no input.

Measure the noise with a noise meter set up with a 200 kHz high-pass filter and a 5 MHz low-pass filter.

8. Let V1 be the C-OUT output with a 350 mVp-p sine wave input to C-IN1 and C-IN2 and SW3 set to a, and let V2 be the C-OUT output with SW3 set to b.

$$ZOC = \frac{V2 \ [mVp-p] - V1 \ [mVp-p]}{V1 \ [mVp-p]} \times 500 \ [\Omega]$$

Test frequencies

ZOC-1 4.431395 MHz (PAL/GBI) ZOC-2 3.571628 MHz (PAL/M) ZOC-3 3.571628 MHz (NTSC/M)

9. The C-OUT output delay time with respect to inputs to C-IN1. (the CCD 2.5 bit delay)

10. Y-OUT voltage (clamp voltage) with no signal input.

11. Measure the Y-OUT output with a 200 kHz 400 mVp-p sine wave input to Y-IN.

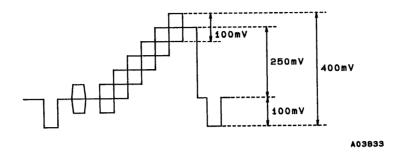
$$GVY = 20 log \frac{Y\text{-}OUT output [mVp-p]}{400 [mVp-p]} [dB]$$

12. Measure the Y-OUT output with a 200 kHz 200 mVp-p sine wave input to Y-IN and with a 3.3 MHz 200 mVp-p sine wave input.

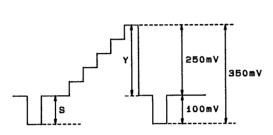
$$GFY = 20 log \ \frac{Y\text{-OUT output with a 3.5 MHz input } [mVp\text{-}p]}{Y\text{-OUT output with a 200 kHz input } [mVp\text{-}p]} \ [dB]$$

Note that  $V_{bias}$  should be adjusted so that the circuit is biased to the clamp level plus 250 mV.

13. Input a five-level step waveform (see the figure below) to Y-IN and measure the differential gain and differential phase in the Y-OUT output with a vector scope.



14. Input a five-level step waveform (see the figure below) to Y-IN and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.



$$LS = \frac{S [mV]}{Y [mV]} \times 100 [\%]$$

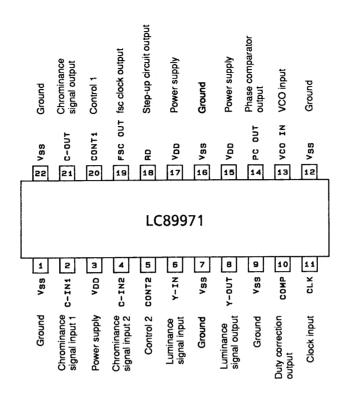
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- 15. Measure the 4 fsc (14.3 MHz) and fsc (3.58 MHz) components in the Y-OUT output with no input.
- 16. Measure the noise in the Y-OUT output with no input.
  Measure the noise with a noise meter set up with a 200 kHz high-pass filter, a 4.2 MHz low-pass filter, and a 3.58 MHz trap filter.
- 17. Let V1 be the Y-OUT output with a 200 kHz 400 mVp-p sine wave input and SW4 set to c, and let V2 be the C-OUT output with SW4 set to b.

$$ZOY = \frac{V2 [mVp-p] - V1 [mVp-p]}{V1 [mVp-p]} \times 500 [\Omega]$$

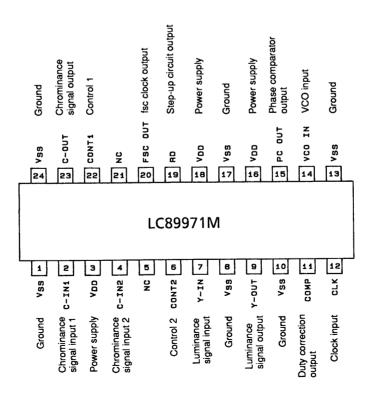
18. The Y-OUT delay time with respect to Y-IN

## Pin Assignment [LC89971]



A03830 Top view

## Pin Assignment [LC89971M]



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## **Block Diagram**

CCD Center C-IN1 bias 2.5 bits 21 (23) C-OUT CCD 912.5 bit Center C-IN2 CCD 12 bits Input Auto-bias switching circuit 1 CONT 1 20 (22) CONT2 5 (6) 8 (9) Y-OUT Sync chip 6 (7) CCD clamp 6 bits Input 18 (19) RD switching Auto-bias circuit 2 Duty correction Clock driver

Note \* Pin numbers in parentheses are for the LC89971M.

### **Control Pin Function**

VCO IN 13 (14)

CONT1	CONT2 Mode (representative example) Chrominance signal delay (CCD bits)		, ,	Luminance signal delay (CCD bits)	
Low	Low	PAL/GBI	2 H (1834.5) + 0 H (2.5)	1 H (914)	
Low	High	PAL/M	2 H (1822.5) + 0 H (2.5)	1 H (908)	
High	Low	_	_	_	
High	High	NTSC/M	1 H (912.5) + 0 H (2.5)	1 H (908)	

Timing generator

14 (15) PC OUT

## **Switching Voltage Levels**

Low/high	Symbol	min	typ	max	Unit
Low	VL	-0.3	0.0	0.5	V
High	V <sub>H</sub>	2.0	5.0	6.0	V

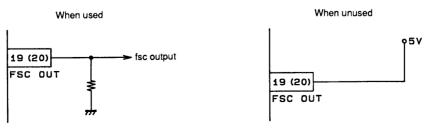
vco

1/4

Note: Since the control pin has a built-in pull-down resistor ( $\approx 70 \text{ k}\Omega$ ), the pin will be set to the low state if left open.

### **FSC OUT Pin Function**

This pin provides a buffer output for the clock signal input to the CLK pin.



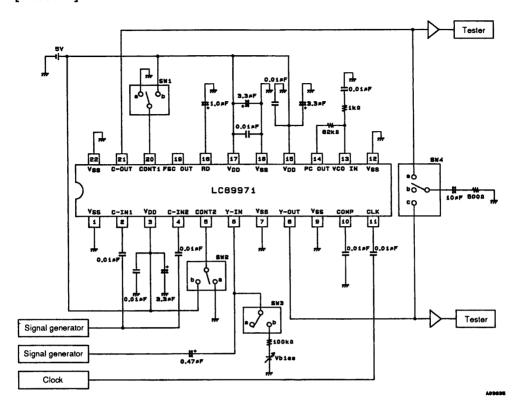
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10 (11) COMP

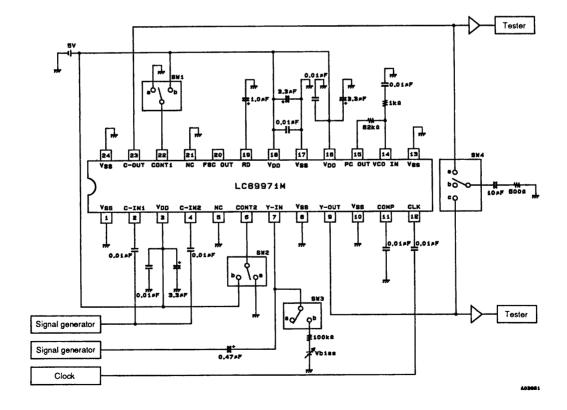
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Note: Since this pin has a built-in pull-up resistor, the pin voltage will go to the supply voltage and output will cease if left open.

# Test Circuit [LC89971]



# Test Circuit [LC89971M]



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