Ordering number : EN4900A

MOS IC

LC89971, 89971M

Multi-system CCD Delay Line

Overview

The LC89971 and LC89971M are CCD delay lines for multi television systems. They incorporate a comb filter for chrominance signal and a 1H delay line for luminance signal.

Structure

- NMOS + CCD

Functions

- Two CCD shift registers (for chrominance and luminance signals)
- CCD drive circuits
- CCD stage count switching circuit
- CCD signal adder
- Auto-bias circuit
- Sync tip clamping circuit (luminance signal)
- Center-bias circuit (chrominance signal)
- Sample-and-hold circuit
- PLL 4 × frequency multiplier
- fsc clock output circuit
- RD voltage generator

Features

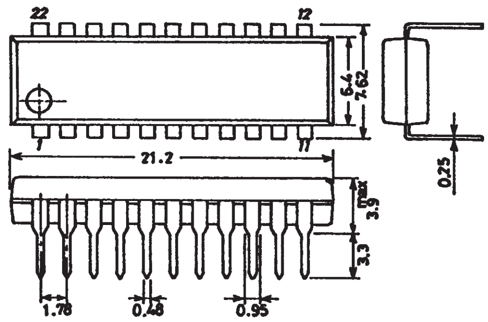
- 5 V single-voltage power supply
- Built-in PLL 4 × frequency multiplier circuit allows 4 fsc operation from an fsc (3.58 MHz) input.
- Control pin switchable to handle NTSC/M, PAL/GBI and PAL/M systems.
- Built-in chrominance signal crosstalk exclusion comb filter features high precision comb characteristics in an adjustment-free circuit.
- Built-in peripheral circuits allow applications to be constructed with a minimum number of external components.
- Positive-phase signal input/positive-phase signal output (luminance signal)

Package Dimensions

unit: mm

3059-DIP22S (375 mil)

[LC89971]

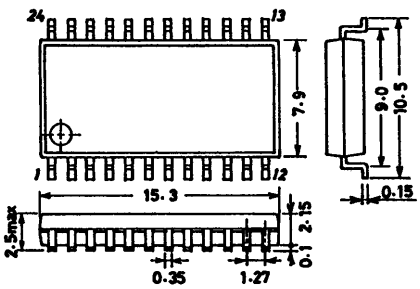


SANYO: DIP22S

unit: mm

3045B-MFP24

[LC89971M]



SANYO: MFP24

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.0	V
Allowable power dissipation	Pd max	LC89971	1200	mW
		LC89971M	600	mW
Operating temperature	Topr		–10 to +70	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Clock input amplitude	V_{CLK}		300	500	1000	mVp-p
Clock frequency	F_{CLK}	Sine wave	—	3.579545	—	MHz
Clock signal input amplitude	V_{IN-C}		—	350	500	mVp-p
Luminance signal input amplitude	V_{IN-Y}		—	400	572	mVp-p

Electrical Characteristics at V_{DD} = 5.0 V, Ta = 25°C, F_{CLK} = 3.579545 MHz, V_{CLK} = 500 mVp-p

Parameter	Symbol	Switch states				Conditions	min	typ	max	Unit
		SW1	SW2	SW3	SW4					
Supply current	I_{DD-1}	a	a	a	b	1	45	55	65	mA
	I_{DD-2}	a	b	a	b					
	I_{DD-3}	b	b	a	b					
Chrominance System Characteristics (with no Y-IN input)										
Pin voltage (input)	V_{INC-1}	a	a	a	b	2	2.0	2.4	2.8	V
	V_{INC-2}	a	b	a	b					
	V_{INC-3}	b	b	a	b					
Pin voltage (output)	V_{OUYC-1}	a	a	a	b		1.2	1.6	2.0	V
	V_{OUTC-2}	a	b	a	b					
	V_{OUTC-3}	b	b	a	b					
Voltage gain	G_{VC-1}	a	a	a	b	3	–2	0	+2	dB
	G_{VC-2}	a	b	a	b					
	G_{VC-3}	b	b	a	b					
Comb depth	C_{D-1}	a	a	a	b	4	—	–40	–35	dB
	C_{D-2}	a	b	a	b					
	C_{D-3}	b	b	a	b					
Linearity	L_{NC-1}	a	a	a	b	5	–0.3	0.0	+0.3	dB
	L_{NC-2}	a	b	a	b					
	L_{NC-3}	b	b	a	b					
Clock leakage (4 fsc)	L_{CK4C-1}	a	a	a	b	6	—	10	50	mVrms
	L_{CK4C-2}	a	b	a	b					
	L_{CK4C-3}	b	b	a	b					
Clock leakage (fsc)	L_{CK1C-1}	a	a	a	b		—	0.8	1.5	mVrms
	L_{CK1C-2}	a	b	a	b					
	L_{CK1C-3}	b	b	a	b					
Noise	N_{C-1}	a	a	a	b	7	—	0.5	2.0	mVrms
	N_{C-2}	a	b	a	b					
	N_{C-3}	b	b	a	b					
Output impedance	Z_{OC-1}	a	a	a	a, b	8	200	350	500	Ω
	Z_{OC-2}	a	b	a	a, b					
	Z_{OC-3}	b	b	a	a, b					
0 H delay time	T_{DC-1}	a	a	a	b	9	—	230	—	ns
	T_{DC-2}	a	b	a	b					
	T_{DC-3}	b	b	a	b					

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Switch states				Conditions	min	typ	max	Unit
		SW1	SW2	SW3	SW4					
Luminance System Characteristics (with no C-IN1 or C-IN2 input)										
Pin voltage (input)	V_{INY-1}	a	a	a	b	10	1.7	2.1	2.5	V
	V_{INY-2}	a	b	a	b					
	V_{INY-3}	b	b	a	b					
Pin voltage (output)	V_{OUTY-1}	a	a	a	b		0.8	1.2	1.6	V
	V_{OUTY-2}	a	b	a	b					
	V_{OUTY-3}	b	b	a	b					
Voltage gain	G_{VY-1}	a	a	a	b	11	–2	0	+2	dB
	G_{VY-2}	a	b	a	b					
	G_{VY-3}	b	b	a	b					
Frequency responce	G_{FY-1}	a	a	b	b	12	–2	0	+2	dB
	G_{FY-2}	a	b	b	b					
	G_{FY-3}	b	b	b	b					
Differential gain	D_{GY-1}	a	a	a	b	13	0	5	7	%
	D_{GY-2}	a	b	a	b					
	D_{GY-3}	b	b	a	b					
Differential phase	D_{PY-1}	a	a	a	b		0	5	7	deg
	D_{PY-2}	a	b	a	b					
	D_{PY-3}	b	b	a	b					
Linearity	L_{SY-1}	a	a	a	b	14	37	40	43	%
	L_{SY-2}	a	b	a	b					
	L_{SY-3}	b	b	a	b					
Clock leakage (4 fsc)	L_{CK4Y-1}	a	a	a	b	15	—	10	50	mVrms
	L_{CK4Y-2}	a	b	a	b					
	L_{CK4Y-3}	b	b	a	b					
Clock leakage (fsc)	L_{CK1Y-1}	a	a	a	b		—	0.8	1.5	mVrms
	L_{CK1Y-2}	a	b	a	b					
	L_{CK1Y-3}	b	b	a	b					
Noise	N_{Y-1}	a	a	a	b	16	—	0.5	2.0	mVrms
	N_{Y-2}	a	b	a	b					
	N_{Y-3}	b	b	a	b					
Output impedance	Z_{OY-1}	a	a	a	c, b	17	250	400	550	Ω
	Z_{OY-2}	a	b	a	c, b					
	Z_{OY-3}	b	b	a	c, b					
Delay time	T_{DY-1}	a	a	a	b	18	—	63.88	—	µs
	T_{DY-2}	a	b	a	b		—	63.46	—	
	T_{DY-3}	b	b	a	b		—	63.46	—	

Test Conditions

1. Supply current with no signal input.
2. C-OUT voltage (center bias voltage) with no signal input.
3. Measure the C-OUT output with 350 mVp-p sine wave signals input to C-IN1 and C-IN2.

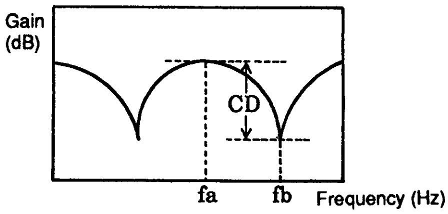
$$\text{GVC} = 20 \log \frac{\text{C-OUT output [mVp-p]}}{350 \text{ [mVp-p]}} \text{ [dB]}$$

Test frequencies

GVC-1 4.431395 MHz (PAL/GBI)
GVC-2 3.571628 MHz (PAL/M)
GVC-3 3.571628 MHz (NTSC/M)

4. Measure the comb depth from the C-OUT output with a 350 mVp-p sine wave signal of frequency fa input to C-IN1 and C-IN2 and with a frequency of fb input.

$$CD = 20 \log \frac{\text{C-OUT output with fb input [mVp-p]}}{\text{C-OUT output with fa input [mVp-p]}} \text{ [dB]}$$



Test frequencies

	fa	fb
CD-1	4.431395 MHz	4.435303 MHz (PAL/GBI)
CD-2	3.571628 MHz	3.575561 MHz (PAL/M)
CD-3	3.571628 MHz	3.575561 MHz (NTSC/M)

5. Measure the C-OUT output with a 200 mVp-p sine wave signal input to C-IN1 and C-IN2 and with 500 mVp-p sine wave signal input and calculate the difference in the gains.

$$LNC = 20 \log \left(\frac{\text{Output for a 500 mVp-p input [mVp-p]}}{\text{500 [mVp-p]}} \Big/ \frac{\text{Output for a 200 mVp-p input [mVp-p]}}{\text{200 [mVp-p]}} \right) \text{ [dB]}$$

Test frequencies

LNC-1 4.431395 MHz (PAL/GBI)
LNC-2 3.571628 MHz (PAL/M)
LNC-3 3.571628 MHz (NTSC/M)

6. Measure the 4 fsc (14.3 MHz) and fsc (3.58 MHz) components in the C-OUT output with no input.

7. Measure the noise in the C-OUT output with no input.
Measure the noise with a noise meter set up with a 200 kHz high-pass filter and a 5 MHz low-pass filter.

8. Let V1 be the C-OUT output with a 350 mVp-p sine wave input to C-IN1 and C-IN2 and SW3 set to a, and let V2 be the C-OUT output with SW3 set to b.

$$ZOC = \frac{\text{V2 [mVp-p]} - \text{V1 [mVp-p]}}{\text{V1 [mVp-p]}} \times 500 \text{ [}\Omega\text{]}$$

Test frequencies

ZOC-1 4.431395 MHz (PAL/GBI)
ZOC-2 3.571628 MHz (PAL/M)
ZOC-3 3.571628 MHz (NTSC/M)

9. The C-OUT output delay time with respect to inputs to C-IN1. (the CCD 2.5 bit delay)

10. Y-OUT voltage (clamp voltage) with no signal input.

11. Measure the Y-OUT output with a 200 kHz 400 mVp-p sine wave input to Y-IN.

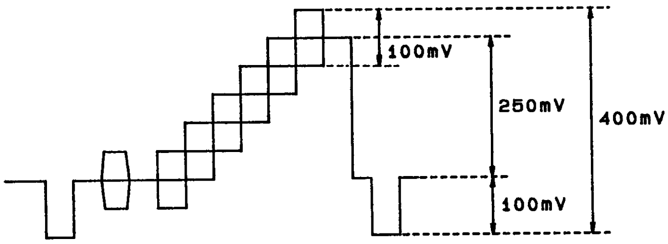
$$GVY = 20 \log \frac{\text{Y-OUT output [mVp-p]}}{\text{400 [mVp-p]}} \text{ [dB]}$$

12. Measure the Y-OUT output with a 200 kHz 200 mVp-p sine wave input to Y-IN and with a 3.3 MHz 200 mVp-p sine wave input.

$$GFY = 20 \log \frac{\text{Y-OUT output with a 3.5 MHz input [mVp-p]}}{\text{Y-OUT output with a 200 kHz input [mVp-p]}} \text{ [dB]}$$

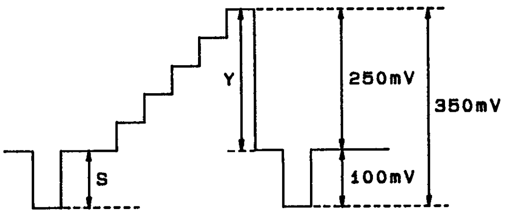
Note that V_{bias} should be adjusted so that the circuit is biased to the clamp level plus 250 mV.

13. Input a five-level step waveform (see the figure below) to Y-IN and measure the differential gain and differential phase in the Y-OUT output with a vector scope.



A03833

14. Input a five-level step waveform (see the figure below) to Y-IN and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.



A03834

$$LS = \frac{S\ [mV]}{Y\ [mV]} \times 100\ [\%]$$

15. Measure the 4 fsc (14.3 MHz) and fsc (3.58 MHz) components in the Y-OUT output with no input.

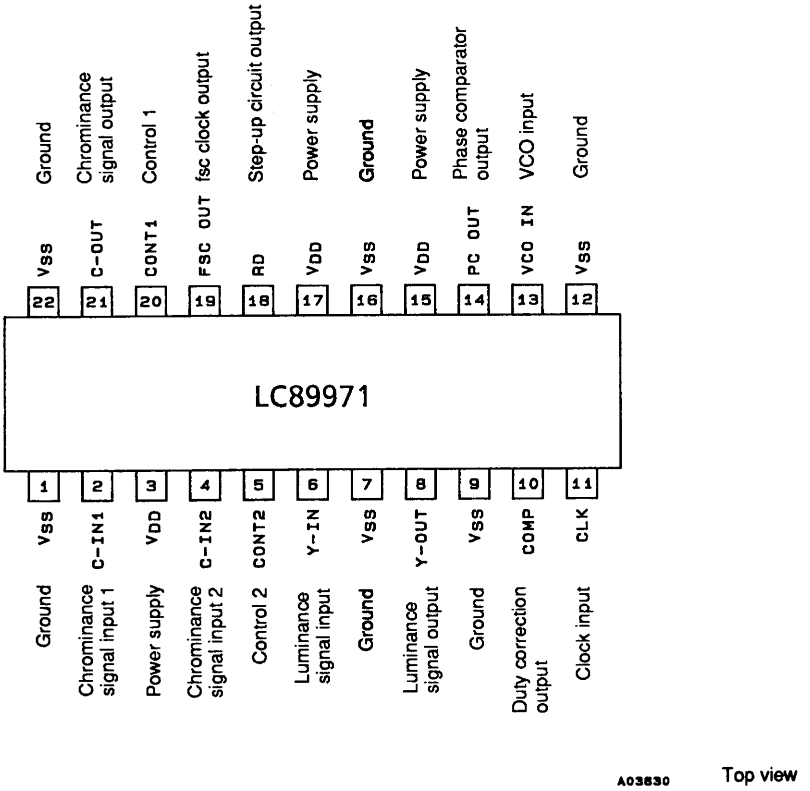
16. Measure the noise in the Y-OUT output with no input.
Measure the noise with a noise meter set up with a 200 kHz high-pass filter, a 4.2 MHz low-pass filter, and a 3.58 MHz trap filter.

17. Let V1 be the Y-OUT output with a 200 kHz 400 mVp-p sine wave input and SW4 set to c, and let V2 be the C-OUT output with SW4 set to b.

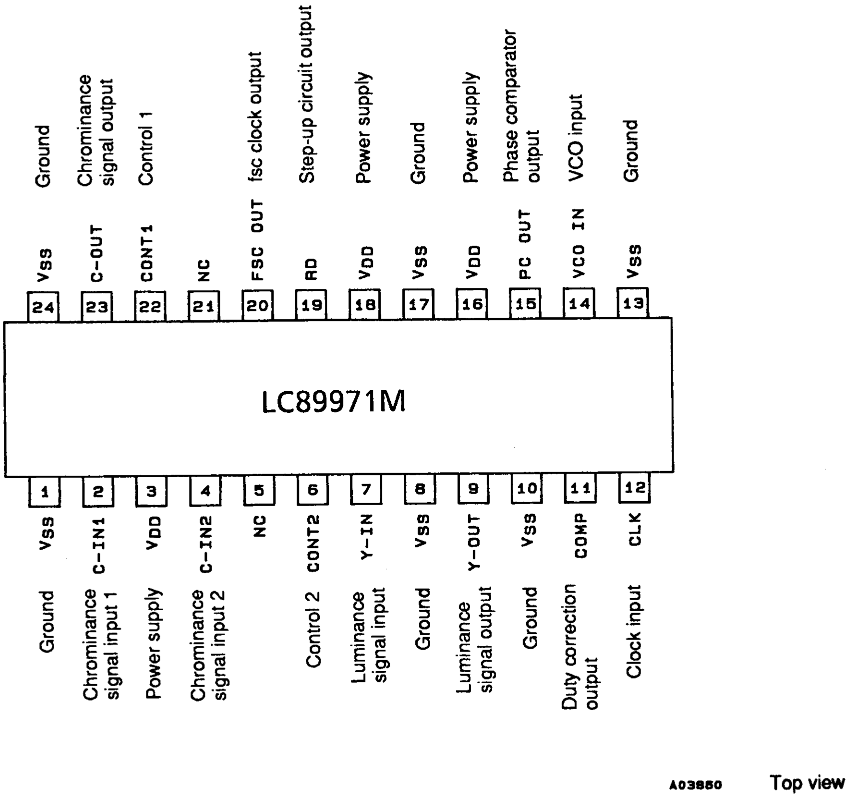
$$ZOY = \frac{V2\ [mVp\text{-}p] - V1\ [mVp\text{-}p]}{V1\ [mVp\text{-}p]} \times 500\ [\Omega]$$

18. The Y-OUT delay time with respect to Y-IN

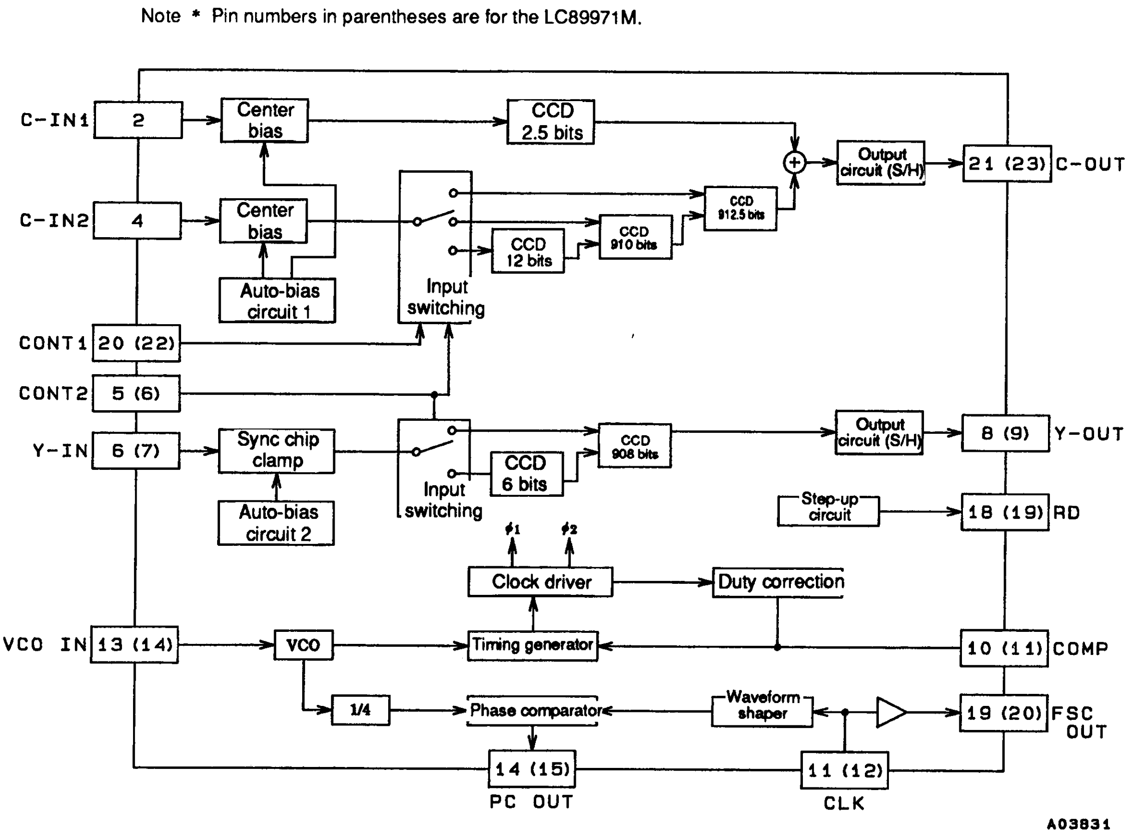
Pin Assignment [LC89971]



Pin Assignment [LC89971M]



Block Diagram



Control Pin Function

CONT1	CONT2	Mode (representative example)	Chrominance signal delay (CCD bits)	Luminance signal delay (CCD bits)
Low	Low	PAL/GBI	2 H (1834.5) + 0 H (2.5)	1 H (914)
Low	High	PAL/M	2 H (1822.5) + 0 H (2.5)	1 H (908)
High	Low	—	—	—
High	High	NTSC/M	1 H (912.5) + 0 H (2.5)	1 H (908)

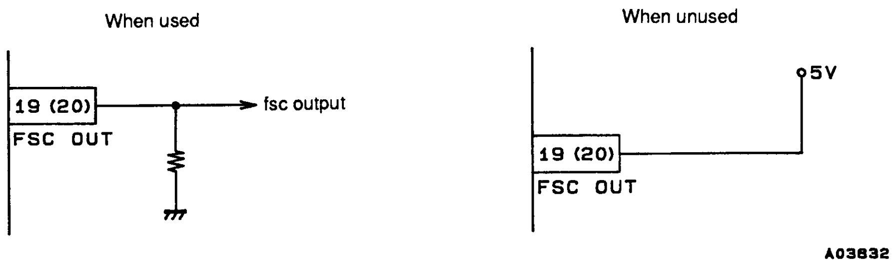
Switching Voltage Levels

Low/high	Symbol	min	typ	max	Unit
Low	V_L	–0.3	0.0	0.5	V
High	V_H	2.0	5.0	6.0	V

Note: Since the control pin has a built-in pull-down resistor (≈ 70 kΩ), the pin will be set to the low state if left open.

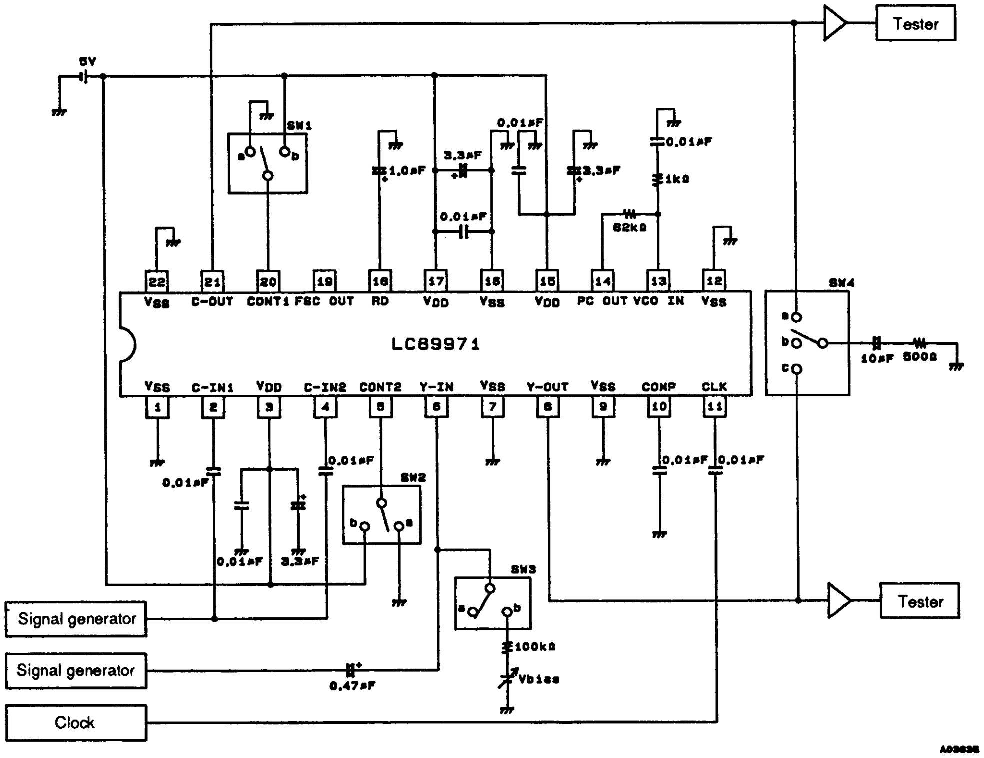
FSC OUT Pin Function

This pin provides a buffer output for the clock signal input to the CLK pin.



Note: Since this pin has a built-in pull-up resistor, the pin voltage will go to the supply voltage and output will cease if left open.

Test Circuit [LC89971]



Test Circuit [LC89971M]