



Integrated Device Technology, Inc.

SUBSYSTEMS "FLEXI-PAK™" FAMILY PRELIMINARY 32K x 16/32K x 16 IDT7M7005 CMOS SRAM/EEPROM MODULE

FEATURES:

- High-density CMOS module with SRAM and EEPROM memory on-board
- Member of the Subsystems "Flexi-Pak" Family of interchangeable modules with equivalent pin-outs
- Footprint compatible module upgrades to the next higher density with relative ease
- Fast access times:
 - 15ns (max.) commercial SRAM
 - 20ns (max.) military SRAM
 - 75ns (max.) commercial EEPROM
 - 95ns (max.) military EEPROM
- Low power CMOS operation
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Offered in a 66-pin HIP (Hex In-line Package), occupying only 1 sq. inch of board space
- Single 5V (±10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Please consult the factory regarding the number of Erase/Write Cycles per Byte Minimum available on the module

DESCRIPTION:

The IDT7M7005 is a high-speed, high-density CMOS module with both SRAM & EEPROM memory on-board. It is constructed on a multi-layer, co-fired ceramic substrate using 32K x 8 SRAM or EEPROM components in leadless chip carriers.

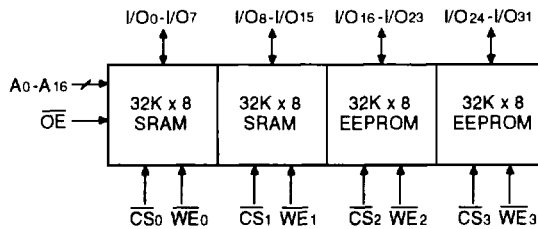
These modules are part of the IDT Subsystems "Flexi-Pak" Family. This family of SRAM/EEPROM/EPROM memory modules support applications requiring stand alone static or programmable memory or those applications needing a combination of both. All of these module configurations have equivalent pin-outs, making them "plug-in compatible" with each other, suitable for a wide range of applications.

The IDT7M7005 is available with SRAM access times as fast as 15ns over the commercial temperature range and 20ns over the military temperature range and EEPROM access times as fast as 75ns over the commercial temperature range and 95ns over the military temperature range.

These modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and fits the SRAM/EEPROM memory into 1 sq. inch of board space.

All military IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2826 drw 01

7

Flexi-Pak is a Trademark of Integrated Device Technology, Inc

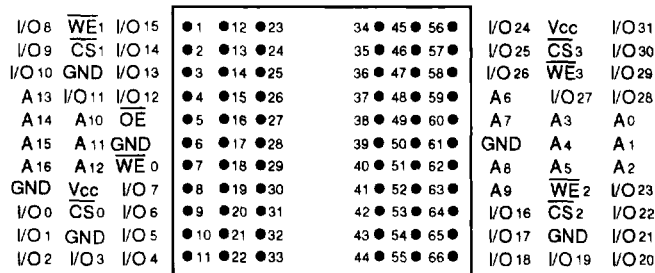
MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1992

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DSC-7079/2

PIN CONFIGURATIONS (1)



2826 drw 02

**HIP
TOP VIEW**

NOTE:

For the IDT7M7005 (32K x 16/32K x 16) version, pins 6 and 7 are no connects.

PIN NAMES

Name	Description
I/O 0-31	Data Inputs/Outputs
A 0-16	Address Inputs
\overline{WE} 0-1	RAM Write Enables
\overline{WE} 2-3	EEPROM Write Enables
\overline{CS} 0-1	RAM Chip Selects
\overline{CS} 2-3	EEPROM Chip Selects
\overline{OE}	Output Enable
VCC	Power Supply
GND	Ground

2826 tbl 01

**RECOMMENDED OPERATING
TEMPERATURE AND VOLTAGE SUPPLY**

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

2826 tbl 03

TRUTH TABLE (1)

Mode	\overline{CS}	\overline{OE}	\overline{WE}	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Write	L	note 1	L	DIN	Active
Read	L	H	H	High Z	Active

2826 tbl 02

NOTE:

1. For the SRAM array \overline{OE} = X (don't care); however, for the EEPROM array \overline{OE} = H (high).

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN (1)	Input Capacitance (Data, \overline{CS} , \overline{WE})	VIN = 0V	12	pF
CIN (2)	Input Capacitance (Address, \overline{OE})	VIN = 0V	50	pF
COU	Output Capacitance	VOU = 0V	15	pF

2826 tbl 04

NOTE:

1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

2826 tbl 05

NOTE:

- V_{IL} (min.) = -3.0V for pulse width less than 20ns.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
V _{TERM}	Terminal Voltage with Respect to Ground	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I _{OUT}	DC Output Current	50	50	mA

2826 tbl 06

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max. ⁽¹⁾	Max. ⁽²⁾	Unit
I _L	Input Leakage Current (Address, \overline{OE})	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	30	40	μA
I _L	Input Leakage Current (Data, \overline{CS} , \overline{WE})	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	10	10	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., \overline{CS} = V _{IH} , V _{OUT} = GND to V _{CC}	—	10	10	μA
I _{CC}	Dynamic Operating Current	V _{CC} = Max., \overline{CS} ≤ V _{IL} , f = f _{MAX} , Output Open	—	560	600	mA
I _{SB}	Standby Supply Current	V _{CC} = Max., \overline{CS} ≥ V _{IH} , f = f _{MAX} , Output Open	—	46	146	mA
I _{SB1}	Full Standby Supply Current	\overline{CS} ≥ V _{CC} - 0.2V V _{IN} > V _{CC} - 0.2V or < 0.2V	—	46	46	mA
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 8mA (3)	—	0.4	0.4	V
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = -4mA (3)	2.4	—	—	V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 6mA (4)	—	0.45	0.45	V
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = -4mA (4)	2.4	—	—	V

NOTES:

- For T_A = 0°C to +70°C versions only.
- For T_A = -55°C to +125°C versions only.
- For I/Os (0-15).
- For I/Os (16-31).

2826 tbl 07



AC TEST CONDITIONS (EEPROM)

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2826 tbl 08

AC ELECTRICAL CHARACTERISTICS (EEPROM)

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameters	-75		-95		-125		-150		-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	75	—	95	—	125	—	150	—	200	—	ns
t _{AA}	Address Access Time	—	75	—	95	—	125	—	150	—	200	ns
t _{ACS}	Chip Select Access Time	—	75	—	95	—	125	—	150	—	200	ns
t _{OE}	Output Enable to Output Valid	—	40	—	50	—	55	—	70	—	80	ns
t _{CHZ} ⁽¹⁾	Chip Select to Output in High Z	0	40	0	50	0	55	0	55	0	60	ns
t _{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
WRITE CYCLE												
t _{WC}	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
t _{AH}	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
t _{AS}	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
t _{WP}	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
t _{CS}	\overline{CS} Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t _{CH}	\overline{CS} Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t _{DS}	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
PAGE MODE WRITE CYCLE												
t _{WC}	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
t _{AH}	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
t _{AS}	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
t _{DS}	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
t _{BLC}	Byte Load Cycle Time	0.2	200	0.2	200	0.2	200	0.2	200	0.2	200	μs
t _{WPH}	Write Pulse Width High	55	—	55	—	55	—	55	—	55	—	ns
DATA POLLING CYCLE												
t _{DH} ⁽¹⁾	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ms
t _{OEH} ⁽¹⁾	Output Enable Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t _{OE} ⁽¹⁾	Output Enable to Output Delay	—	100	—	100	—	100	—	100	—	100	ns
t _{WR} ⁽¹⁾	Write Recovery Time	2	—	2	—	2	—	2	—	2	—	ns

2826 tbl 09

NOTE:

1. This parameter is guaranteed by design but not tested

AC TEST CONDITIONS (SRAM)

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

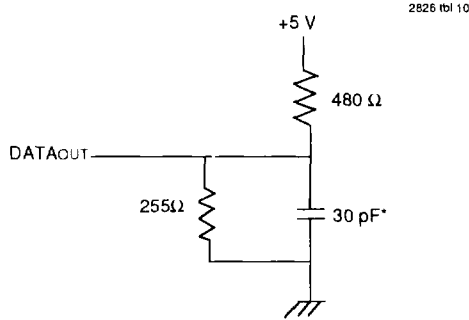


Figure 1. Output Load 2826 drw 03

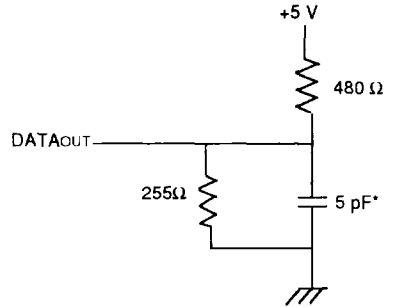


Figure 2. Output Load (for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ) 2826 drw 04

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-15 ⁽²⁾		-17 ⁽²⁾		-20 ⁽²⁾		-25		-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
tRC	Read Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
tAA	Address Access Time	—	15	—	17	—	20	—	25	—	30	ns
tACS	Chip Select Access Time	—	15	—	17	—	20	—	25	—	30	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	12	—	13	—	15	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low Z	0	—	0	—	0	—	2	—	2	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	12	—	15	ns
tOHZ ⁽¹⁾	Output Disable to Output in High Z	—	6	—	7	—	7	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
WRITE CYCLE												
tWC	Write Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
tCW	Chip Select to End of Write	12	—	13	—	15	—	20	—	25	—	ns
tAW	Address Valid to End of Write	12	—	13	—	15	—	20	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	13	—	15	—	20	—	23	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High Z	—	6	—	8	—	9	—	12	—	13	ns
tDW	Data to Write Time Overlap	8	—	8	—	9	—	13	—	15	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	3	—	3	—	ns
tOW ⁽¹⁾	Output Active from End of Write	0	—	0	—	0	—	5	—	5	—	ns

NOTES:

1. This parameter is guaranteed by design, but not tested.
2. Preliminary specification only.

2711 tbl 09

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-35		-40		-50		-60 (Mil. Only)		-70 (Mil. Only)		-85 (Mil. Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	35	—	40	—	50	—	60	—	70	—	85	—	ns
t _{AA}	Address Access Time	—	35	—	40	—	50	—	60	—	70	—	85	ns
t _{ACS}	Chip Select Access Time	—	35	—	40	—	50	—	60	—	70	—	85	ns
t _{CLZ} ⁽¹⁾	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t _{OE}	Output Enable to Output Valid	—	20	—	25	—	30	—	30	—	35	—	40	ns
t _{OLZ} ⁽¹⁾	Output Enable to Output in Low Z	2	—	5	—	5	—	5	—	5	—	5	—	ns
t _{CHZ} ⁽¹⁾	Chip Deselect to Output in High Z	—	17	—	20	—	20	—	25	—	30	—	35	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output in High Z	—	15	—	20	—	20	—	25	—	30	—	35	ns
t _{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE														
t _{WC}	Write Cycle Time	35	—	40	—	50	—	60	—	70	—	85	—	ns
t _{CW}	Chip Select to End of Write	30	—	35	—	45	—	55	—	65	—	80	—	ns
t _{AW}	Address Valid to End of Write	30	—	35	—	45	—	55	—	65	—	80	—	ns
t _{AS}	Address Set-up Time	0	—	2	—	2	—	5	—	5	—	5	—	ns
t _{WP}	Write Pulse Width	25	—	30	—	40	—	45	—	45	—	50	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t _{WHZ} ⁽¹⁾	Write Enable to Output in High Z	—	17	—	20	—	20	—	25	—	30	—	35	ns
t _{DW}	Data to Write Time Overlap	16	—	16	—	25	—	30	—	30	—	35	—	ns
t _{DH}	Data Hold from Write Time	3	—	3	—	5	—	5	—	5	—	5	—	ns
t _{OW} ⁽¹⁾	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

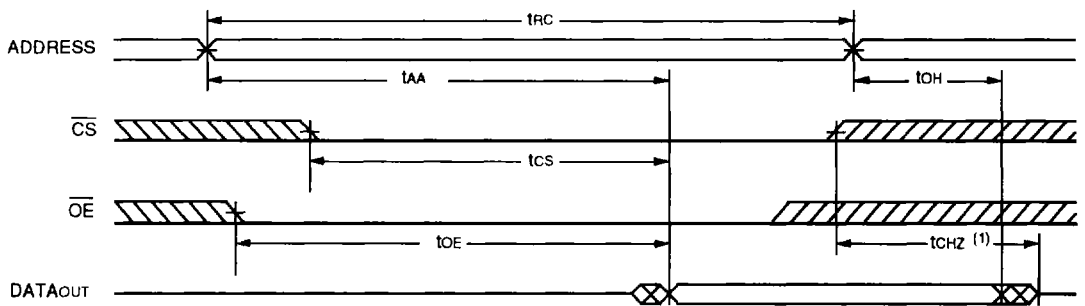
2711 tbl 10

NOTE:

1. This parameter is guaranteed by design, but not tested.

EEPROM TIMING WAVEFORMS

TIMING WAVEFORM OF READ CYCLE⁽¹⁾

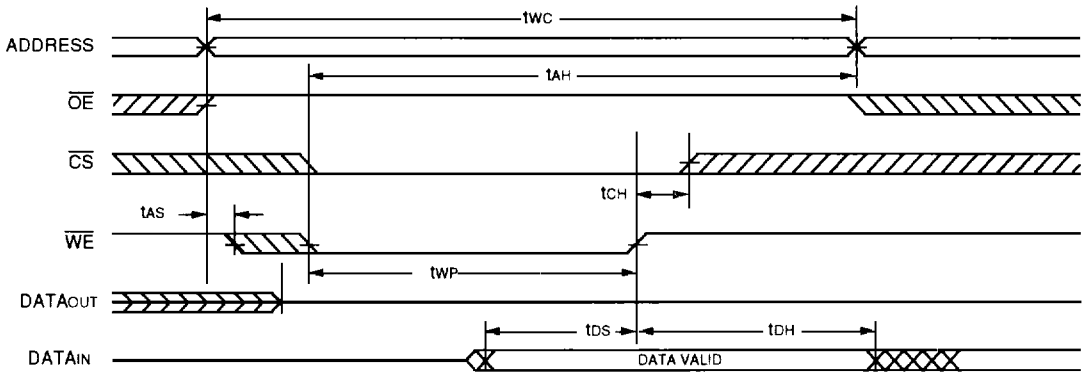


2826 drw 05

NOTES:

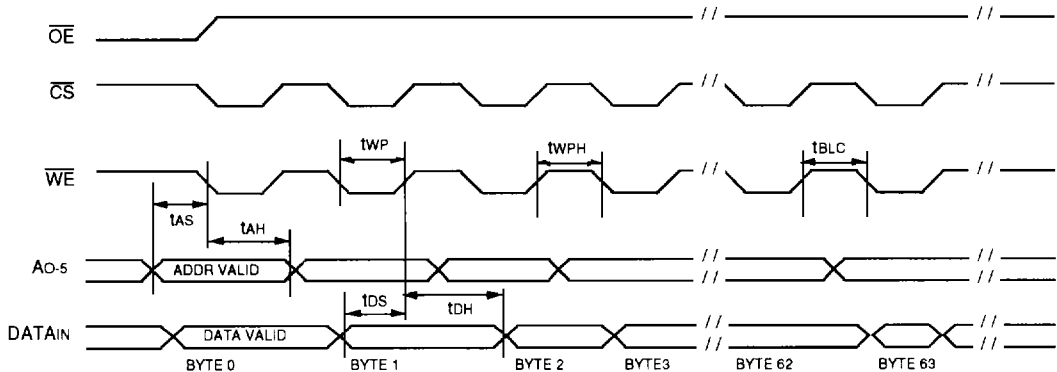
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)



TIMING WAVEFORM OF PAGE MODE WRITE CYCLE (1)

2826 drw 06

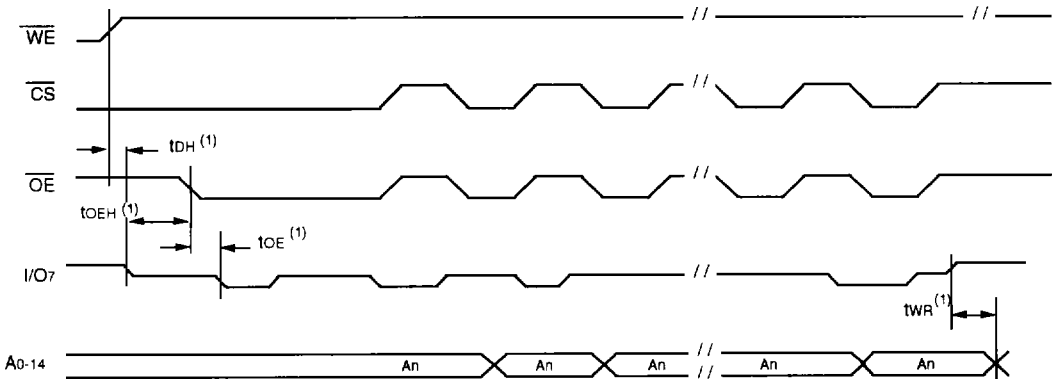


2826 drw 07

NOTE:

- A6 through A14 must specify the page address during each High to Low transitions of \overline{WE} (or \overline{CS}). \overline{OE} must be High only when \overline{WE} and \overline{CS} are both Low.

TIMING WAVEFORM OF DATA POLLING CYCLE



2826 drw 08

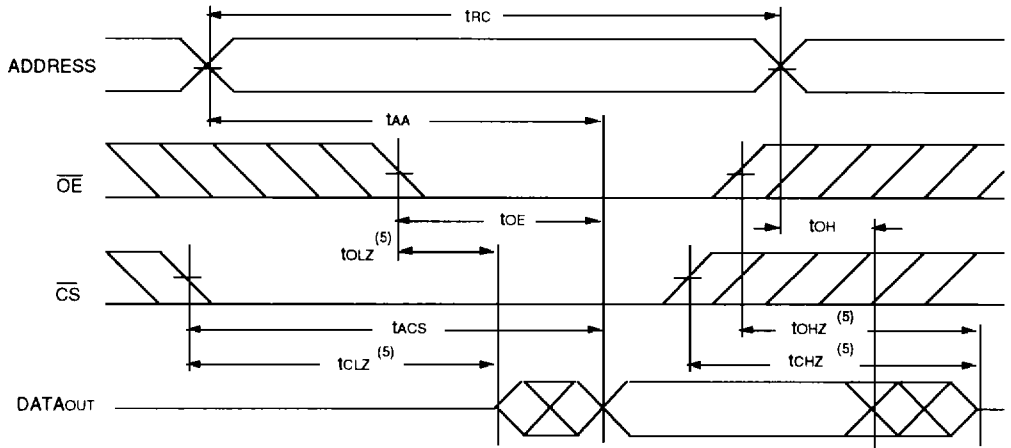
NOTES:

- This parameter is guaranteed by design but not tested.
- A6 through A14 must specify the page address during each High to Low transitions of \overline{WE} (or \overline{CS}). \overline{OE} must be High only when \overline{WE} and \overline{CS} are both Low.

7

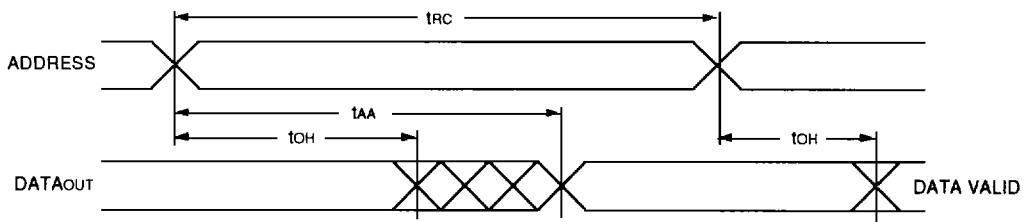
SRAM TIMING WAVEFORMS

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



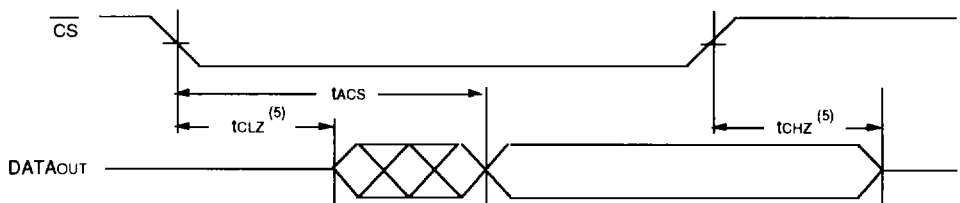
2826 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



2826 drw 10

TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)

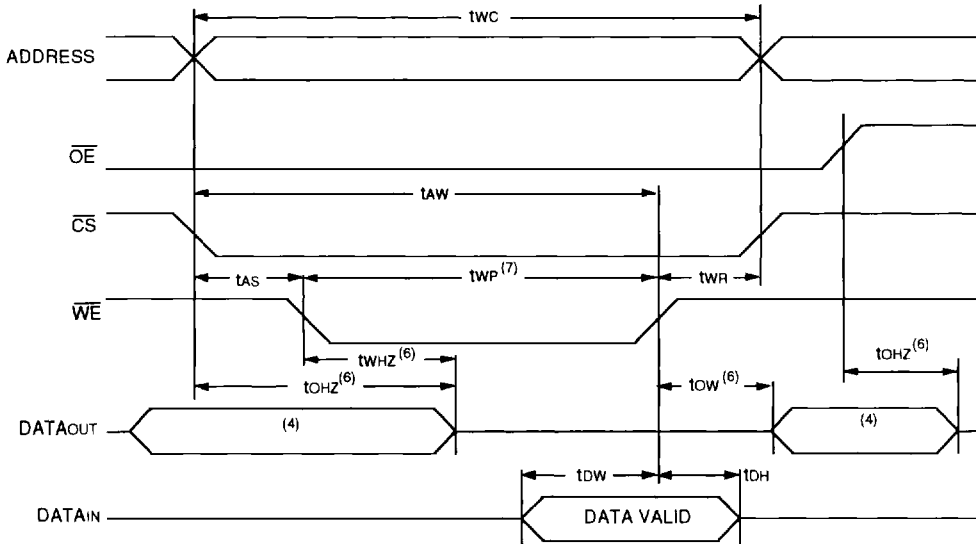


2826 drw 11

NOTES:

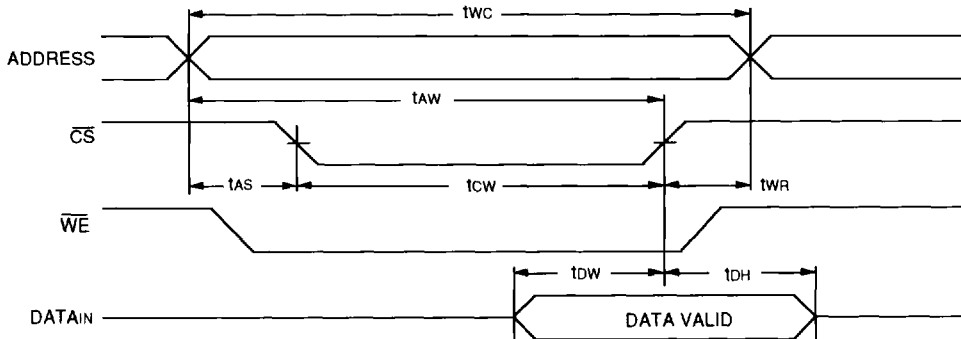
1. WE is high for Read Cycle.
2. Device is continuously selected, CS = VIL.
3. Address valid prior to or coincident with CS transition low.
4. OE = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)^(1, 2, 3, 7)



2826 drw 12

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED)^(1, 2, 3, 5)

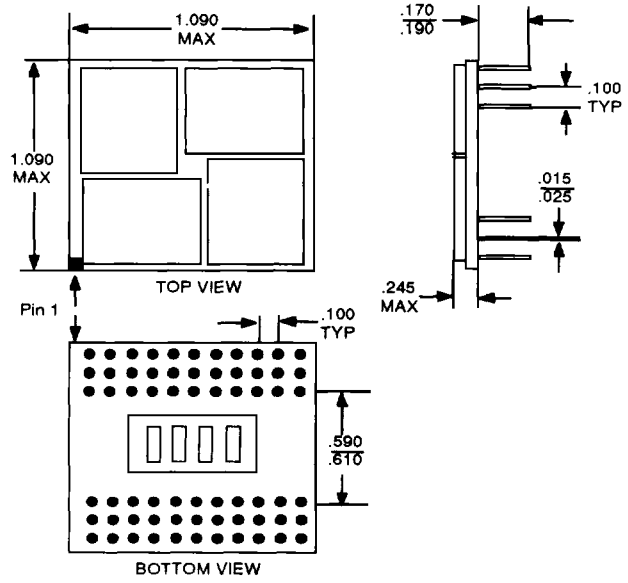


2826 drw 13

NOTES:

1. \overline{WE} or \overline{CS} must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the \overline{CS} Low transition occurs simultaneously with or after the \overline{WE} Low transition, the outputs remain in a high impedance state.
6. Transition is measured $\pm 200mV$ from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If \overline{OE} is low during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{OW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If \overline{OE} is high during an \overline{WE} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

PACKAGE DIMENSIONS



2826 drw 14