FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-10168-2E

MEMORY
CMOS 1M x 16 BIT FAST PAGE MODE DYNAMIC RAM

MB81V16160A -60/-70

CMOS 1,048,576 x 16BIT Fast Page Mode Dynamic RAM

■ DESCRIPTION

The Fujitsu MB81V16160A is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 16-bit increments. The MB81V16160A features a "fast page" mode of operation whereby high-speed random access of up to 256-bits of data within the same row can be selected. The MB81V16160A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81V16160A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81V16160A is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81V16160A are not critical and all inputs are TTL compatible.

■ ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to + 4.6	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	–0.5 to + 4.6	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Operating Temperature	T_{OPE}	0 to 70	°C
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

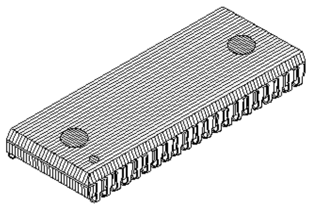
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PRODUCT LINE & FEATURES

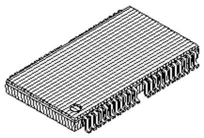
Parameter		MB81V16160A –60	MB81V16160A –70
$\overline{\text{RAS}}$ Access Time		60ns max.	70ns max.
Random Cycle Time		110ns min.	130ns min.
Address Access Time		30ns max.	35ns max.
$\overline{\text{CAS}}$ Access Time		15ns max.	17ns max.
Fast Page Mode Cycle Time		40ns min.	45ns min.
Low Power Dissipation	Operating current	324mW max.	288mW max.
	Standby current	7.2mW max. (TTL level) / 3.6mW max. (CMOS level)	

- 1,048,576 words × 16 bit organization
- Silicon gate, CMOS, Advanced Capacitor Cell
- All input and output are LVTTL compatible
- 4096 refresh cycles every 65.6ms
- 1$\overline{\text{WE}}$ / 2$\overline{\text{CAS}}$
- Self refresh function
- Early write or $\overline{\text{OE}}$ controlled write capability
- RAS only, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

PACKAGE



Plastic SOJ Package
(LCC-42P-M01)



Plastic TSOP Packages
(FPT-50P-M06)
(Normal Bend)
(Reverse Bend)

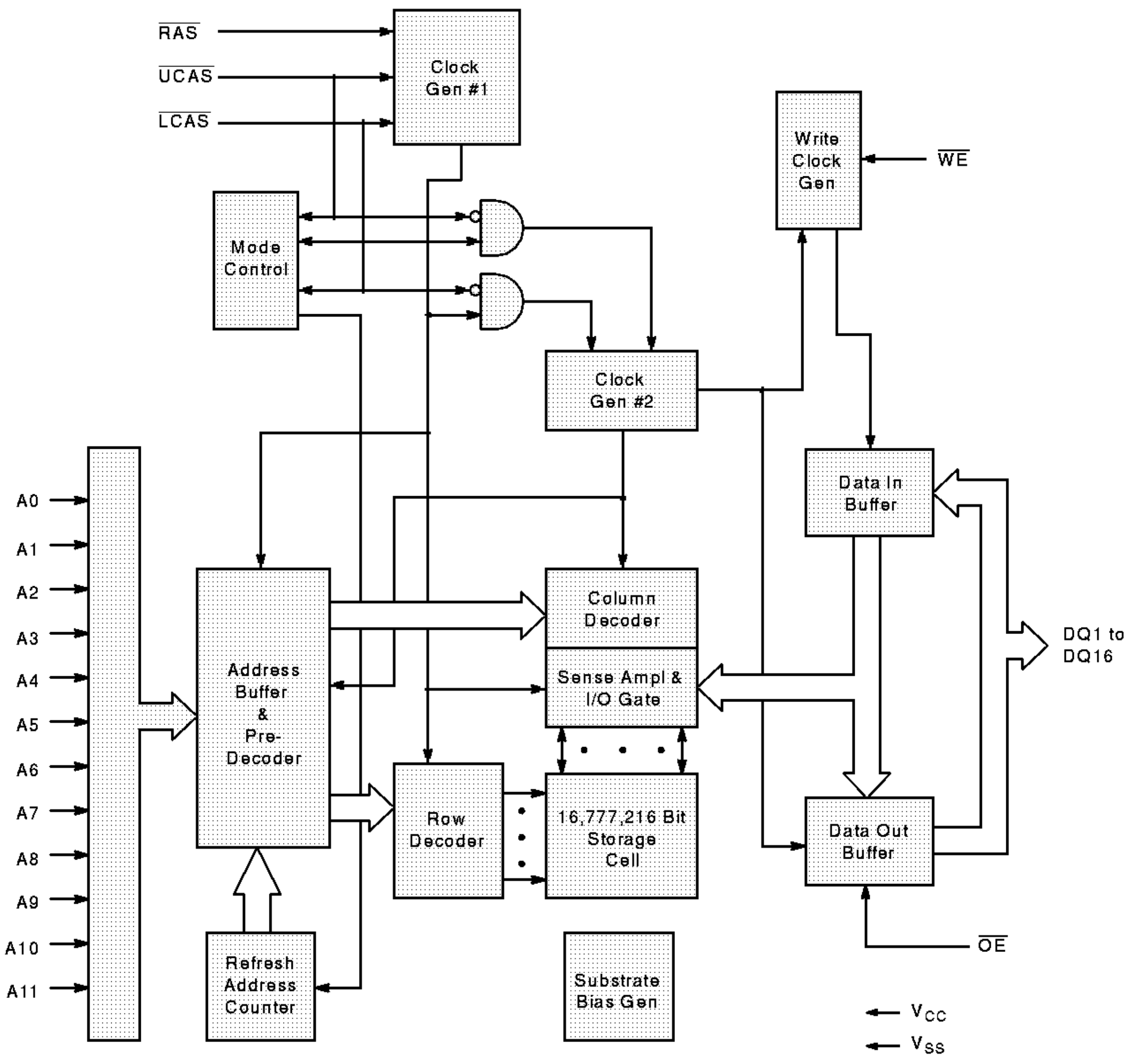
Package and Ordering Information

– 42-pin plastic (400mil) SOJ, order as MB81V16160A-XXPJ

– 50 pin plastic (400mil) TSOP-II with normal bend leads, order as MB81V16160A-XXPFTN

– 50-pin plastic (400mil) TSOP-II with reverse bend leads, order as MB81V16160A-XXPFTR

Fig. 1 – MB81V16160A DYNAMIC RAM – BLOCK DIAGRAM

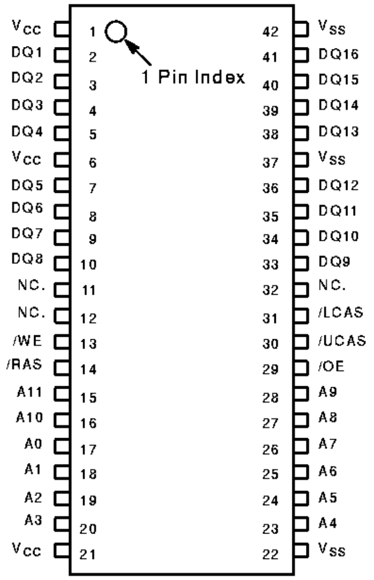


CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Max	Unit
Input Capacitance, A0 to A11	C_{IN1}	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	5	pF
Input/Output Capacitance, DQ1 to DQ16	C_{DQ}	7	pF

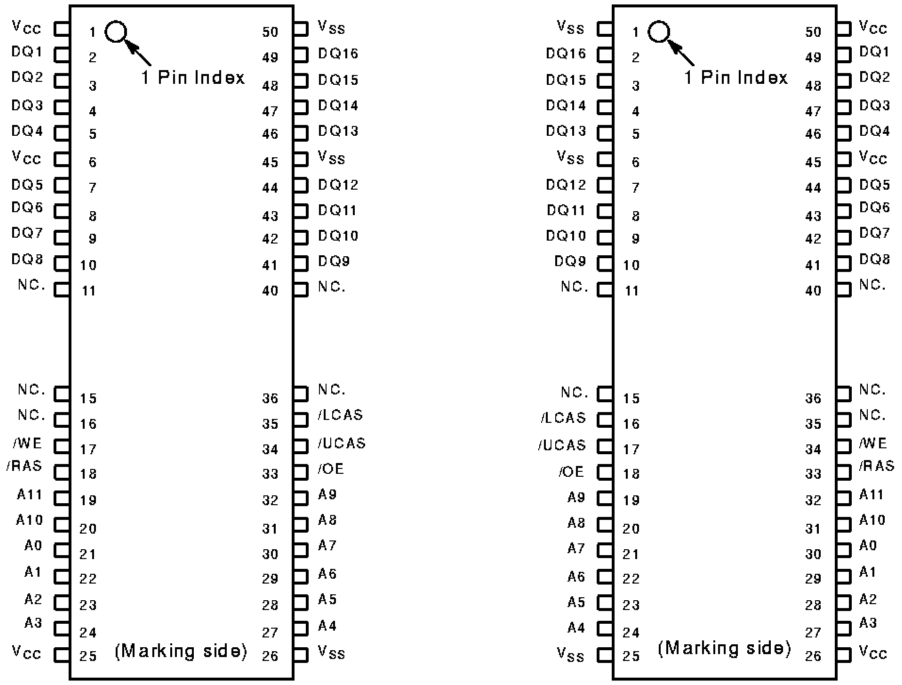
PIN ASSIGNMENTS AND DESCRIPTIONS

42-Pin SOJ
(TOP VIEW)



Designator	Function
A0 to A11	Address inputs. row : A0 to A11 column : A0 to A7 refresh : A0 to A11
$\overline{\text{RAS}}$	Row address strobe.
$\overline{\text{LCAS}}$	Lower column address strobe.
$\overline{\text{UCAS}}$	Upper column address strobe.
$\overline{\text{WE}}$	Write enable.
$\overline{\text{OE}}$	Output enable.
DQ1 to DQ16	Data Input/Output
V_{CC}	+3.3 volt power supply.
V_{SS}	Circuit ground

50-Pin TSOP
(TOP VIEW)


<Normal Bend> <Reverse Bend>

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp.
Supply Voltage	$\boxed{1}$	V_{CC}	3.0	3.3	3.6	V	0°C to +70°C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	$\boxed{1}$	V_{IH}	2.0	—	V_{CC}+0.3	V	
Input High Voltage, all inputs/outputs*	$\boxed{1}$	V_{IL}	−0.3	—	0.8	V	

* : Undershoots of up to −2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any sixteen of 16,777,216 cell addresses in the memory matrix. Since only twelve address bits (A0 to A11) are available, the column and row inputs are separately strobed by $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and $\overline{\text{RAS}}$ as shown in Figure 1. First, twelve row address bits are input on pins A0–through–A11 and latched with the row address strobe ($\overline{\text{RAS}}$) then, eight column address bits are input and latched with the column address strobe ($\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$). Both row and column addresses must be stable on or before the falling edges of $\overline{\text{RAS}}$ and $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min) + t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{\text{WE}}$. When $\overline{\text{WE}}$ is active Low, a write cycle is initiated; when $\overline{\text{WE}}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways–an early write cycle, an $\overline{\text{OE}}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{\text{WE}}$ or $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data of DQ1-DQ8 is strobed by LCAS and DQ9-DQ16 is strobed by $\overline{\text{UCAS}}$ and the setup/hold times are referenced to each $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ because WE goes Low before $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$. in a delayed write or a read-modify-write cycle, WE goes Low after $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$; thus, input data is strobed by WE and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

t_{RAC} : from the falling edge of $\overline{\text{RAS}}$ when t_{RCD} (max) is satisfied.

t_{CAC} : from the falling edge of $\overline{\text{LCAS}}$ (for DQ1–DQ8) $\overline{\text{UCAS}}$ (for DQ9–DQ16) when t_{RCD} is greater than t_{RCD} (max).

t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max).

t_{OEA} : from the falling edge of $\overline{\text{OE}}$ when $\overline{\text{OE}}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.

The data remains valid until either $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$ or $\overline{\text{OE}}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{\text{RAS}}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 256x16-bits can be accessed and, when multiple MB81V16160As are used, $\overline{\text{CAS}}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Parameter		Notes	Symbol	Conditions	Value Min	Value Typ	Value Max	Unit
Output high voltage		1	V_{OH}	$I_{OH} = -2.0mA$	2.4	—	—	V
Output low voltage		1	V_{OL}	$I_{OL} = +2.0mA$	—	—	0.4	
Input leakage current (any input)			$I_{I(L)}$	$0V \leq V_{IN} \leq 3.6V$; $3.0V \leq V_{CC} \leq 3.6V$; $V_{SS} = 0V$; All other pins not under test = 0V	−10	—	10	µA
Output leakage current			$I_{DO(L)}$	$0V \leq V_{OUT} \leq 3.6V$; Data out disabled	−10	—	10	
Operating current (Average power supply current)	MB81V16160A-60	2	I_{CC1}	$\overline{RAS}$ & $\overline{LCAS}$, $\overline{UCAS}$ cycling; t_{RC} = min	—	—	90	mA
	MB81V16160A-70						80	
Standby current (Power supply current)	TTL level		I_{CC2}	$\overline{RAS} = \overline{LCAS}, \overline{UCAS} = V_{IH}$	—	—	2.0	mA
	CMOS level			$\overline{RAS} = \overline{LCAS}, \overline{UCAS} \geq V_{CC}-0.2V$			1.0	
Refresh current #1 (Average power supply current)	MB81V16160A-60	2	I_{CC3}	$\overline{LCAS}$, $\overline{UCAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min	—	—	90	mA
	MB81V16160A-70						80	
Fast Page Mode Current	MB81V16160A-60	2	I_{CC4}	$\overline{RAS} = V_{IL}$, $\overline{LCAS}$, $\overline{UCAS}$ cycling; t_{PC} = min	—	—	90	mA
	MB81V16160A-70						80	
Refresh current #2 (Average power supply current)	MB81V16160A-60	2	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	90	mA
	MB81V16160A-70						80	
Refresh current #3 (Average power supply current)	MB81V16160A-60 MB81V16160A-70		I_{CC9}	$\overline{RAS}$ = VIL, $\overline{CAS}$ = VIL Self refresh ; t_{RASS} = min.	—	—	1000	µA

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3,4,5

No.	Parameter	Notes	Symbol	MB81V16160A-60		MB81V16160A-70		Unit
				Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	65.6	—	65.6	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	130	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	174	—	ns
4	Access Time from $\overline{\text{RAS}}$	6,9	t_{RAC}	—	60	—	70	ns
5	Access Time from $\overline{\text{CAS}}$	7,9	t_{CAC}	—	15	—	17	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	ns
7	Output Hold Time		t_{OH}	3	—	3	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	10	t_{OFF}	—	15	—	17	ns
10	Transition Time		t_{T}	3	50	3	50	ns
11	$\overline{\text{RAS}}$ Precharge Time		t_{RP}	40	—	50	—	ns
12	$\overline{\text{RAS}}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
13	$\overline{\text{RAS}}$ Hold Time		t_{RSH}	15	—	17	—	ns
14	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t_{CRP}	0	—	0	—	ns
15	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	11,12	t_{RCD}	20	45	20	53	ns
16	$\overline{\text{CAS}}$ Pulse Width		t_{CAS}	15	—	17	—	ns
17	$\overline{\text{CAS}}$ Hold Time		t_{CSH}	60	—	70	—	ns
18	$\overline{\text{CAS}}$ Precharge Time (Normal)	19	t_{CPN}	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	ns
23	Column Address Hold Time from $\overline{\text{RAS}}$		t_{AR}	35	—	35	—	ns
24	$\overline{\text{RAS}}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	ns
25	Column Address to $\overline{\text{RAS}}$ Lead Time		t_{RAL}	30	—	35	—	ns
26	Column Address to $\overline{\text{CAS}}$ Lead Time		t_{CAL}	30	—	35	—	ns
27	Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	14	t_{RRH}	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	14	t_{RCH}	0	—	0	—	ns
30	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	ns
31	Write Command Hold Time		t_{WCH}	15	—	15	—	ns
32	Write Hold Time from $\overline{\text{RAS}}$		t_{WCR}	35	—	35	—	ns
33	$\overline{\text{WE}}$ Pulse Width		t_{WP}	15	—	15	—	ns
34	Write Command to $\overline{\text{RAS}}$ Lead Time		t_{RWL}	15	—	17	—	ns
35	Write Command to $\overline{\text{CAS}}$ Lead Time		t_{CWL}	15	—	17	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3,4,5

No.	Parameter	Notes	Symbol	MB81V16160A-60		MB81V16160A-70		Unit
				Min	Max	Min	Max	
36	DIN Set Up Time		t_{DS}	0	—	0	—	ns
37	DIN Hold Time		t_{DH}	15	—	15	—	ns
38	Data Hold Time from RAS		t_{DHR}	35	—	35	—	ns
39	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	20	t_{RWD}	80	—	92	—	ns
40	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	20	t_{CWD}	35	—	39	—	ns
41	Column Address to $\overline{\text{WE}}$ Delay Time	20	t_{AWD}	50	—	57	—	ns
42	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh cycles)		t_{RPC}	5	—	5	—	ns
43	$\overline{\text{CAS}}$ Set Up Time for $\overline{\text{CAS}}$-before-RAS Refresh		t_{CSR}	0	—	0	—	ns
44	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh		t_{CHR}	10	—	12	—	ns
45	Access Time from $\overline{\text{OE}}$	9	t_{OEA}	—	15	—	17	ns
46	Output Buffer Turn Off Delay from $\overline{\text{OE}}$	10	t_{OEZ}	—	15	—	17	ns
47	$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	ns
48	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$	16	t_{OEH}	5	—	5	—	ns
49	$\overline{\text{OE}}$ to Data In Delay Time		t_{OED}	15	—	17	—	ns
50	$\overline{\text{CAS}}$ to Data In Delay Time		t_{CDD}	15	—	17	—	ns
51	DIN to $\overline{\text{CAS}}$ Delay Time	17	t_{DZC}	0	—	0	—	ns
52	DIN to $\overline{\text{OE}}$ Delay Time	17	t_{DZO}	0	—	0	—	ns
60	Fast Page Mode $\overline{\text{RAS}}$ Pulse width		t_{RASP}	—	100000	—	100000	ns
61	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	ns
62	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	80	—	89	—	ns
63	Access Time from $\overline{\text{CAS}}$ Precharge	9,18	t_{CPA}	—	35	—	40	ns
64	Fast Page Mode $\overline{\text{CAS}}$ Precharge Time		t_{CP}	10	—	10	—	ns
65	Fast Page Mode $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge		t_{RHCP}	35	—	40	—	ns
66	Fast Page Mode $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time		t_{CPWD}	55	—	62	—	ns

Notes:

1. Referenced to V_{SS}.
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.

   I_{CC} depends on the number of address change as $\overline{\text{RAS}} = V_{IL}$ $\overline{\text{UCAS}}=V_{IH}$, $\overline{\text{LCAS}}=V_{IH}$ and $V_{IL} > -0.3\text{V}$.

   I_{CC1}, I_{CC3} I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{\text{RAS}} = V_{IL}$ and $\overline{\text{UCAS}} = V_{IH}$, $\overline{\text{LCAS}} = V_{IH}$.

   I_{CC2} is specified during $\overline{\text{RAS}} = V_{IH}$ and $V_{IL} > -0.3\text{V}$.
3. An initial pause ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$) of 200μs is required after power-up followed by any eight $\overline{\text{RAS}}$–only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
4. AC characteristics assume $t_T = 5\text{ns}$.
5. Input voltage levels are 0V and 3.0V, and input reference levels are V_{IH}(min) and V_{IL}(max) for measuring timing of input signals. Also, the transition time (t_T) is measured between V_{IH}(min) and V_{IL}(max).

   The output reference levels are $V_{OH}=2.0\text{V}$ and $V_{OL}=0.8\text{V}$.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig.2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to one TTL loads and 100pF.
10. t_{OFF} and t_{OEZ} are specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access tome is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min).
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
19. Assumes that $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh.
20. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high impedance state through out the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{OUT} pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.

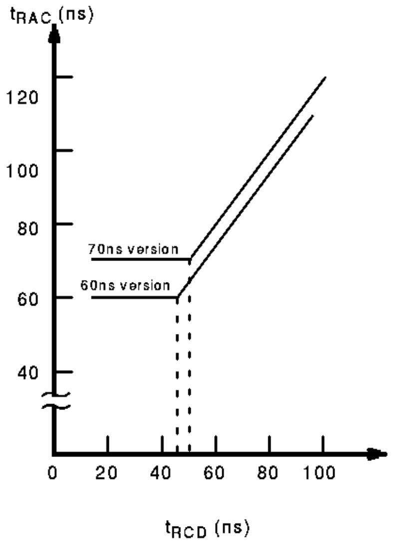


Fig. 2 – t_{RAC} vs. t_{RCD}

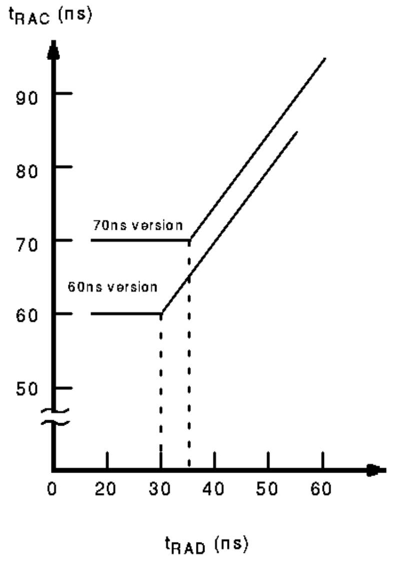


Fig. 3 – t_{RAC} vs. t_{RAD}

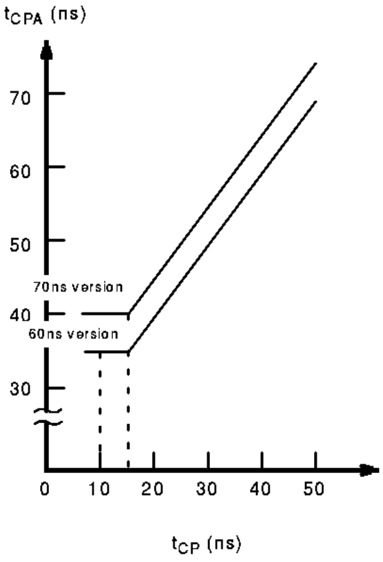


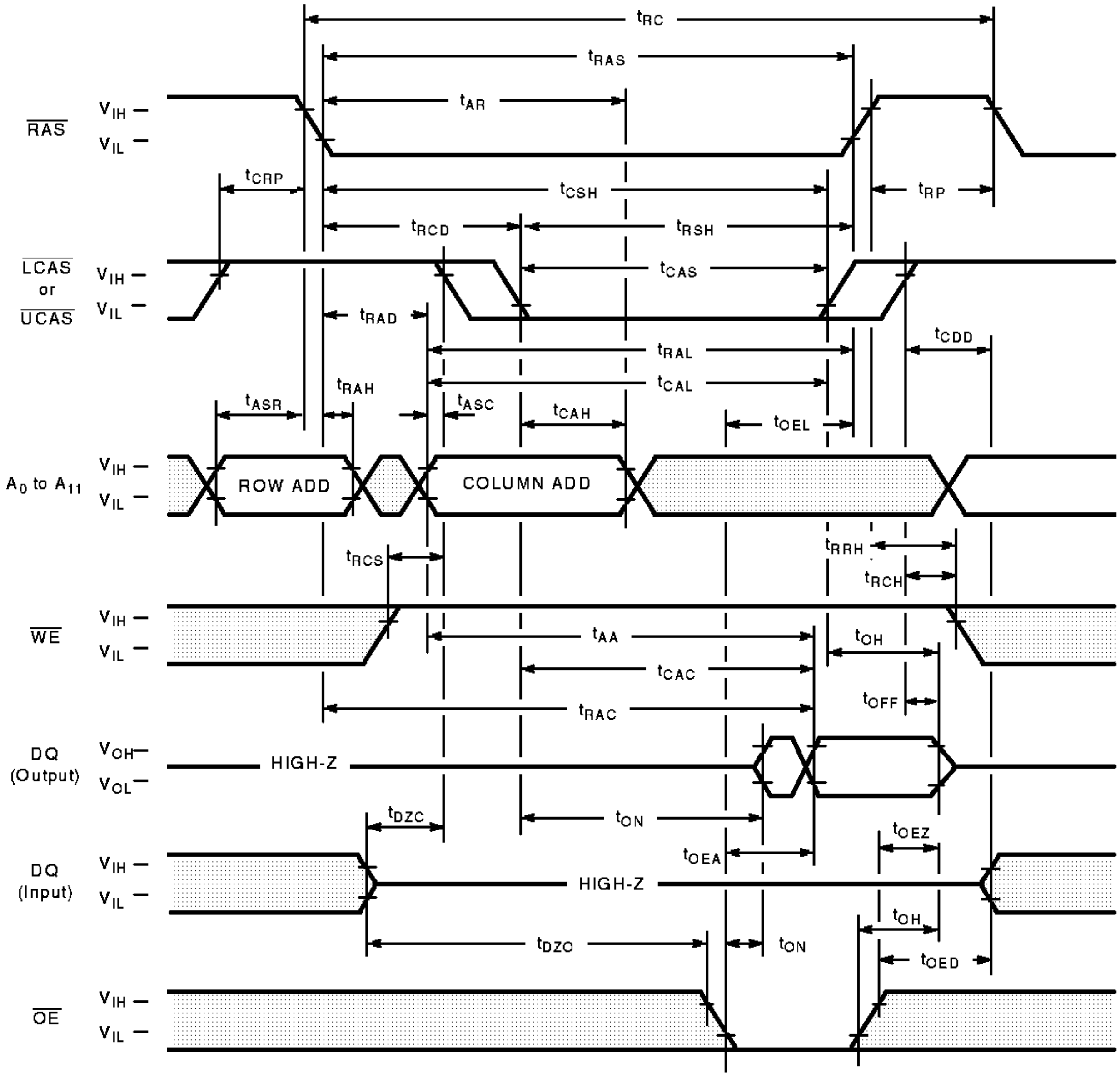
Fig. 4 – t_{CPA} vs. t_{CP}

FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address		Input/Output Data				Reflesh	Note
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	DQ1 to DQ8		DQ9 to DQ16			
								Input	Output	Input	Output		
Standby	H	H	H	X	X	–	–	–	High-Z	–	High-Z	–	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	–	Valid High-Z Valid	–	High-Z Valid Valid	Yes.*	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid – Valid	High-Z	– Valid Valid	High-Z	Yes.*	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L H L	H L L	H →L	L →H	Valid	Valid	Valid – Valid	Valid High-Z Valid	– Valid Valid	High-Z Valid Valid	Yes.*	
$\overline{RAS}$-only Refresh Cycle	L	H	H	X	X	Valid	–	–	High-Z	–	High-Z	Yes.	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	L	X	X	–	–	–	High-Z	–	High-Z	Yes.	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H →L	L H L	H L L	H →X	L	–	–	–	Valid High-Z Valid	–	High-Z Valid Valid	Yes.	Previous data is kept

X; "H" or "L"
*; It is impossible in Fast Page Mode.

Fig. 5 – READ CYCLE



▨ “H” or “L”

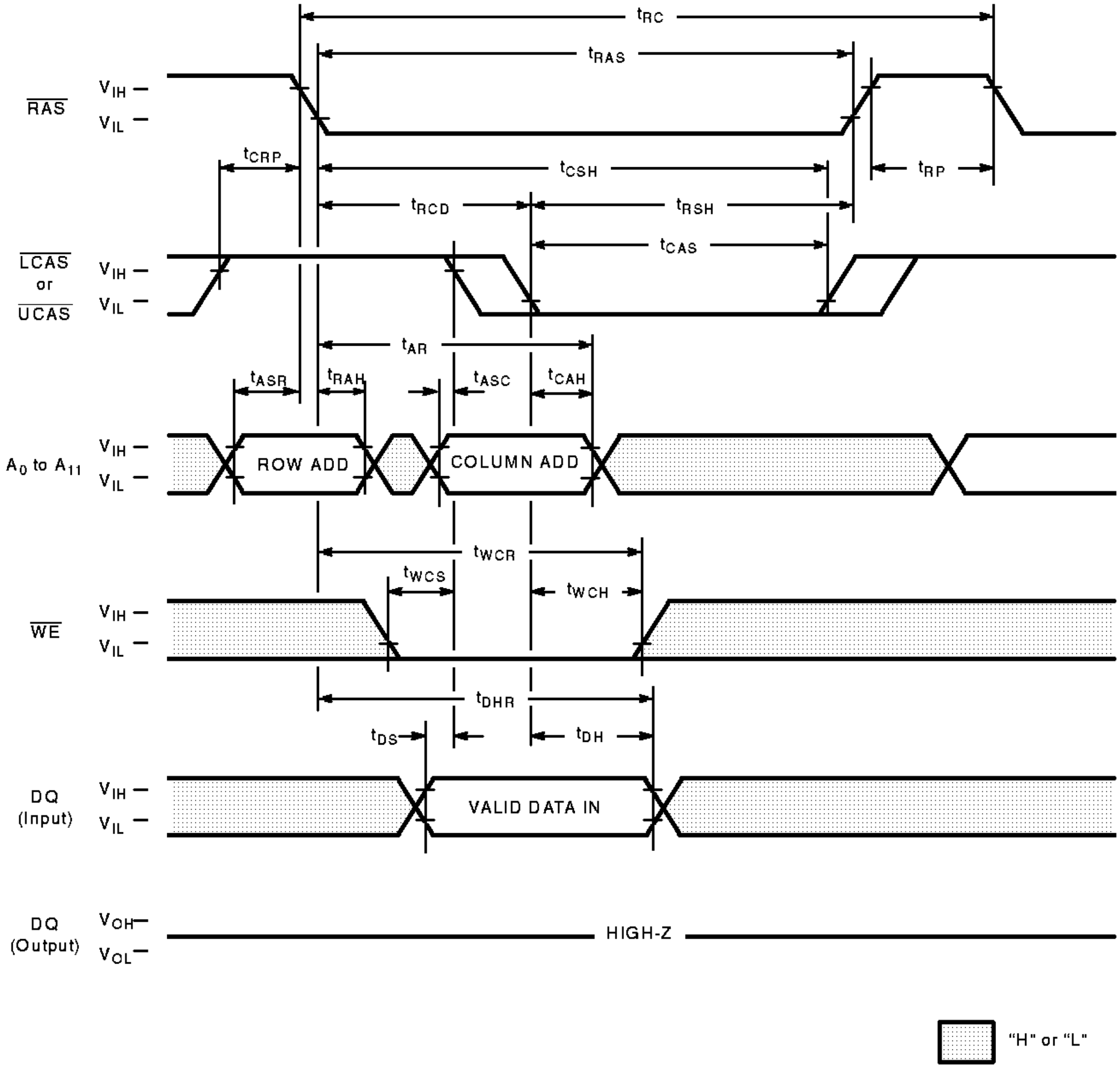
DESCRIPTION

To implement a read operation, a valid address is latched by the $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. $\overline{LCAS}$ controls the input/output data on DQ1–DQ8 pins, $\overline{UCAS}$ controls one on DQ8–DQ16 pins. The access time is determined by RAS(t_{RAC}), $\overline{LCAS}/\overline{UCAS}$($t_{CAC}$), $\overline{OE}$(t_{OEA}) or column addresses (t_{AA}) under the following conditions:

If $t_{RCD} > t_{RCD}$(max), access time = t_{CAC}.
If $t_{RAD} > t_{RAD}$(max), access time = t_{AA}
If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}(whichever occurs later), access time = t_{OEA}.

However, if either $\overline{LCAS}/\overline{UCAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

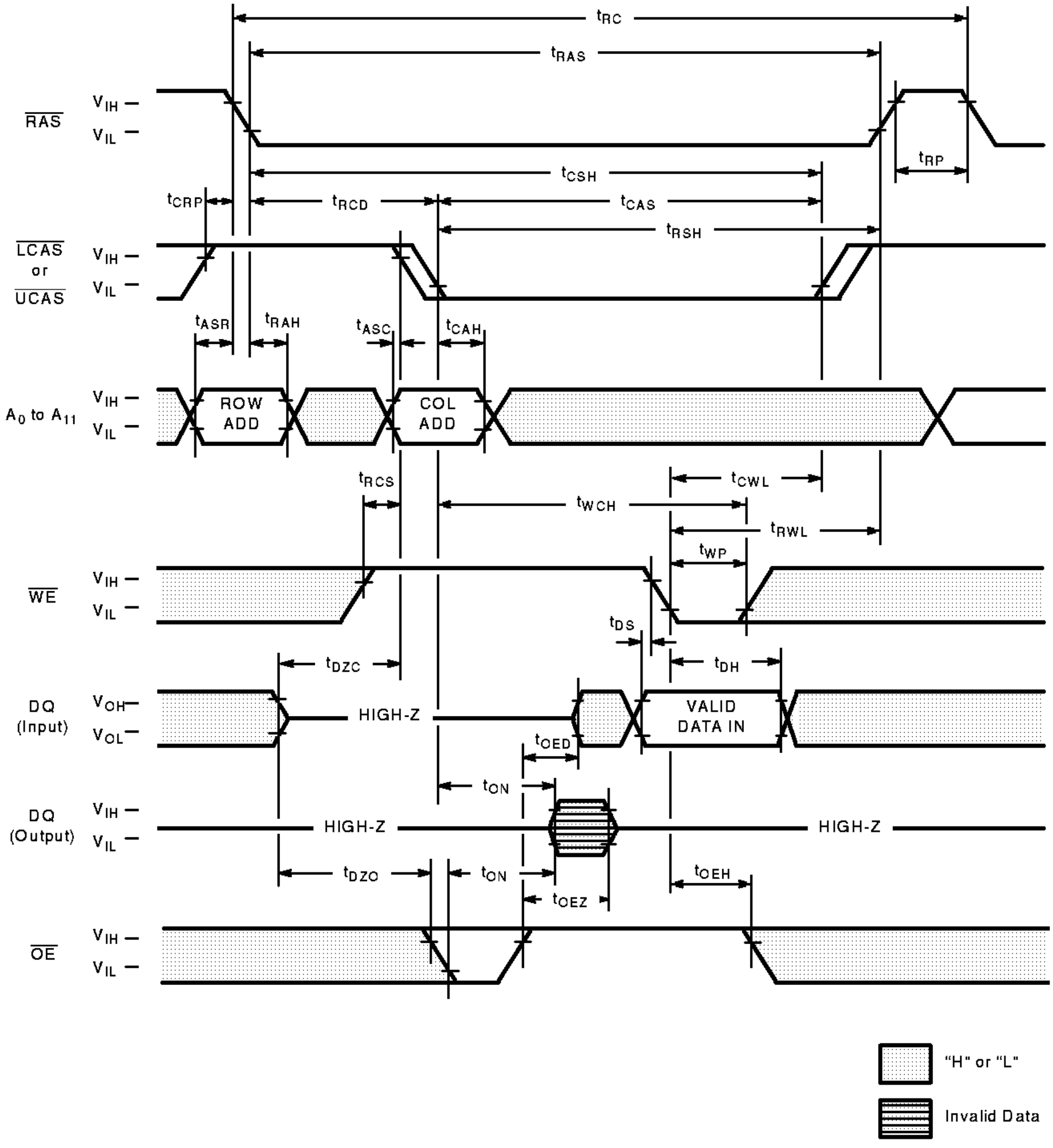
Fig. 6 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is an "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, delayed write, or read-modify-write. During all write cycles, timing parameters t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins are latched with the falling edge of $\overline{LCAS}$ or $\overline{UCAS}$ and written into memory.

Fig. 7 – DELAYED WRITE CYCLE



DESCRIPTION

In the delayed write cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

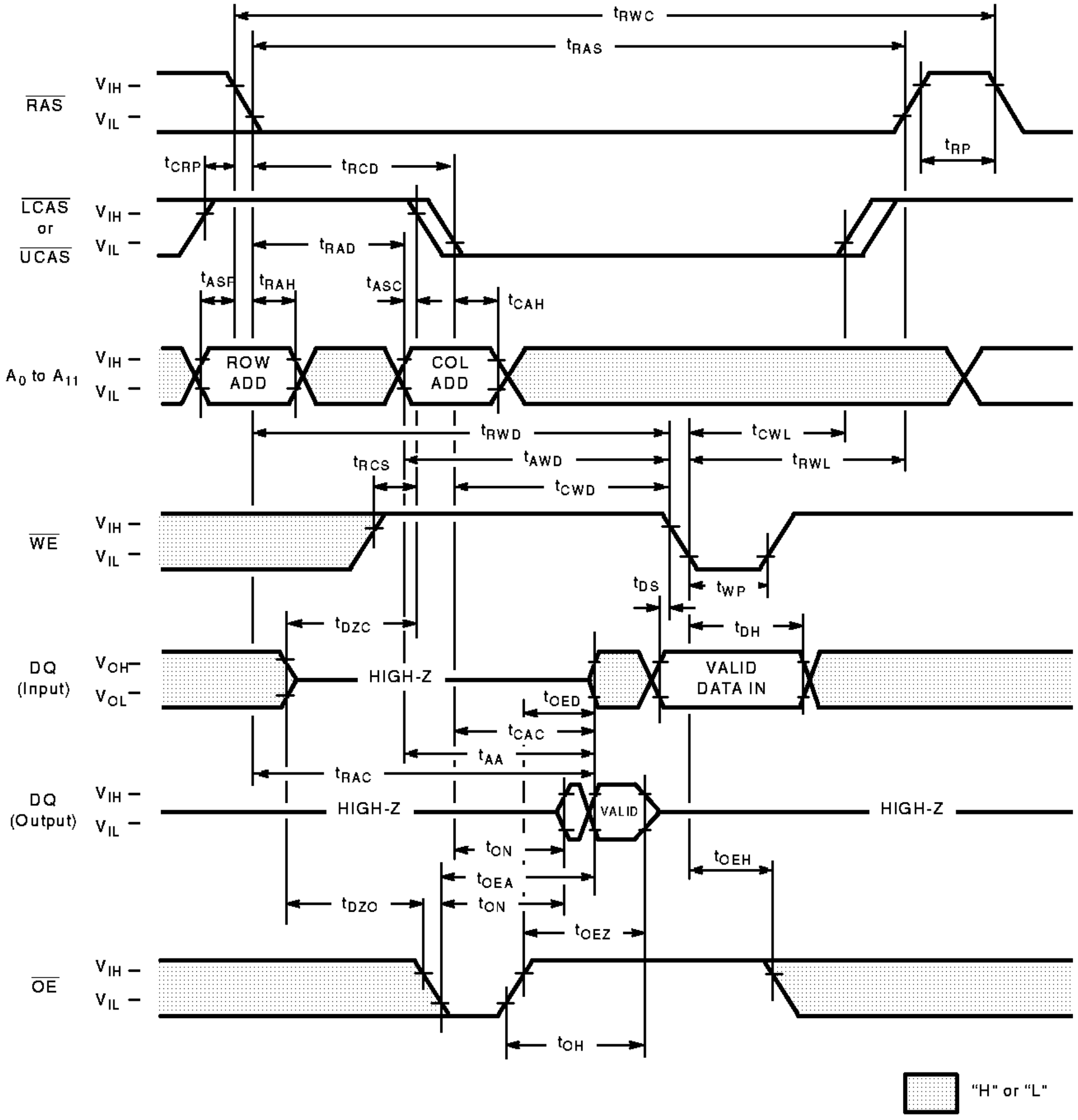
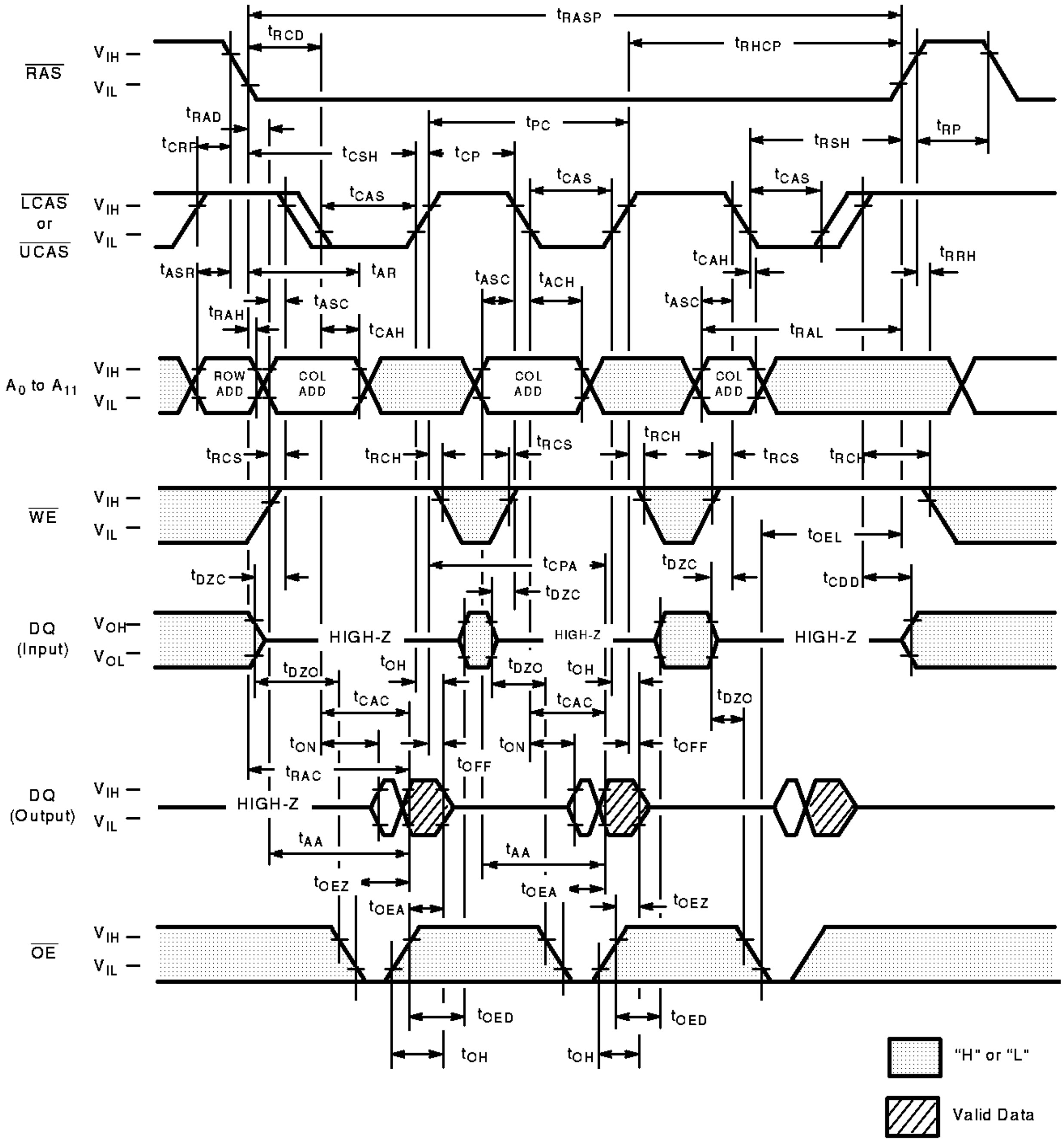


Fig. 8 – READ-MODIFY-WRITE-CYCLE

DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

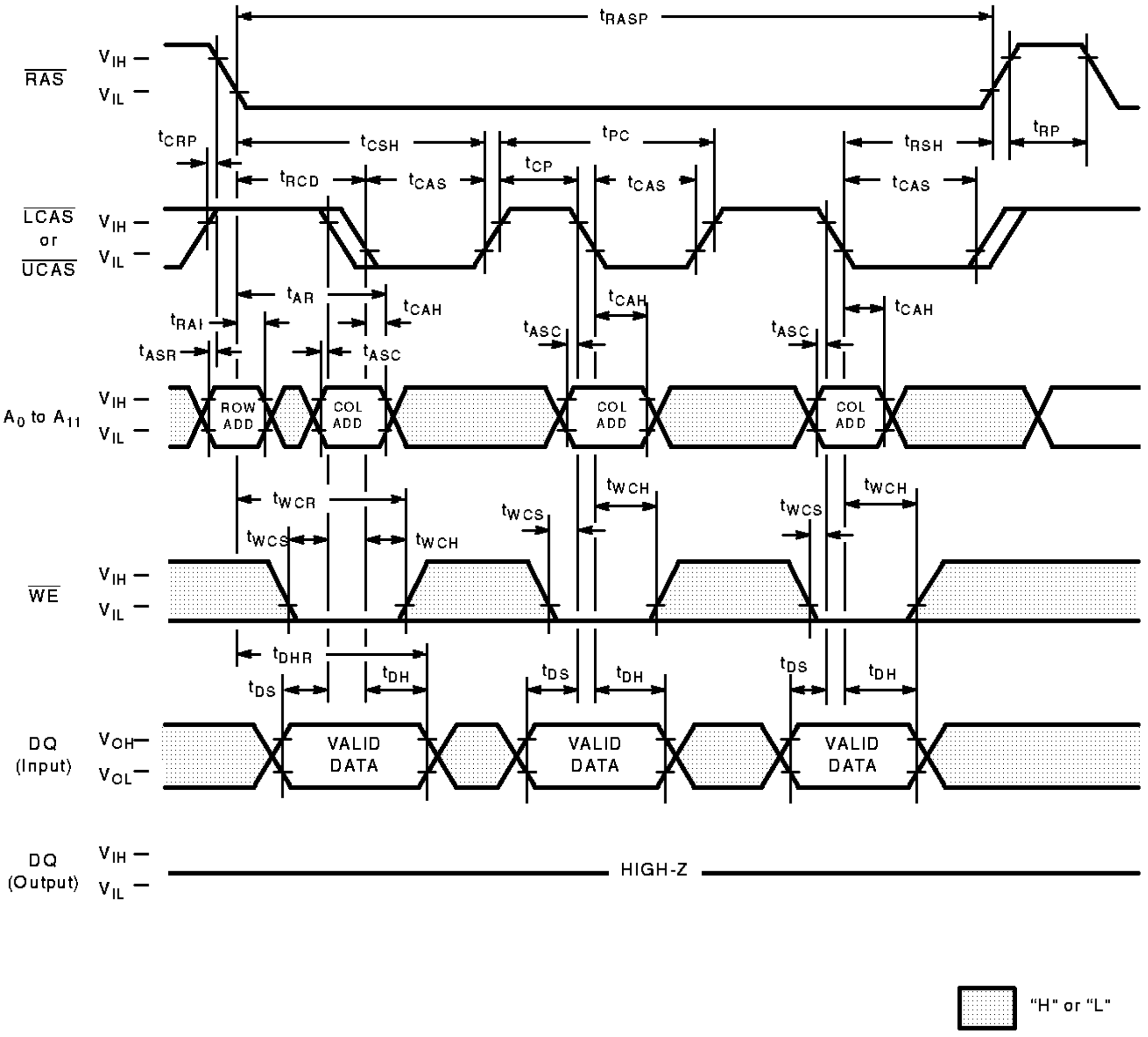
Fig. 9 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The address time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the lastest in occuring.

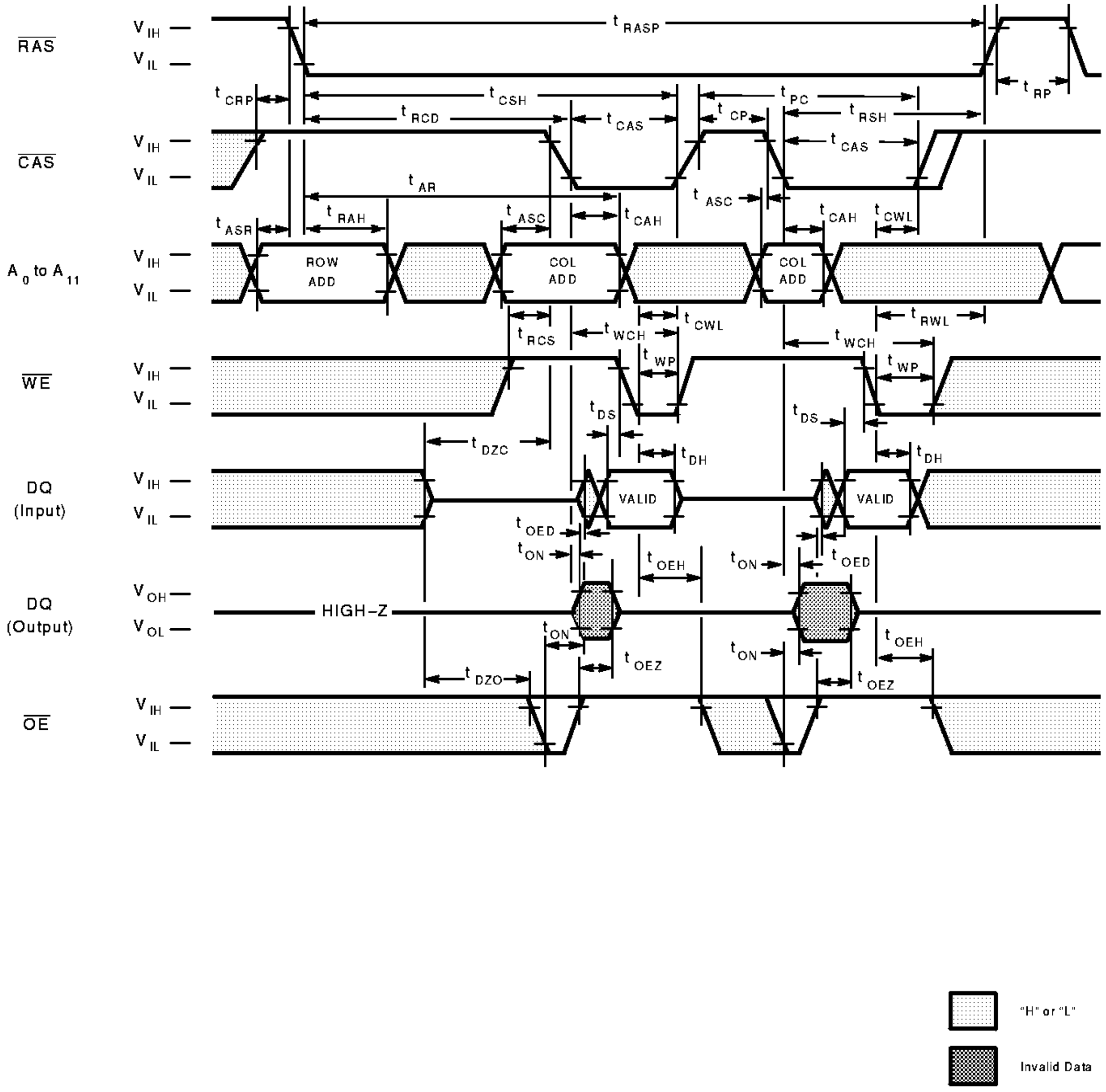
Fig. 10 – FAST PAGE MODE EARLY WRITE CYCLE ($\overline{\text{OE}}$ = “H ”or “L”)



DESCRIPTION

The fast page mode early write cycle is executed in the same manner as the fast page mode read cycle except the states of WE and $\overline{\text{OE}}$ are reversed. Data appearing on the DQ1 to DQ8 is latched on the falling edge of $\overline{\text{LCAS}}$ and one appearing on the DQ9 to DQ16 is latched on the falling edge of $\overline{\text{UCAS}}$ and the data is written into the memory. During the fast page mode early write cycle, including the delayed ($\overline{\text{OE}}$) write and read-modify-write cycles, t_{CWL} must be satisfied.

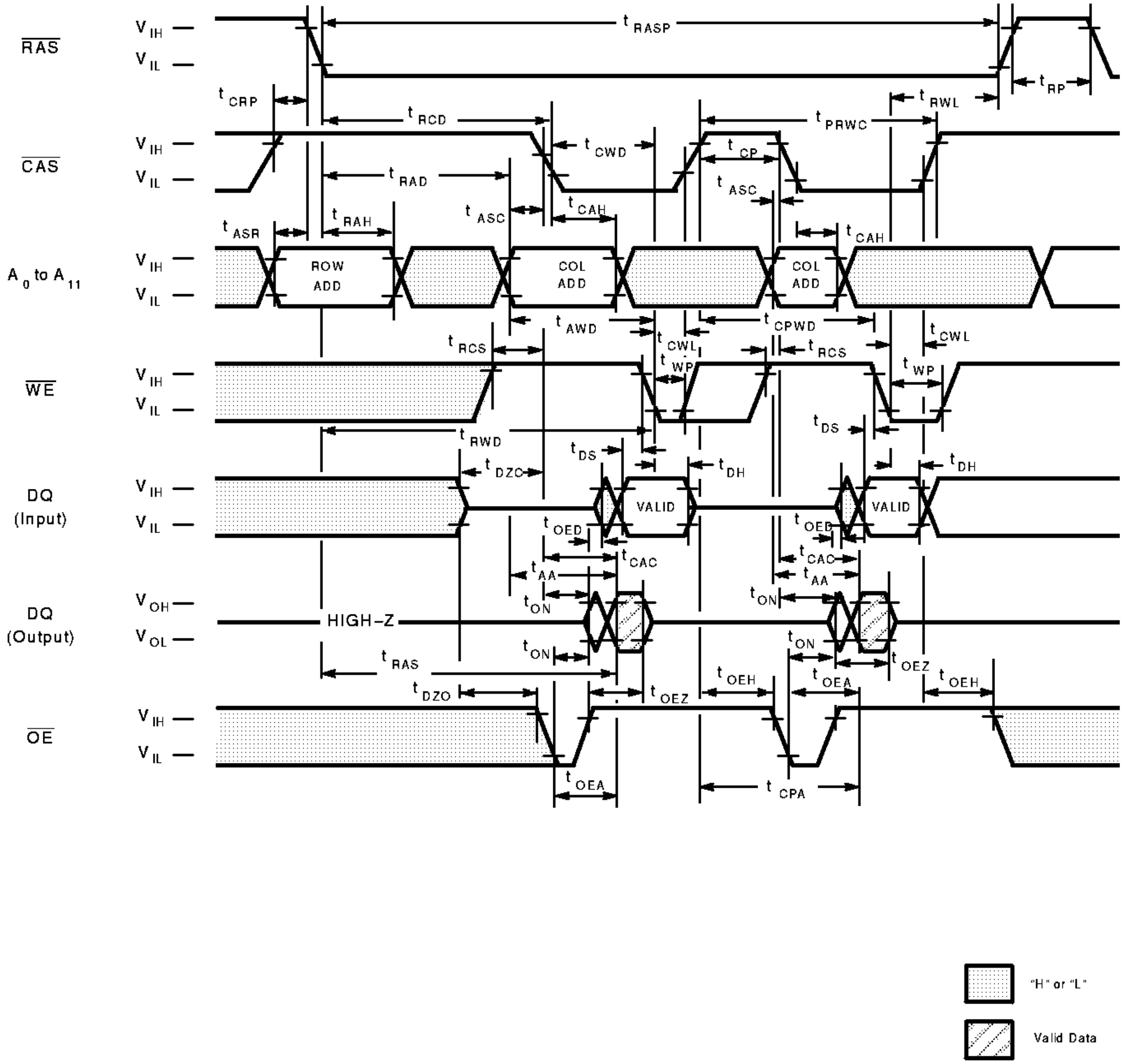
Fig. 11 – FAST PAGE MODE DELAYED WRITE CYCLE



DESCRIPTION

The fast page mode delayed write cycle is executed in the same manner as the fast page mode early write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low $(t_{OED} + t_T + t_{DS})$.

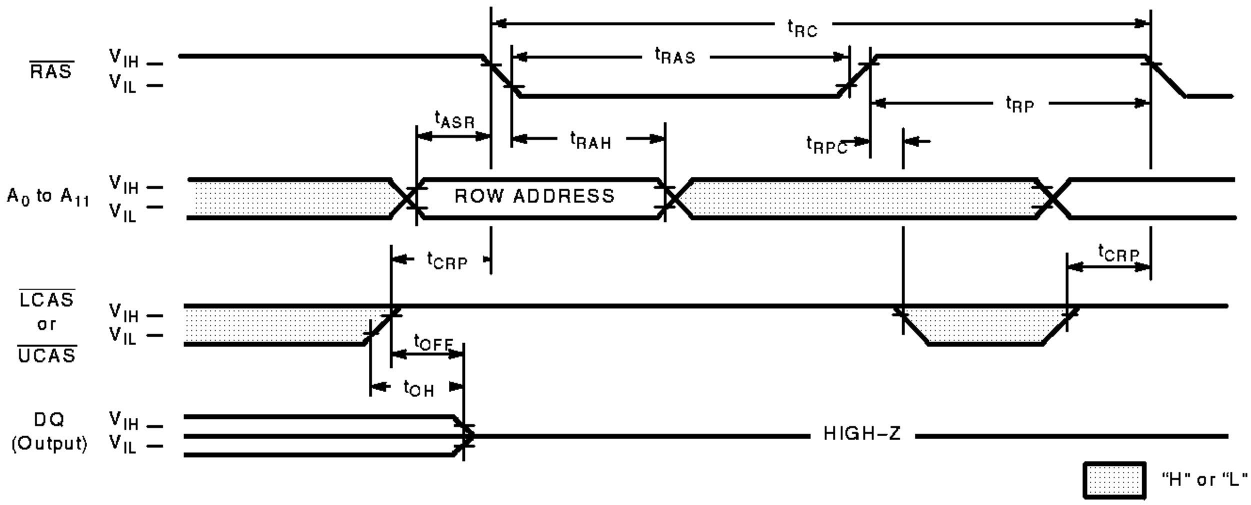
Fig. 12 – Fast Page Mode Read Modify Write Cycle



DESCRIPTION

During the fast page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input data appears at the DQ pins during a normal cycle.

Fig. 13 – $\overline{\text{RAS}}$-ONLY REFRESH ($\overline{\text{WE}}$ = $\overline{\text{OE}}$ = "H"or "L")

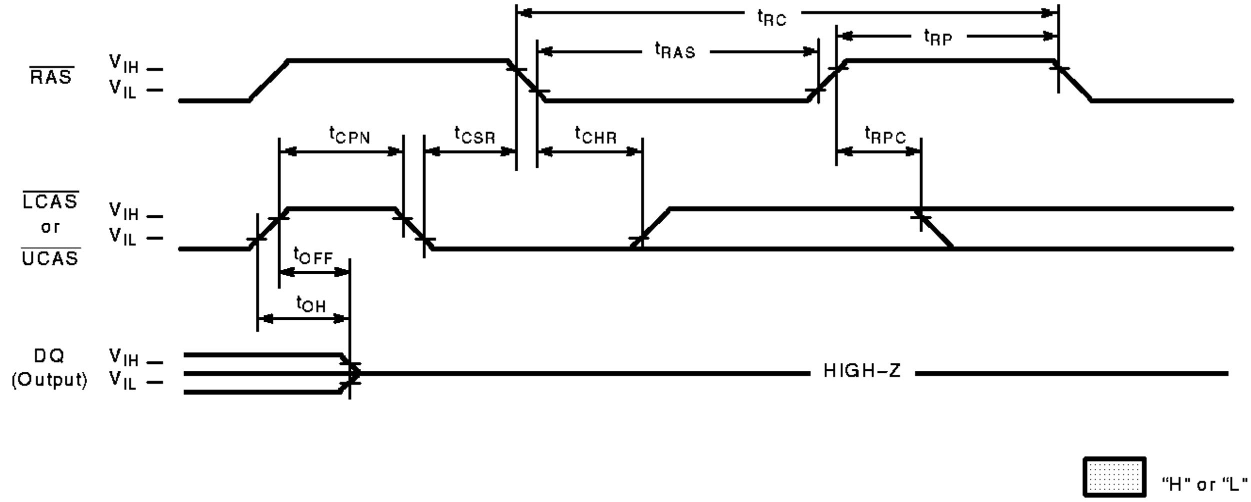


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 4096 row addresses every 65.6–milliseconds. Three refresh modes are available: $\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, and hidden refresh.

$\overline{\text{RAS}}$-only refresh is performed by keeping $\overline{\text{RAS}}$ Low and $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of RAS. During $\overline{\text{RAS}}$-only refresh, DQ pins are kept in a high-impedance state.

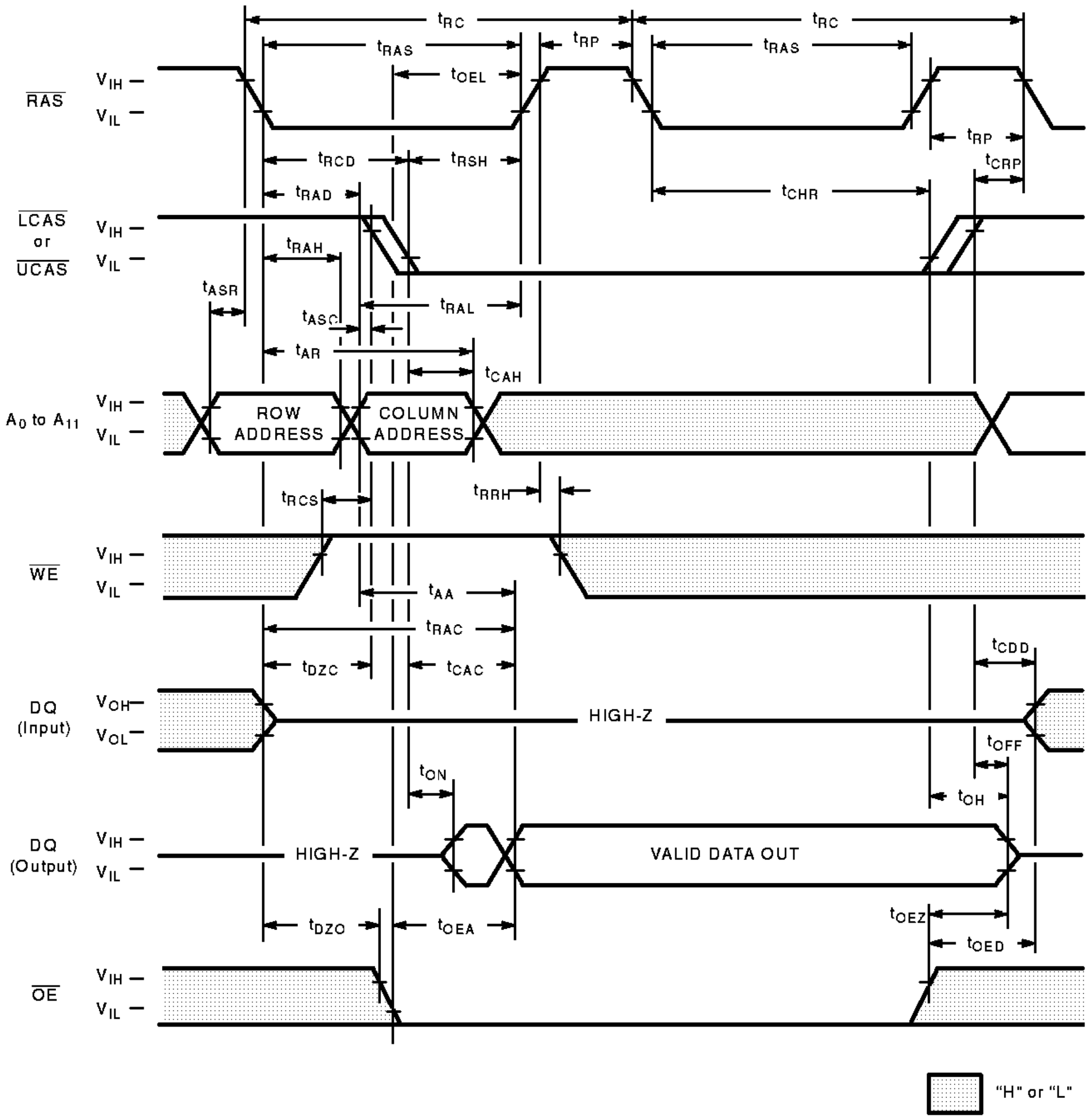
Fig. 14 – $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH (ADDRESSES = $\overline{\text{WE}}$ = $\overline{\text{OE}}$ = "H"or "L")



DESCRIPTION

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ is held Low for the specified setup time (t_{CSR}) before $\overline{\text{RAS}}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation.

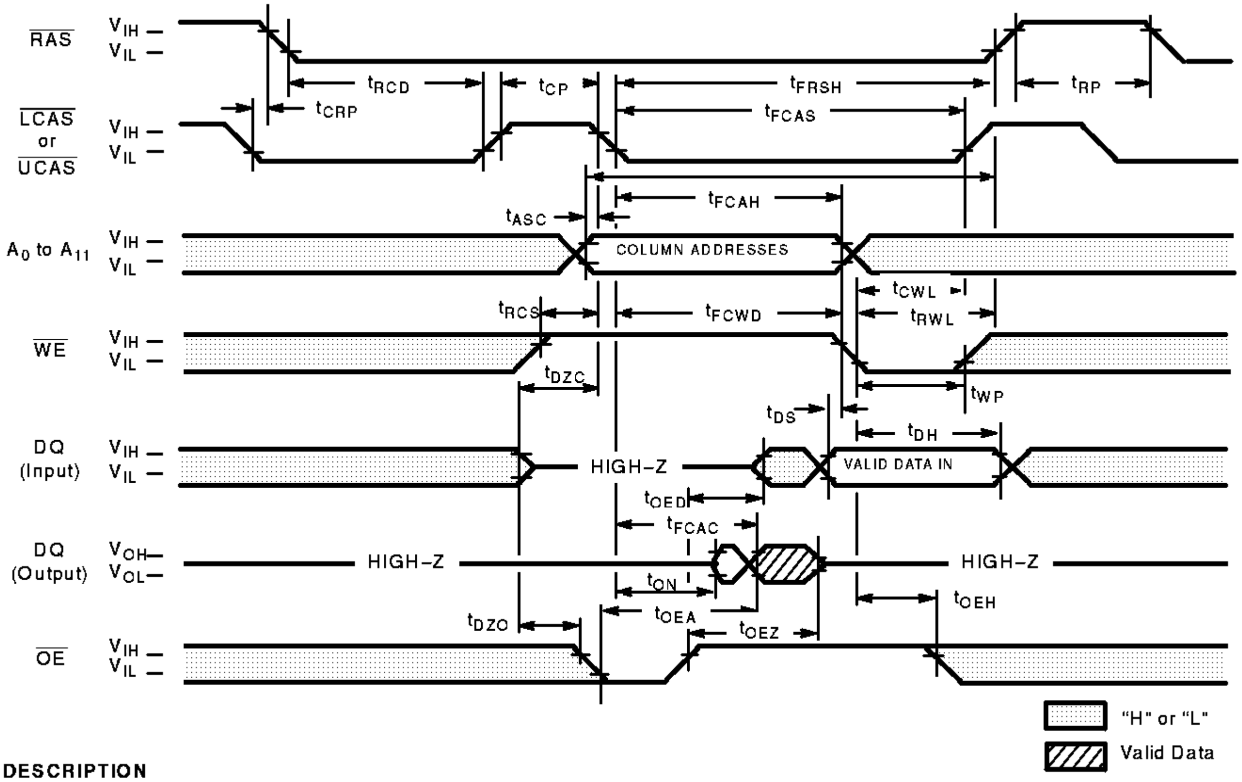
Fig. 15 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and cycling $\overline{\text{RAS}}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability.

Fig. 16 – $\overline{\text{CAS}}$–BEFORE–$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the function of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh circuitry. If, after a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle $\overline{\text{CAS}}$ makes a transition from High to Low while RAS is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A11 are defined by the on-chip refresh counter.
Column Addresses: Bits A0 through A7 are defined by latching levels on A0–A7 at the second falling edge of $\overline{\text{CAS}}$.

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test procedure is as follows;

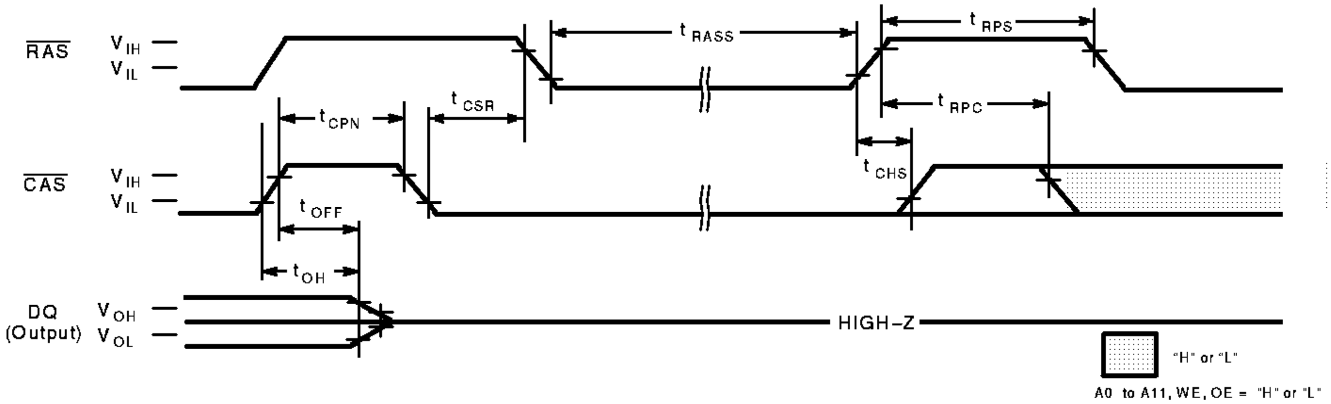
1) Initialize the internal refresh address counter by using 8 $\overline{\text{RAS}}$ only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 4096 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test (read-modify-write cycles). Repeat this procedure 4096 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 4096 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V16160A-60		MB81V16160A-70		Unit
			Min	Max	Min	Max	
90	Access Time from $\overline{\text{CAS}}$	t_{FCAC}	—	50	—	55	ns
91	Column Address Hold Time	t_{FCAH}	35	—	35	—	ns
92	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{FCWD}	70	—	77	—	ns
93	$\overline{\text{CAS}}$ Pulse width	t_{FCAS}	90	—	99	—	ns
94	$\overline{\text{RAS}}$ Hold Time	t_{FRSH}	90	—	99	—	ns

Note. Assumes that $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle only.

Fig. 17 – SELF REFRESH CYCLE (A0–A11 = $\overline{\text{WE}}$ = $\overline{\text{OE}}$ = “H” or “L”)



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V16160A-60		MB81V16160A-70		Unit
			Min	Max	Min	Max	
100	$\overline{\text{RAS}}$ Pulse Width	t_{RASS}	100	—	100	—	µs
101	$\overline{\text{RAS}}$ Precharge Time	t_{RPS}	110	—	125	—	ns
102	$\overline{\text{CAS}}$ Hold Time	t_{CHS}	–50	—	–50	—	ns

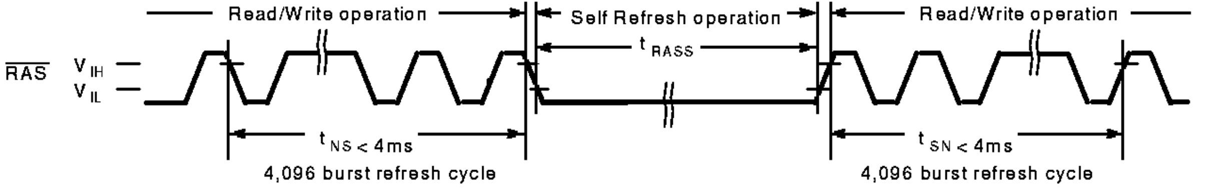
Note . Assumes self refresh cycle only

DESCRIPTION

The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter.
If $\overline{\text{CAS}}$ goes to "L" before /$\overline{\text{RAS}}$ goes to "L" (CBR) and the condition of $\overline{\text{CAS}}$ "L" and /$\overline{\text{RAS}}$ "L" is kept for term of tRASS (more than 100µs), the device can enter the self refresh cycle. Following that, refresh operation is automatically executed at fixed intervals using internal refresh address counter during "/$\overline{\text{RAS}}$=L" and "/$\overline{\text{CAS}}$=L".
Exit from self refresh cycle is performed by toggling /$\overline{\text{RAS}}$ and /$\overline{\text{CAS}}$ to "H" with specified tCHS min.. In this time, /$\overline{\text{RAS}}$ must be kept "H" with specified tRPS min..
Using self refresh mode, data can be retained without external $\overline{\text{CAS}}$ signal during system is in standby.

Restriction for Self Refresh operation ;
For self refresh operation, the notice below must be considered.

1) In the case that distributed CBR refresh are operated between read/write cycles
   Self refresh cycles can be executed without special rule if 4,096 cycles of distributed CBR refresh are executed within tREF max..
2) In the case that burst CBR refresh or distributed/burst /RAS only refresh are operated between read/write cycles
   4,096 times of burst CBR refresh or 4,096 times of burst /RAS only refresh must be executed before and after Self refresh cycles.

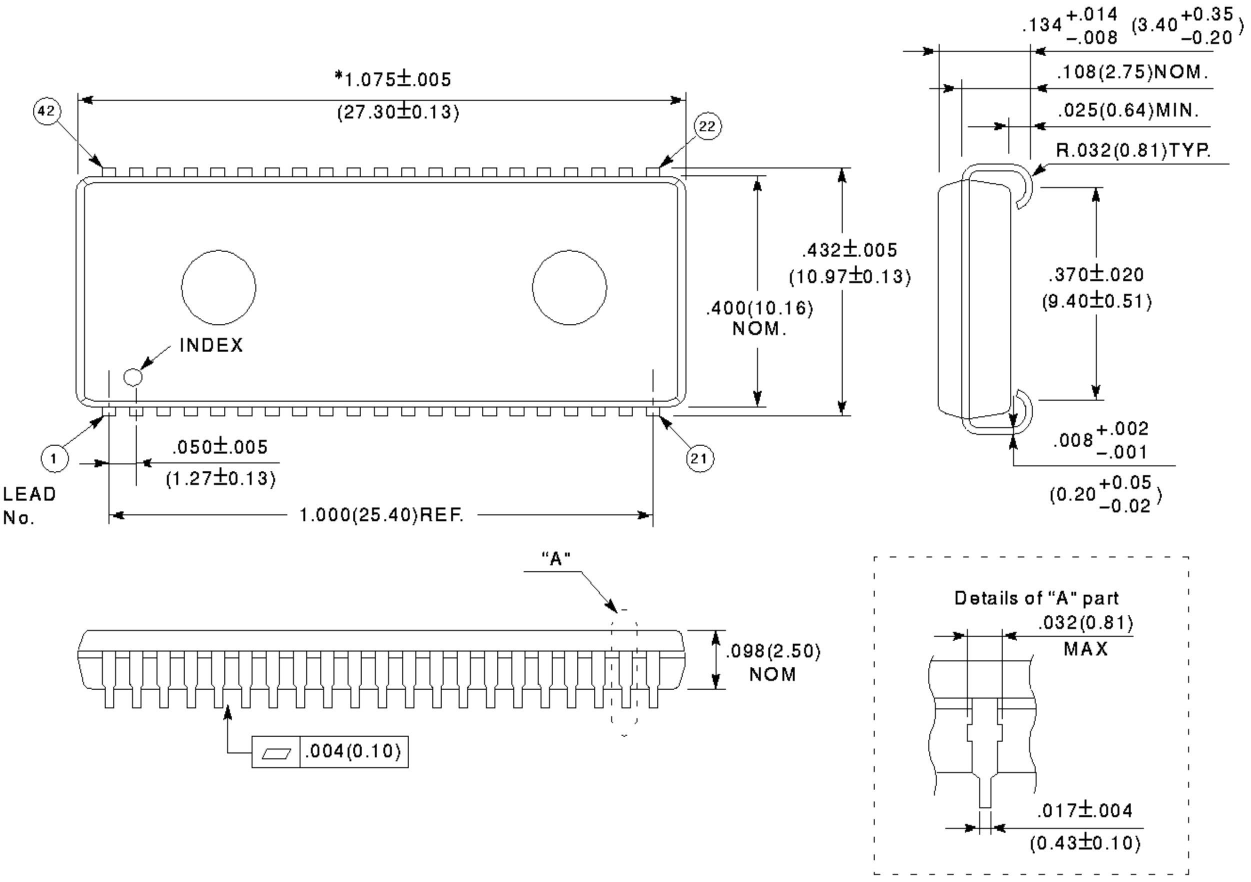


* read/write operation can be performed non refresh time within tNS or tSN

PACKAGE DIMENSIONS

(Suffix: -PJ)

42-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-42P-M01)



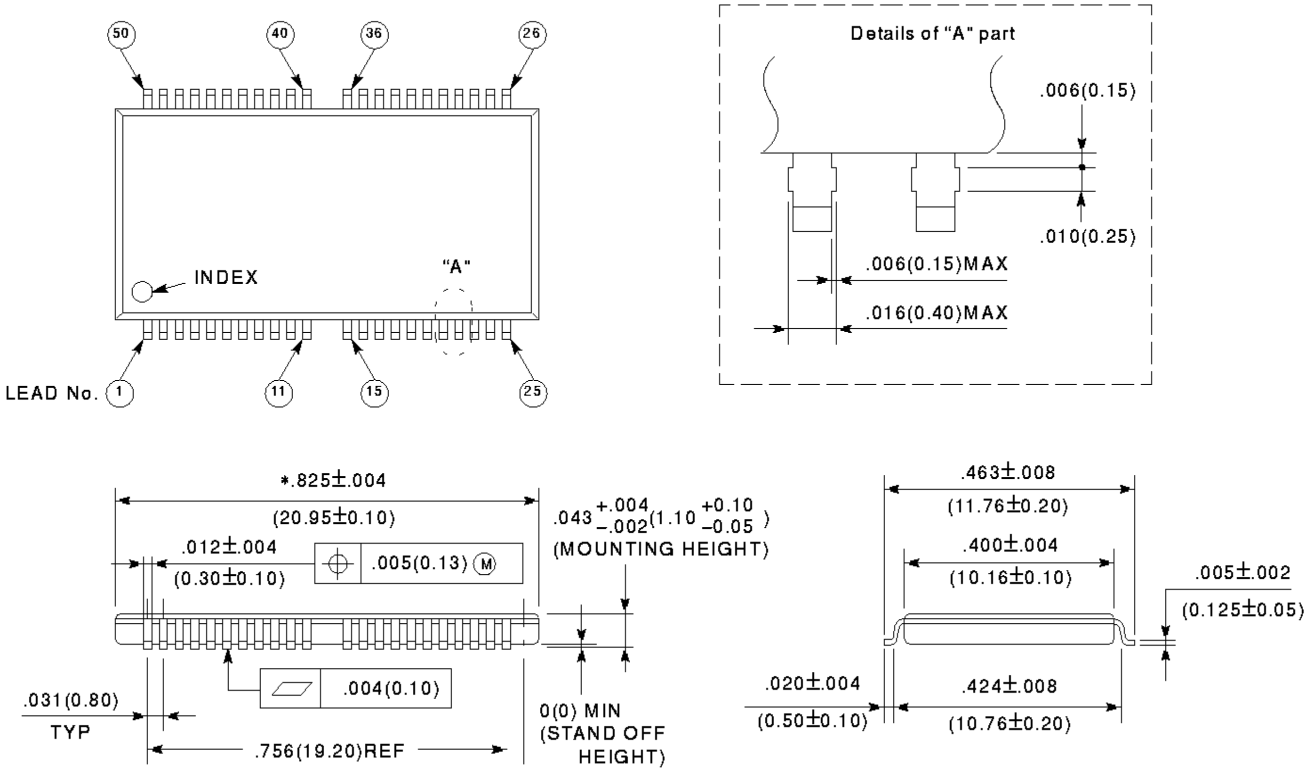
*Resin protrusion. (Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN/PFTR)

50-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-50P-M06)



*: Resin protrusion.(Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

Notes

Notes

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