XH9500 HardWire™ Array Family

July 1996

Advanced Product Specification

Features

- Mask-programmed versions of CPLD
  - Specifically designed for easy XC9500 series CPLD conversions
  - Significant cost reduction for high volume applications
  - Transparent conversion from programmable device
  - On-chip scan-path
  - High performance deep submicron CMOS process
  - Meets XC9500 series -7, -10 speeds
  - 5 V, 3.3 V operation
  - I/O drive = 24 mA
  - IEEE 1149.1 Boundary Scan (JTAG) support
- Easy conversion with guaranteed results
  - No customer engineering resource required
  - Fully pin-for-pin compatible with CPLD
  - Supports most popular package types
  - Same specifications and architecture as programmable CPLD devices
  - Design File used to generate production ready prototypes
  - Prototypes built on production fab line, fully tested to production specification

Description

The XC9500 CPLD family is designed for high performance, general purpose logic integration. The XC9500 architecture consists of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the Fast Connect Switch matrix.

The XH9500 HardWire Arrays are advanced mask-programmed versions of the XC9500 programmable devices. In high volume applications where the design is stable, the programmable CPLD is used for prototyping and initial production can be replaced by their HardWire Array equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

The XH9500 HardWire Array has the identical functional architecture as the programmed XC9500 CPLD it replaces. In the HardWire Array, the logic is optimized for area but maintains the relative FB placement and logic as the programmed CPLD.

Xilinx manufactures the HardWire Array using the information from the programmable array design file. Since the HardWire device is both pinout and architecturally identical to the programmable device, it is easily created without all the costly and time-consuming engineering activity that other semicustom solutions would require – no redesign time, no simulation runs, no place-and-route, and no test-vector generation. The combination of the programmable CPLD and the HardWire Array offers the fastest and easiest way to get a new product to market, while ensuring low cost, low risk, and high-volume cost reduction.

HardWire Array	Replacement for Pin-compatible CPLD		Packages			
			PQFP		HQFP	
		# Pins	100	160	208	304
XH95144	XC95144	Max I/Os	81	133		
XH95180	XC95180			133	168	
XH95216	XC95216			133	168	
XH95288	XC95288				168	192
XH95432	XC95432					232
XH95576	XC95576					232

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