UM3882

Dot Matrix LCD 40-Channel Driver

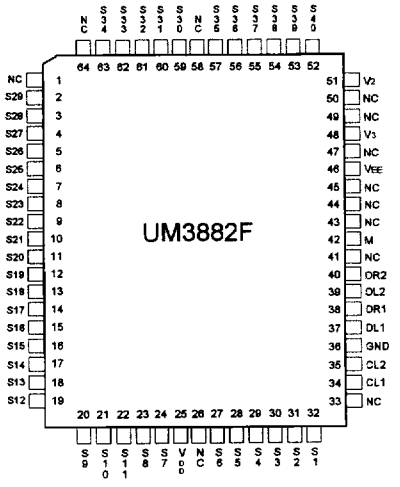
Features

- Provides 40-channel LCD driver
- Internal serial to parallel conversion circuits:
  20-bit shift register x 2
  40-bit latch x 1
  40-bit 4-level driver x 1
- Logic circuit supply voltage:4.5 to 5.5 volts
- LCD driving voltage (V_{DD}-V_{EE}):3.5 to 11 volts
- Applicable LCD duty cycle:1/2 to 1/16
- Interface with UM3881B LCD controller
- LCD bias voltage can be supplied externally

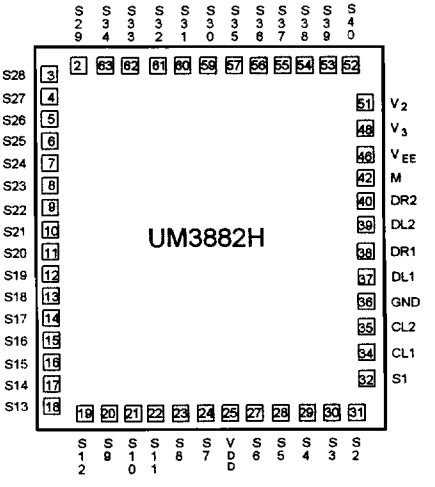
General Description

The UM3882 is a dot matrix LCD 40-channel driver fabricated by low power CMOS technology. This IC consists of two 20-bit shift registers, 40-bit latch and 40-bit 4-level LCD driver.The UM3882 converts serial data which are received from LCD controller, such as UM3881B, to parallel data and outputs LCD driving waveform to drive LCD. Expansion of character-type liquid crystal display can be easily obtained according to the number and structure of characters.

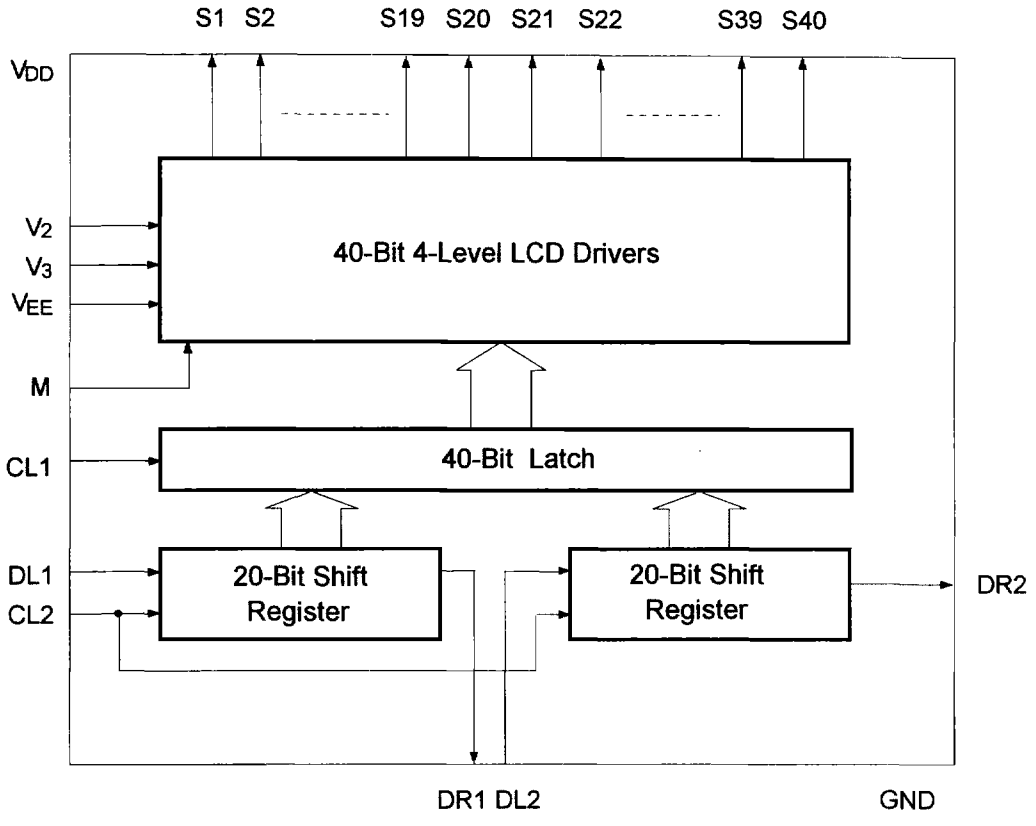
Pin Configuration



Pad Configuration



Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage (V_{DD}-GND). . . . . -0.3V to 7.0V
Power Supply Voltage (V_{DD}-V_{EE}). . . . . .
. . . . . V_{DD}-13.5V to V_{DD} + 0.3V
Input Voltage. . . . . -0.3V to V_{DD} +0.3V
Operating Temperature. . . . . -20°C to +75°C
Storage Temperature. . . . . -55°C to +125°C

Notes :
All voltage values are referenced to GND = 0V
V_2, V_3, V_{EE} must maintain $V_{DD}>V_2>V_3>V_{EE}$

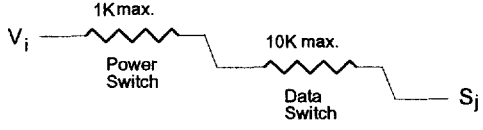
*Comments

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD}=5.0V, GND=0V, V_{EE}=0V, T_A=25°C)

Parameter	Symbol	Terminal	Min.	Typ.	Max.	Unit	Conditions
Input Voltage	V_{IH}	CL1, CL2	0.7 x V_{DD}	-	V_{DD}	V	
	V_{IL}	DL1, DL2	0		0.3 x V_{DD}	V	
Output Voltage	V_{OH}	DR1, DR2	V_{DD}-0.4			V	I_{OH}=-0.4mA
	V_{OL}		-	-	0.4	V	I_{OL}=+0.4mA
Vi-Sj Voltage	V_{D1}	Note 1	-	-	1.1	V	I_{ON}=0.1mA for one of S_j
Descending	V_{D2}		-	-	1.5	V	I_{ON}=0.05mA for each of S_j
Input Leakage Current	I_{IL}	CL1, CL2, DL1, DL2	-5	-	5	µA	V_{IN}=0 or V_{DD}
Vi Leakage Current	I_{VL}	V_2, V_3, V_{EE}	-10	-	10	µA	S1 to S40 open
Power Supply Current	I_{DD}	Note 2	-	-	200	µA	f_{CL1}=1KHz f_{CL2}=400KHz

Note 1: V_i - S_j (V_i = V_{DD}, V_2, V_3, V_{EE} ; j =1 to 40) equivalent circuit

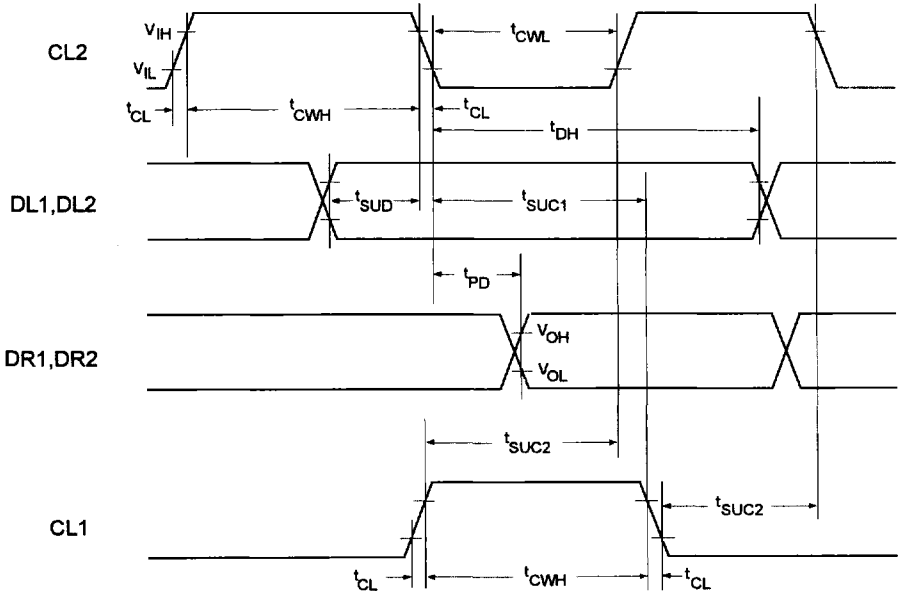


Note 2: Input/output current is excluded. When the input is at the intermediate level with CMOS, some excessive current will flow through the input circuit to power supply. To avoid this, the input level must be fixed at high or low state.

AC Characteristics (V_{DD}=5.0V, GND=0V, V_{EE}=0V, T_A=25°C)

Parameter		Symbol	Terminal	Min.	Typ.	Max.	Unit
Data Shift Frequency		f_{CL2}	CL2	-	-	400	KHz
Clock Width	High	t_{CWH}	CL1, CL2	800	-	-	ns
	Low	t_{CWL}	CL2	800	-	-	ns
Data Hold Time		t_{DH}	DL1, DL2	300	-	-	ns
Data Set-up Time		t_{SUD}	DL1, DL2	300	-	-	ns
Clock Set-up Time (CL2→CL1)		t_{SUC1}	CL1, CL2	500	-	-	ns
Clock Set-up Time (CL1→CL2)		t_{SUC2}	CL1, CL2	500	-	-	ns
Clock Rise/Fall Tme		t_{CL}	CL1, CL2	-	-	200	ns
Data Delay Time		t_{PD}	-	75	-	-	ns

Timing Waveforms



Pin and Pad Descriptions

Pin No.	Pad No.	Designation	I/O	External Connection	Description
2~24, 27~32, 52~57, 59~63	2~24, 27~32, 52~57, 59~63	S29~S7, S6~S1, S40~S35, S30~S34	O	LCD panel	Segment signal output pins
25	25	V_{DD}	P	Power supply	Power for logic circuits
34	34	CL1	I	Controller	Clock to latch serial data
35	35	CL2	I	Controller	Clock to shift serial data
36	36	GND	P	Power Supply	0V
37	37	DL1	I	Controller or UM3882	Data input of 1~20 bits from controller
38	38	DR1	O	UM3882	Data output of 20 bit shift register
39	39	DL2	I	Controller or UM3882	Data input of 21~40 bits from controller
40	40	DR2	O	UM3882	Data output of 40 bit shift register
42	42	M	I	Controller	Alternate signal for LCD drivers
46, 48, 51	46, 48, 51	V_{EE}, V_3, V_2	P	Power Supply	Power for LCD drivers
1, 26, 33, 41, 43~45, 47, 49, 50, 58, 64	-	NC	-	-	No connection

Functional Description

UM3882 is a dot matrix LCD segment driver LSI. It operates with the controller, such as UM3881B, or(and) another segment driver LSI UM3882. UM3882 receives serial data from the controller or another UM3882, converts it to parallel data and supplies LCD driving waveforms to the LCD panel.

1. CL1

This signal is used for latching the shift register contents. When CL1 is set at high, the shift register contents are transferred to the 40-bit 4-level LCD driver. When CL1 is set to low, the last display output data (S1 to S40) are held.

2. CL2

Clock pulse inputs for the two 20-bit shift registers. The data are shifted to 40-bit latch at the falling edge of CL2. The clock signal CL2 must be active when operating to refresh shift registers' contents.

3. DL1

The 1~20 bit data from LCD controller is fed into the first 20-bit shift register through DL1.

4. DR1

The 20th bit data of first 20-bit shift register output from DR1. The data shifted out from DR1 after 20 bit delay are synchronized with the clock pulse(CL2). By connecting DR1 to DL2, two 20-bit shift registers can be cascaded to one 40-bit shift register.

5. DL2

The 21~40 bit data from LCD controller are fed into the second 20-bit shift register through DL2.

6. DR2

The 40th bit data of second 20-bit shift register output from DR2. The data shifted out from DR2 after 20 bit delay are synchronized with the clock pulse(CL2). By connecting DR2 to the next UM3882 DL1, the cascade construction is obtained to drive a wider LCD panel.

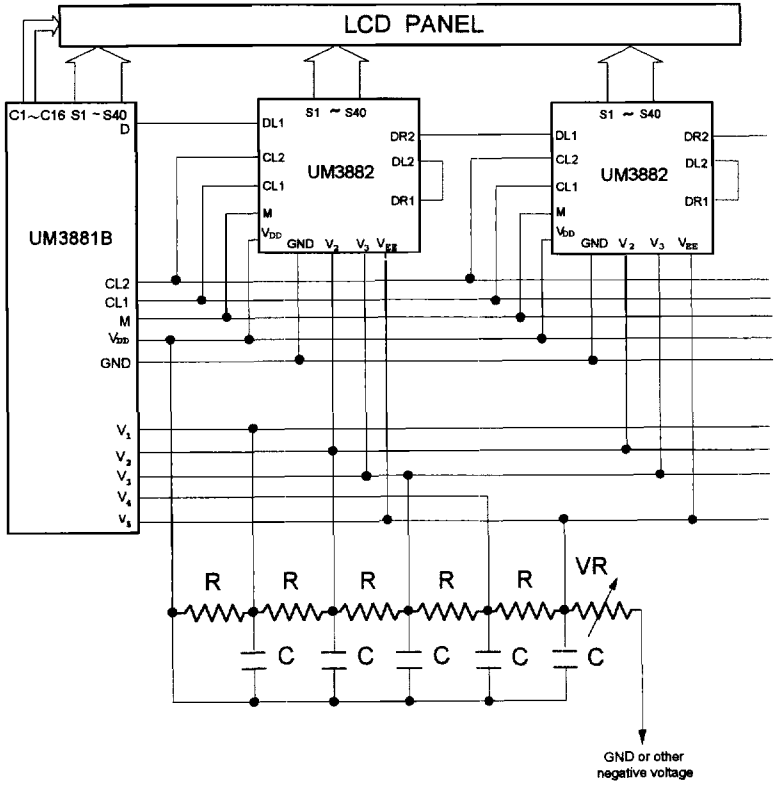
7. S1 to S40

These 40 bits represent the 40 data bits in the 40-bit latch. One of V_{DD}, V_2, V_3 and V_{EE} is selected as a LCD driving voltage source according to the combination of latched data level and the alternate signal(M).

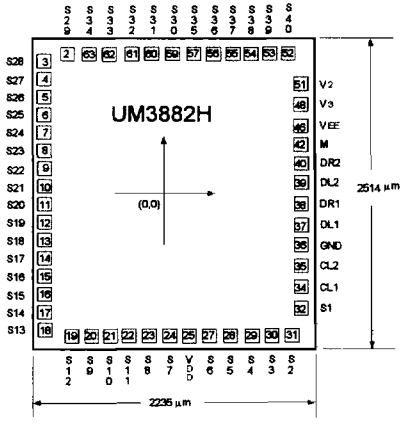
The truth table is listed as follows :

Latched Data	M	Output level of S1 to S40
1(High)	1(High)	V_{EE}
(Selected)	0(Low)	V_{DD}
0(Low)	1(High)	V_3
(Nonselected)	0(Low)	V_2

Application Circuit (for reference only)



Bonding Diagram



* Connecting IC substrate to V_{DD} or keeping floating is recommended.
* Pad window area120µm x 110µm.

Pad No.	Designation	X	Y
2	S29	-729	1148
3	S28	-985	1125
4	S27	-985	975
5	S26	-985	825
6	S25	-985	675
7	S24	-985	525
8	S23	-985	375
9	S22	-985	225
10	S21	-985	75
11	S20	-985	-75
12	S19	-985	-225
13	S18	-985	-375
14	S17	-985	-525
15	S16	-985	-675
16	S15	-985	-825
17	S14	-985	-975
18	S13	-985	-1125
19	S12	-729	-1148
20	S9	-579	-1148
21	S10	-429	-1148
22	S11	-279	-1148
23	S8	-129	-1148
24	S7	21	-1148
25	V_{DD}	171	-1148
27	S6	321	-1148
28	S5	471	-1148
29	S4	621	-1148
30	S3	771	-1148
31	S2	921	-1148
32	S1	985	-859
34	CL1	985	-705
35	CL2	985	-555
36	GND	985	-373
37	DL1	985	-204
38	DR1	985	-54
39	DL2	985	96
40	DR2	985	246
42	M	985	396
46	V_{EE}	985	562
48	V_3	985	722
51	V_2	985	882
52	S40	921	1148
53	S39	771	1148
54	S38	621	1148
55	S37	471	1148
56	S36	321	1148
57	S35	171	1148
59	S30	21	1148
60	S31	-129	1148
61	S32	-279	1148
62	S33	-429	1148
63	S34	-579	1148

(unit:µm)

Ordering Information

Part No.	Package
UM3882H	CHIP FORM
UM3882F	64L QFP