

7483, LS83A Adders

4-Bit Full Adder Product Specification

Logic Products

FEATURES

- High speed 4-bit binary addition
- Cascadeable in 4-bit increments
- LS83A has fast internal carry lookahead
- See '283 for corner power pin version

DESCRIPTION

The '83 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the '83 can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). See Function Table. With active-HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN} , A_1 , B_1 , can arbitrarily be assigned to pins 10, 11, 13, etc.

TYPE	TYPICAL ADD TIMES (TWO 8-BIT WORDS)	TYPICAL SUPPLY CURRENT (TOTAL)
7483	23ns	66mA
74LS83A	25ns	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7483N, N74LS83AN
Plastic SO	N74LS83AD

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

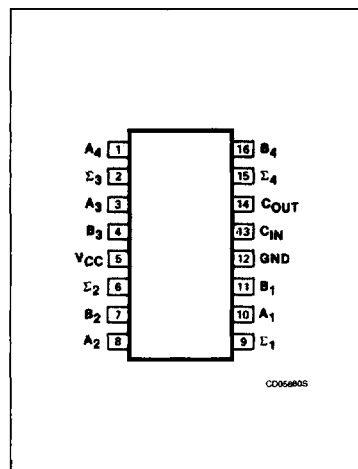
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
$A_1, B_1, A_3, B_3, C_{IN}$	Inputs	2uI	
A_2, B_2, A_4, B_4	Inputs	1uI	
A, B	Inputs		2LSuI
C_{IN}	Input		1LSuI
Sum	Outputs	10uI	10LSuI
Carry	Output	5uI	10LSuI

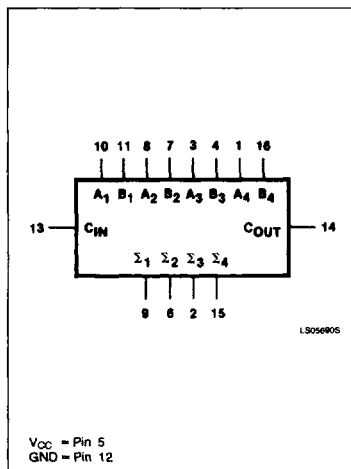
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSuI) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

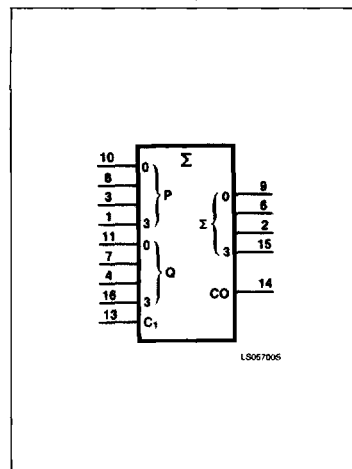
PIN CONFIGURATION



LOGIC SYMBOL



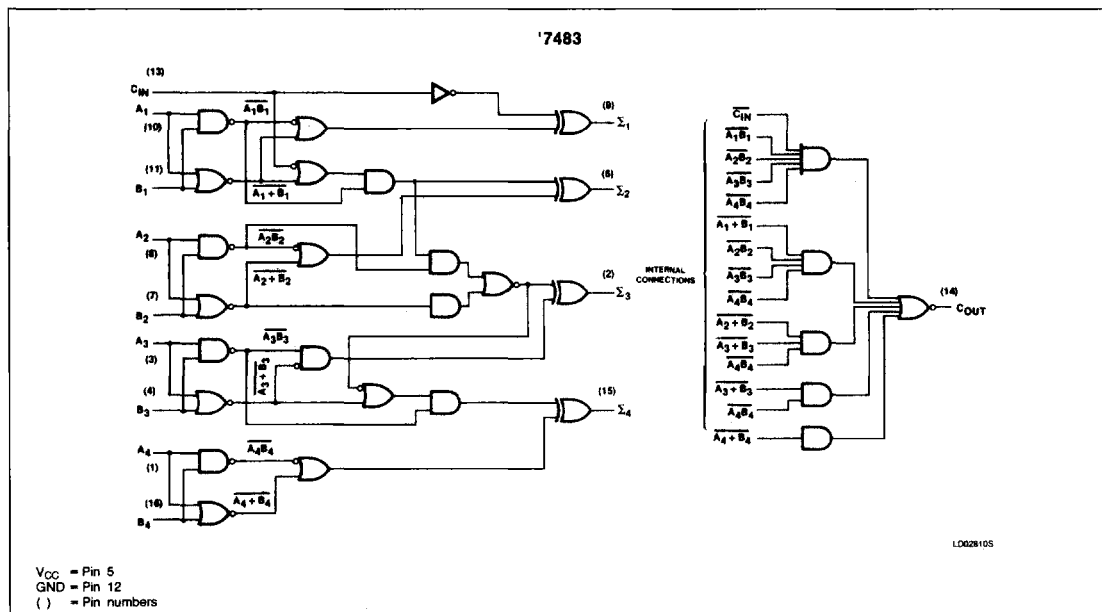
LOGIC SYMBOL (IEEE/IEC)



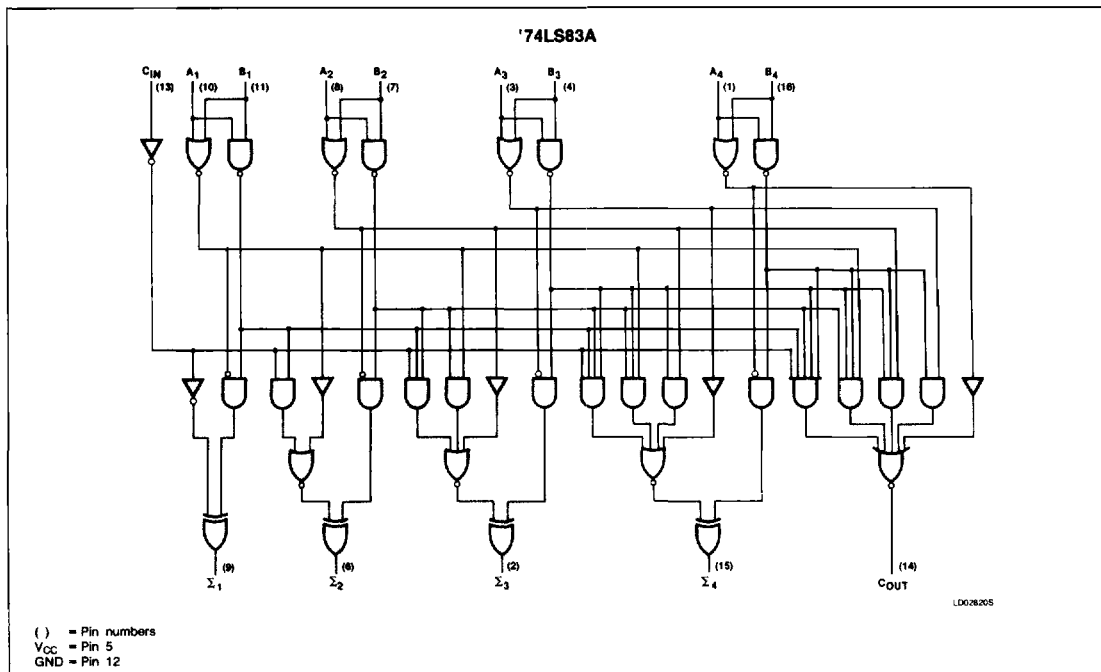
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LOGIC DIAGRAM



LOGIC DIAGRAM



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FUNCTION TABLE

PINS	C _{IN}	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ ₁	Σ ₂	Σ ₃	Σ ₄	C _{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10 + 9 = 19)
(carry + 5 + 6 = 12)

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA
I _{OH}	HIGH-level output current	Sum		-800			-400	μA
		Carry		-400			-400	μA
I _{OL}	LOW-level output current	Sum		16			8	mA
		Carry		8			8	mA
T _A	Operating free-air temperature	0		70	0		70	°C

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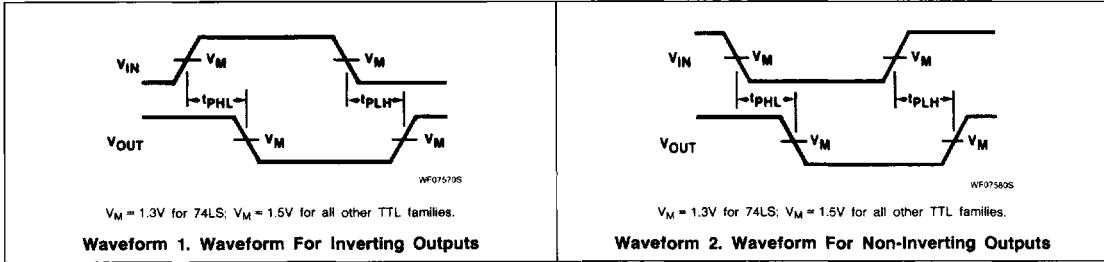
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		7483			74LS83A			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA (74LS)					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA
		A, B inputs						0.2	mA
		C _{IN} input						0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			80				μA
		A ₁ , B ₁ , A ₃ , B ₃ , C _{IN}							
		A ₂ , B ₂ , A ₄ , B ₄			40				μA
		V _I = 2.7V						40	μA
I _{IL} LOW-level input current	V _{CC} = MAX V _I = 0.4V	A ₁ , B ₁ , A ₃ , B ₃ , C _{IN}			-3.2				mA
		A ₂ , B ₂ , A ₄ , B ₄			-1.6				mA
		A, B inputs						-0.8	mA
		C _{IN} input						-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Sum outputs	-18		-55	-20		-100	mA
		C _{OUT} output	-18		-70	-20		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX outputs open	All inputs at 4.5V		66	110		19	34	mA
		All inputs grounded					22	39	mA
		All B inputs low, other inputs at 4.5V					19	34	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



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AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			$C_L = 50\text{pF}, R_L = 400\Omega$		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_1	Waveforms 1 & 2		34 34		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_2	Waveforms 1 & 2		35 35		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_3	Waveforms 1 & 2		50 40		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_4	Waveforms 1 & 2		50 50		24 24	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveforms 1 & 2		40 35		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2 $R_L = 780\Omega$ for 7483		20 20		17 22	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveforms 1 & 2 $R_L = 780\Omega$ for 7483		22 22		17 17	ns

TEST CIRCUITS AND WAVEFORMS

Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns