DATA SHEET

74AC573/74ACT573

Octal D-type transparent latch (3-State)

Product specification

1997 Apr 08

Philips
Semiconductors

PHILIPS

Octal D-type transparent latch (3-State)

74AC573
74ACT573

FEATURES

- 74ACT573 has TTL-compatible inputs
- 74AC573 has CMOS-compatible inputs
- 3-State outputs source/sink 24mA
- 3-State outputs drive bus lines or buffer memory address registers
- Meets or exceeds JEDEC standard for 74AC(T)XX family
- Superior ground bounce noise immunity

DESCRIPTION

The 74AC573/74ACT573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '573' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '573' is functionally identical to the '373', but the '373' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL			UNIT
			AC		ACT	
			V_{CC} = 3.3V	V_{CC} = 5.0V	V_{CC} = 5.0V	
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn; LE to Qn	C_L = 50pF	4.9 5.5	3.5 3.8	4.5 4.8	ns
C_I	Input capacitance		4.5			pF
C_{PD}	Power dissipation capacitance	V_I = GND to V_{CC}[1] outputs enabled[2] outputs enabled[3] outputs disabled[2] outputs disabled[3]	24 84 14 23		28 86 15 30	pF

NOTES:

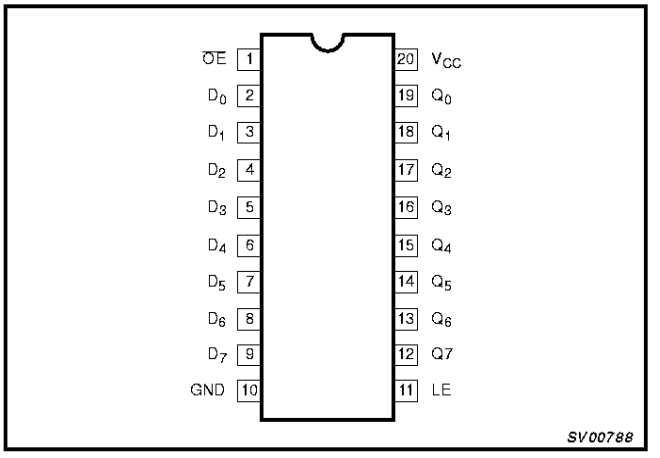
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. Switch the latch enable and one data input such that one latch toggles
3. Switch the latch enable and all data inputs such that all latches toggle

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SO	–40°C to +85°C	74AC573 D 74ACT573 D	74AC573 D 74ACT573 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74AC573 DB 74ACT573 DB	74AC573 DB 74ACT573 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74AC573 PW 74ACT573 PW	74AC573 PW DH 74ACT573 PW DH	SOT360-1

Octal D-type transparent latch (3-State)

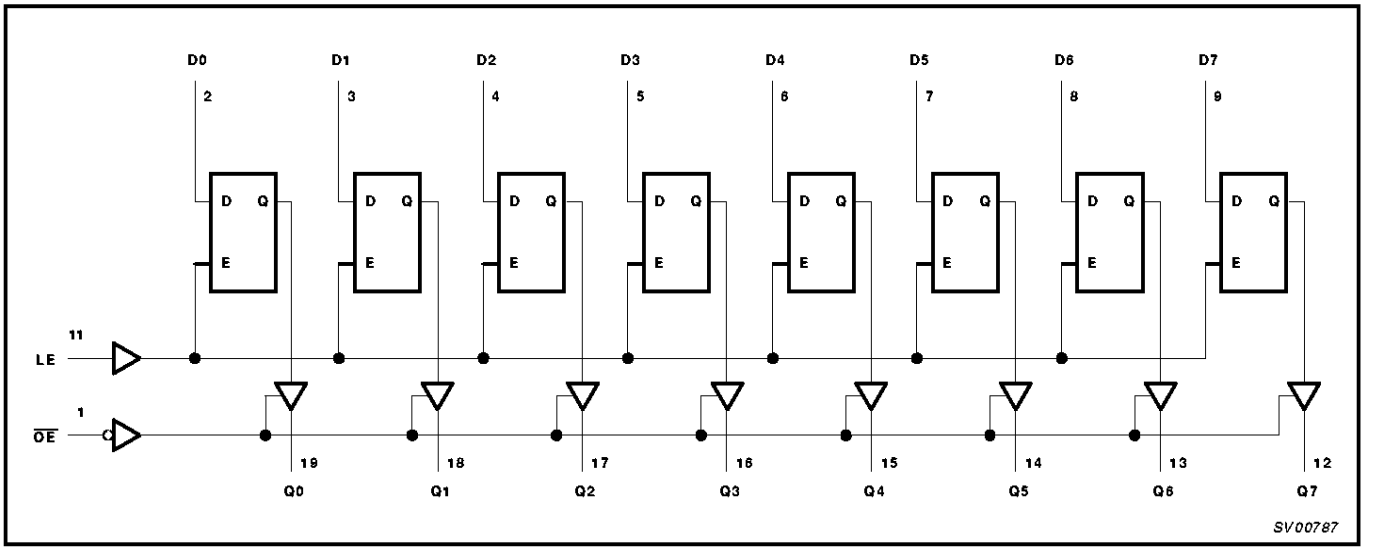
PIN CONFIGURATION



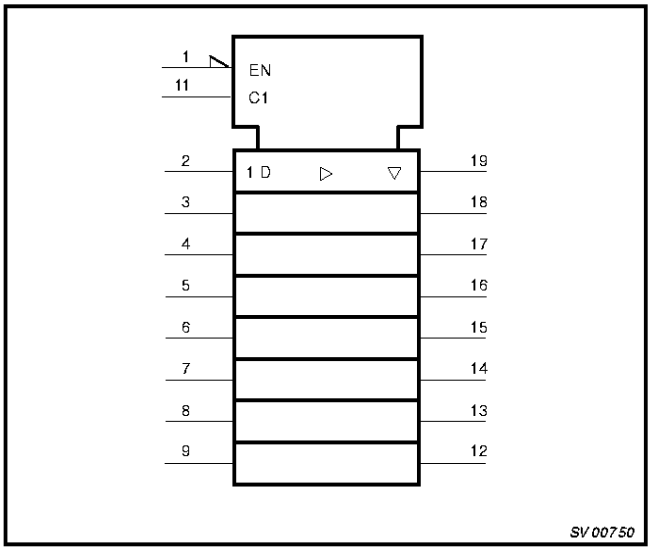
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
10	GND	Ground (0V)
11	LE	Latch enable input (active-High)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage for 'AC	2.0	6.0	V
V_{CC}	DC supply voltage for 'ACT	4.5	5.5	V
V_{IN}	DC input voltage range	0	V_{CC}	V
V_O	DC output voltage range	0	V_{CC}	V
T_{amb}	Operating free-air temperature range	−40	+85	°C
$\Delta V/\Delta t$	Minimum input edge rate — AC devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125		

ABSOLUTE MAXIMUM RATINGS[1]

in accordance with the Absolute Maximum Rating System (IEC134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	V_{IN} = −0.5V	−20	mA
		V_{IN} = V_{CC} + 0.5V	+20	
V_{IN}	DC input voltage		−0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	V_O = −0.5V	−20	mA
		V_O = V_{CC} + 0.5V	+20	
V_O	DC output voltage		−0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current		±50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current per output		±50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current		±200	mA
T_{stg}	Storage temperature range		−65 to 150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (74AC573)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0	2.1	1.5		V
			4.5	3.15	2.25		
			5.5	3.85	2.75		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0		1.5	0.9	V
			4.5		2.25	1.35	
			5.5		2.75	1.65	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	3.0	2.9	2.99		V
			4.5	4.4	4.49		
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –12mA[1]	3.0	2.46			V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76			
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76			
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	3.0		0.01	0.1	V
			4.5		0.01	0.1	
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 12mA[1]	3.0			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			± 1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} ($\overline{OE}$) = V_{IL}, V_{IH} V_{IN} = V_{CC}, GND V_{OUT} = V_{CC}, GND	5.5			± 2.5	μA
I_{OLD}[2]	Dynamic output current[2]	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}[2]	Dynamic output current[2]	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			40	μA

NOTES:

1. All outputs loaded
2. Maximum test duration 2.0 ms; one output loaded at a time

DC ELECTRICAL CHARACTERISTICS (74ACT573)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5	2.0	1.5		V
			5.5	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5		1.5	0.8	V
			5.5		1.5	0.8	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	4.5	4.4	4.49		V
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76	3.86		V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76	4.86		
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	4.5		0.01	0.1	V
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			± 1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} ($\overline{OE}$) = V_{IL}, V_{IH} V_{IN} = V_{CC}, GND V_{OUT} = V_{CC}, GND	5.5			± 2.5	μA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{IN} = V_{CC} – 2.1V Other inputs at V_{CC} or GND; I_{OUT} = 0	5.5			1.5	mA
I_{OLD}[2]	Dynamic output current	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}[2]	Dynamic output current	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			40	μA

NOTES:

1. All outputs loaded
2. Maximum test duration 2.0ms, one output loaded at a time

AC CHARACTERISTICS FOR 74AC573

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V_{CC}[1] (V)	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay D_n to Q_n	3.3 5.0	2.0 1.5	4.9 3.5	12.0 9.0	1.5 1.0	14.0 10.0	ns	2
t_{PHL}	Propagation delay D_n to Q_n	3.3 5.0	2.0 1.5	4.9 3.5	12.0 9.0	1.5 1.0	14.0 10.0	ns	2
t_{PLH}	Propagation delay LE to Q_n	3.3 5.0	2.0 1.5	5.5 3.8	12.0 9.0	1.5 1.0	14.0 10.0	ns	1
t_{PHL}	Propagation delay LE to Q_n	3.3 5.0	2.0 1.5	5.5 3.8	12.0 9.0	1.5 1.0	14.0 10.0	ns	1
t_{PZH}	3-State output enable time $\overline{OE}$ to Q_n	3.3 5.0	2.0 1.5	5.0 3.5	10.5 8.5	1.5 1.0	12.0 9.5	ns	4
t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	3.3 5.0	2.0 1.5	5.9 4.2	10.5 8.5	1.5 1.0	12.0 9.5	ns	4
t_{PHZ}	3-State output disable time $\overline{OE}$ to Q_n	3.3 5.0	2.0 1.5	4.6 2.8	9.0 8.0	1.5 1.0	10.0 9.0	ns	4
t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	3.3 5.0	2.0 1.5	4.3 2.8	9.0 8.0	1.5 1.0	10.0 9.0	ns	4
t_w	LE pulse width HIGH	3.3 5.0	5.5 4.0	2.4 2.2		6.0 4.5		ns	1
t_{su}	Set up time D_n to LE	3.3 5.0	3.5 3.0	−0.3 −0.3		4.0 3.5		ns	3
t_h	Hold time D_n to LE	3.3 5.0	1.0 1.0	0.5 0.5		1.5 1.5		ns	3

NOTE:

1. Voltage range 3.3V is V_{CC} = 3.3V ± 0.3V
   Voltage range 5.0V is V_{CC} = 5.0V ± 0.5V

AC CHARACTERISTICS FOR 74ACT573[1]

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

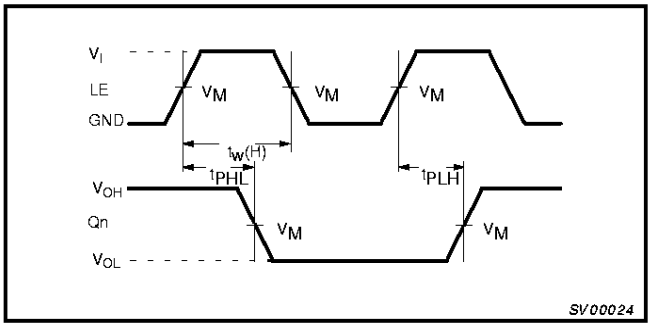
SYMBOL	PARAMETER	V_{CC}[1] (V)	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay D_n to Q_n	5.0	2.0	4.2	9.5	1.5	10.5	ns	2
t_{PHL}	Propagation delay D_n to Q_n	5.0	2.0	4.9	9.5	1.5	10.5	ns	2
t_{PLH}	Propagation delay LE to Q_n	5.0	2.0	4.9	9.5	1.5	10.5	ns	1
t_{PHL}	Propagation delay LE to Q_n	5.0	2.0	4.7	9.5	1.5	10.5	ns	1
t_{PZH}	3-State output enable time $\overline{OE}$ to Q_n	5.0	2.0	4.7	9.5	1.5	10.5	ns	4
t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	5.0	2.0	5.4	9.5	1.5	10.5	ns	4
t_{PHZ}	3-State output disable time $\overline{OE}$ to Q_n	5.0	2.0	4.4	8.5	1.5	9.5	ns	4
t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	5.0	2.0	4.4	8.5	1.5	9.5	ns	4
t_w	LE pulse width HIGH	5.0	3.5	1.8		4.0		ns	1
t_{su}	Set up time D_n to LE	5.0	3.0	−0.8		3.5		ns	3
t_h	Hold time D_n to LE	5.0	2.5	0.8		3.0		ns	3

NOTE:

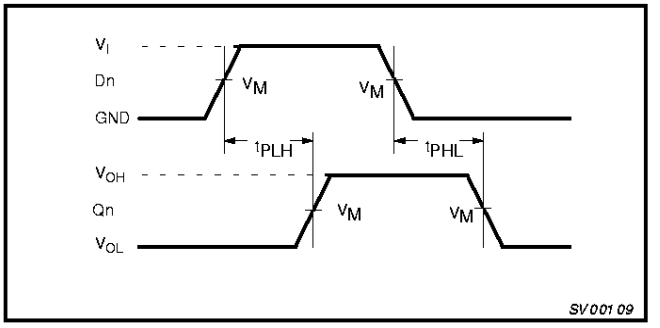
1. These values are at V_{CC} = 5.0V ± 0.5V

AC WAVEFORMS

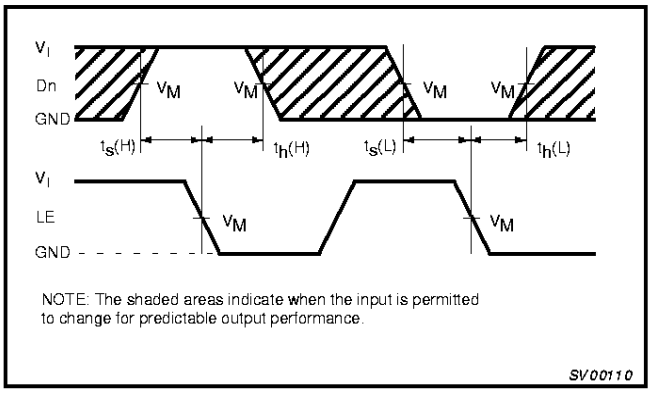
V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.



Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width

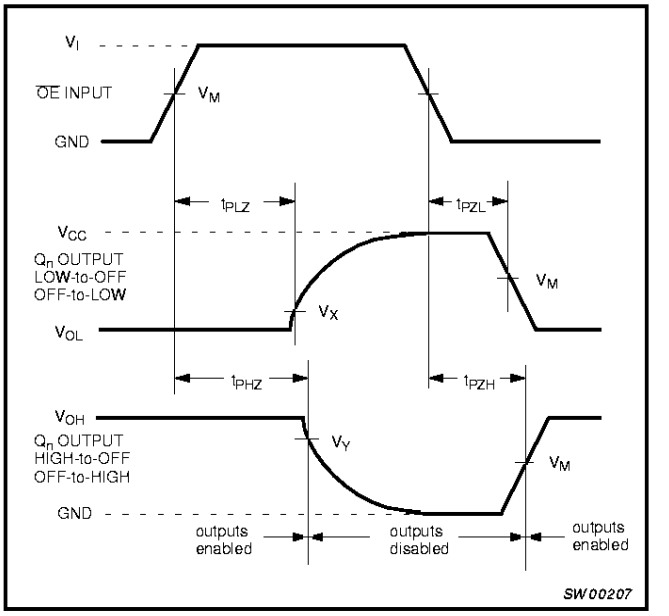


Waveform 2. Propagation Delay for Data to Outputs



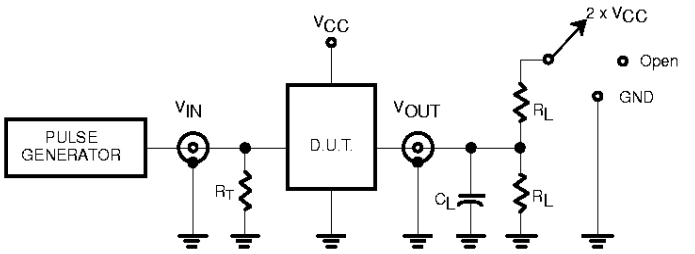
Waveform 3. Data Setup and Hold Times

$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$



Waveform 4. Waveforms showing the 3-State output enable and disable times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	Open

FAMILY	V_I Input Requirements	V_m Input	V_m Output
AC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
ACT	GND to 3.0V	1.5V	50% V_{CC}

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

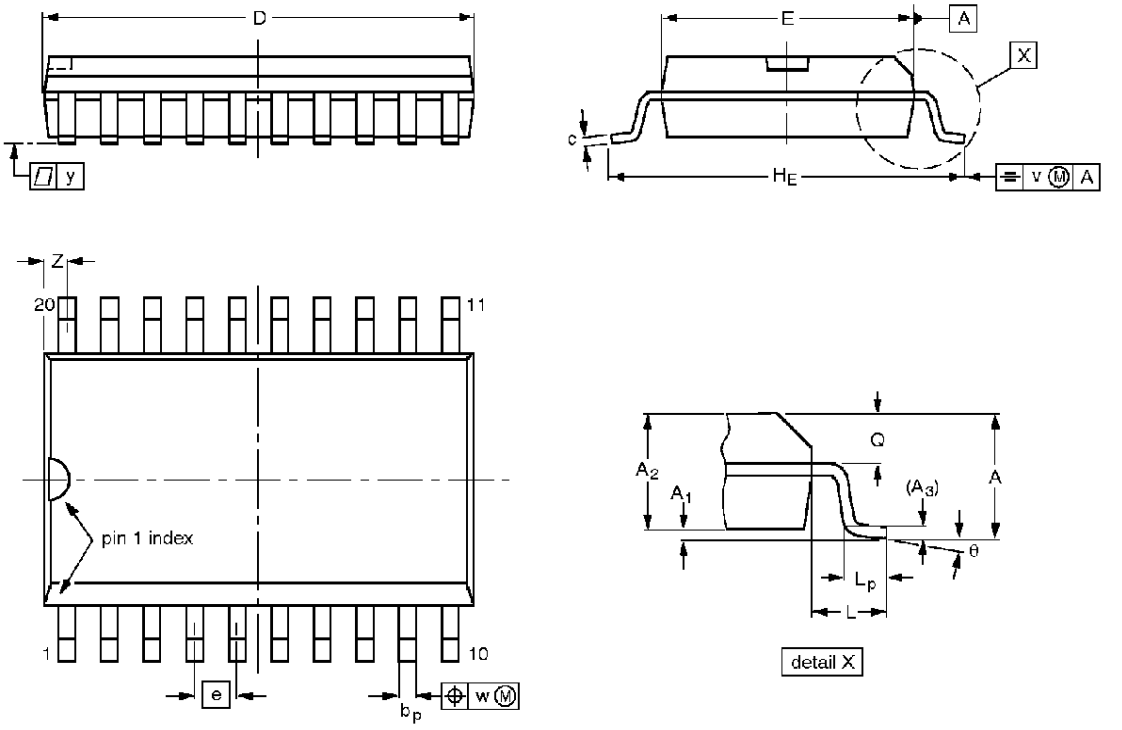
C_L = Load capacitance, see AC characteristics

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00451

Waveform 5. Load circuitry for switching times.

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

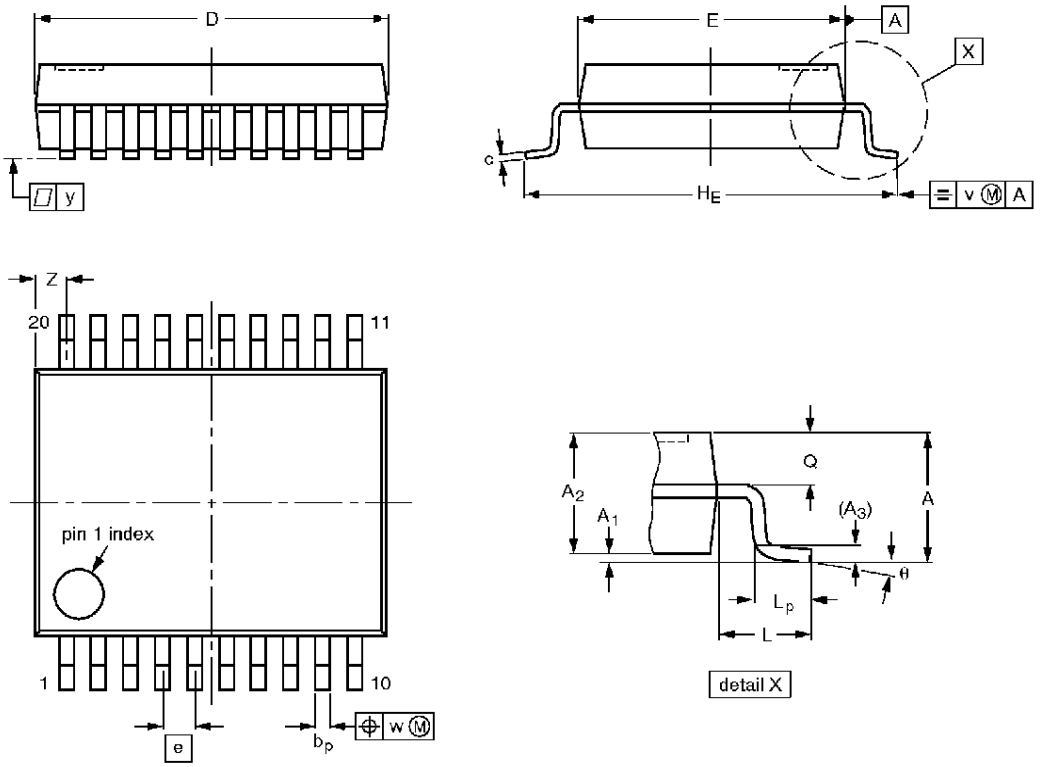
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

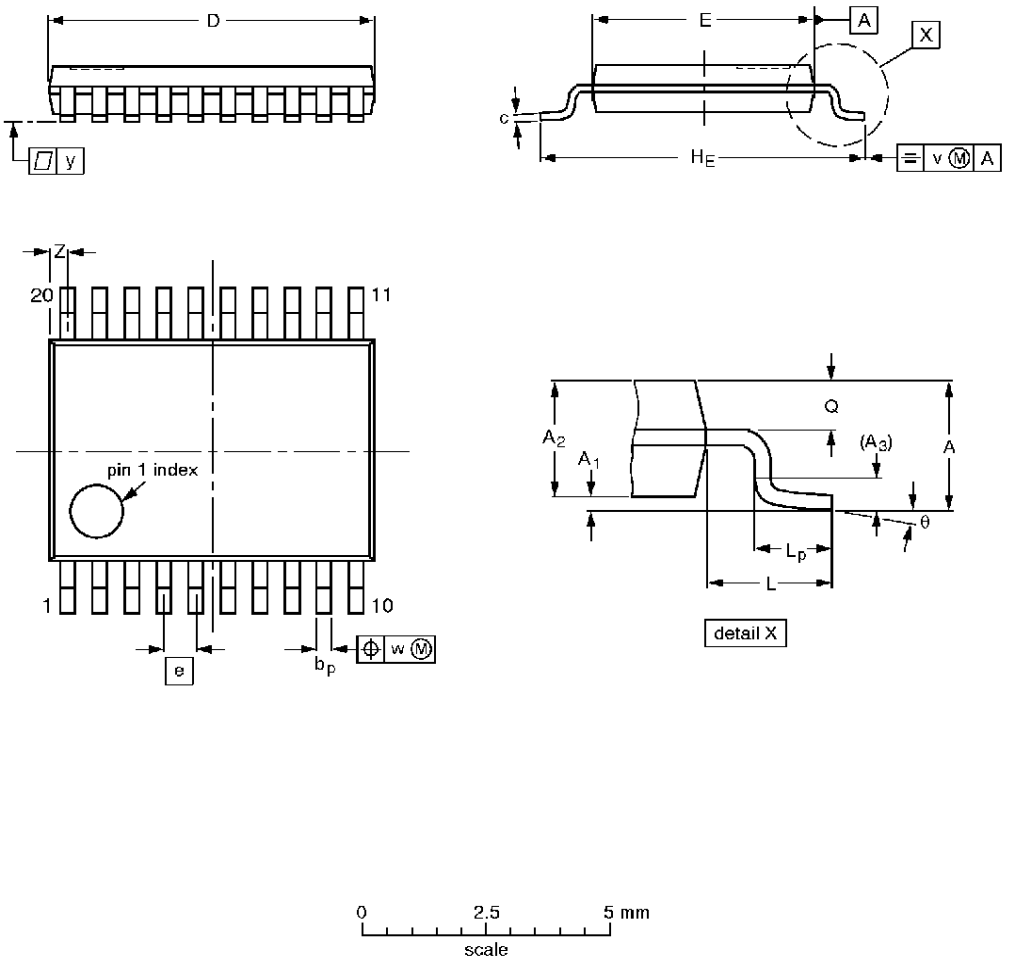
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

Octal D-type transparent latch (3-State)

74AC573
74ACT573

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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