NEC

MOS INTEGRATED CIRCUIT

μPD4516421, 4516821, 4516161

16M-bit Synchronous DRAM

Description

The μPD4516421, 4516821, 4516161 are high-speed 16,777,216-bit synchronous dynamic random-access memories, organized as 2,097,152×4×2, 1,048,576×8×2 and 524,288×16×2 (word×bit×bank), respectively.

The synchronous DRAMs achieve high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAMs compatible with Low Voltage TTL (LVTTL).

The synchronous DRAMs are packaged in 44-pin TSOP (II) (×4, ×8) and 50-pin TSOP (II) (×16).

Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A11 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 Full Page)
- Programmable wrap sequence (Sequential/Interleave)
- Programmable $\overline{CAS}$ latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- ×4, ×8, ×16 organization
- Single +3.3±0.3 V power supply
- LVTTL compatible
- Byte control (×16) by LDQM and UDQM
- 2,048 refresh cycles/32ms
- Burst termination by Burst Stop command and Precharge command

Please contact your NEC sales representative if you need a complete data sheet.

Ordering Information

Part number	Organization (word x bit x bank)	Clock frequency MHz (MAX.)	Package
μPD4516421G5-A10	2Mx4x2	100	44-pin Plastic TSOP(II) (400mil)
4516421G5-A12		83	
4516421G5-A13		77	
4516421G5-A15		66	
μPD4516821G5-A10	1Mx8x2	100	44-pin Plastic TSOP(II) (400mil)
4516821G5-A12		83	
4516821G5-A13		77	
4516821G5-A15		66	
μPD4516161G5-A10	512Kx16x2	100	50-pin Plastic TSOP(II) (400mil)
4516161G5-A12		83	
4516161G5-A13		77	
4516161G5-A15		66	