

# NTD32N06L

## Power MOSFET 32 Amps, 60 Volts Logic Level, N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Features

- Smaller Package than MTB30N06VL
- Lower  $R_{DS(on)}$ ,  $V_{DS(on)}$ , and Total Gate Charge
- Lower and Tighter  $V_{SD}$
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge
- Pb-Free Packages are Available

### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	60	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 10\text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-to-Source Voltage - Continuous - Non-Repetitive ( $t_p \leq 10\text{ ms}$ )	$V_{GS}$ $V_{GS}$	$\pm 20$ $\pm 30$	Vdc
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$ - Continuous @ $T_A = 100^\circ\text{C}$ - Single Pulse ( $t_p \leq 10\ \mu\text{s}$ )	$I_D$ $I_D$ $I_{DM}$	32 22 90	Adc Adc Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	93.75 0.625	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)		2.88	W
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)		1.5	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ (Note 3) ( $V_{DD} = 50\text{ Vdc}$ , $V_{GS} = 5\text{ Vdc}$ , $L = 1.0\text{ mH}$ , $I_{L(pk)} = 25\text{ A}$ , $V_{DS} = 60\text{ Vdc}$ , $R_G = 25\ \Omega$ )	$E_{AS}$	313	mJ
Thermal Resistance - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.6 52 100	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

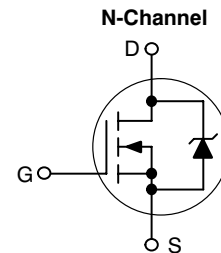
1. When surface mounted to FR4 board using 0.5 in pad size.
2. When surface mounted to FR4 board using minimum recommended pad size.
3. Repetitive rating; pulse width limited by maximum junction temperature.



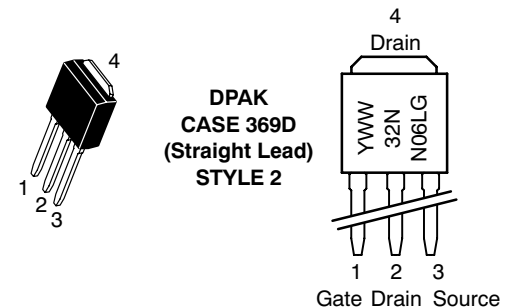
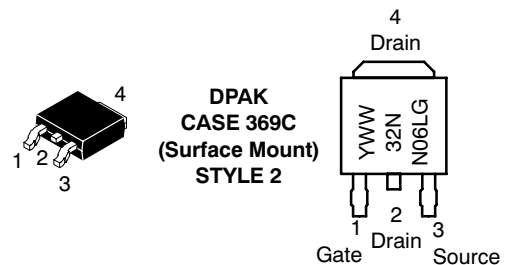
ON Semiconductor®

<http://onsemi.com>

$V_{DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
60 V	23.7 m $\Omega$	32 A



### MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year  
WW = Work Week  
32N06L = Device Code  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# NTD32N06L

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (Note 4) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 -	70 62	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	±100	nAdc

## ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage (Note 4) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 -	1.7 4.8	2.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 4) (V <sub>GS</sub> = 5 Vdc, I <sub>D</sub> = 16 Adc)	R <sub>DS(on)</sub>	-	23.7	28	mΩ
Static Drain-to-Source On-Resistance (Note 4) (V <sub>GS</sub> = 5 Vdc, I <sub>D</sub> = 20 Adc) (V <sub>GS</sub> = 5 Vdc, I <sub>D</sub> = 32 Adc) (V <sub>GS</sub> = 5 Vdc, I <sub>D</sub> = 16 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	- - -	0.48 0.78 0.61	0.67 - -	Vdc
Forward Transconductance (Note 4) (V <sub>DS</sub> = 6 Vdc, I <sub>D</sub> = 16 Adc)	g <sub>FS</sub>	-	27	-	mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	-	1214	1700	pF
Output Capacitance		C <sub>oss</sub>	-	343	480	
Transfer Capacitance		C <sub>rss</sub>	-	87	180	

## SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 32 Adc, V <sub>GS</sub> = 5 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 4)	t <sub>d(on)</sub>	-	12.8	30	ns
Rise Time		t <sub>r</sub>	-	221	450	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	37	80	
Fall Time		t <sub>f</sub>	-	128	260	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 32 Adc, V <sub>GS</sub> = 5 Vdc) (Note 4)	Q <sub>T</sub>	-	23	50	nC
		Q <sub>1</sub>	-	4.5	-	
		Q <sub>2</sub>	-	14	-	

## SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc) (Note 4) (I <sub>S</sub> = 32 Adc, V <sub>GS</sub> = 0 Vdc) (Note 4) (I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	- - -	0.89 0.95 0.74	1.0 - -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 32 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 4)	t <sub>rr</sub>	-	56	-	ns
		t <sub>a</sub>	-	31	-	
		t <sub>b</sub>	-	25	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.093	-	μC

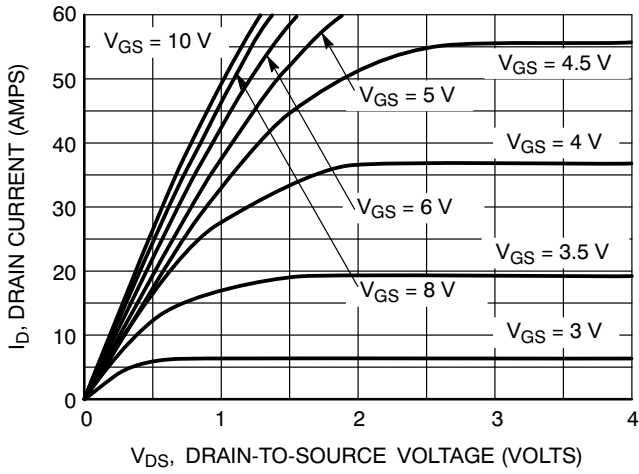
- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

## ORDERING INFORMATION

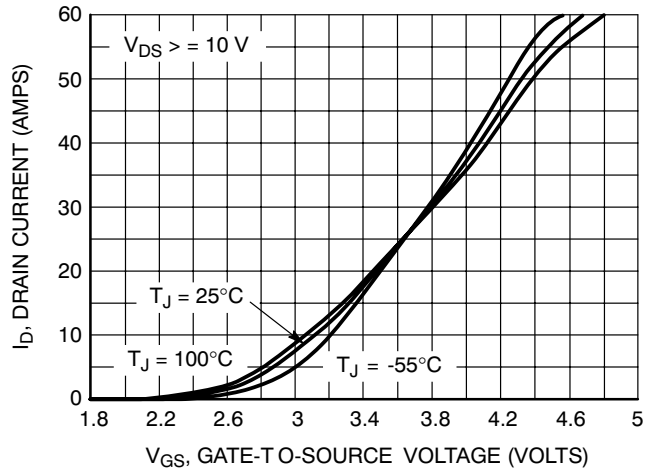
Device	Package	Shipping <sup>†</sup>
NTD32N06L	DPAK	75 Units / Rail
NTD32N06LG	DPAK (Pb-Free)	75 Units / Rail
NTD32N06L-1	DPAK (Straight Lead)	75 Units / Rail
NTD32N06L-1G	DPAK (Straight Lead) (Pb-Free)	75 Units / Rail
NTD32N06LT4	DPAK	2500 Units / Tape & Reel
NTD32N06LT4G	DPAK (Pb-Free)	2500 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

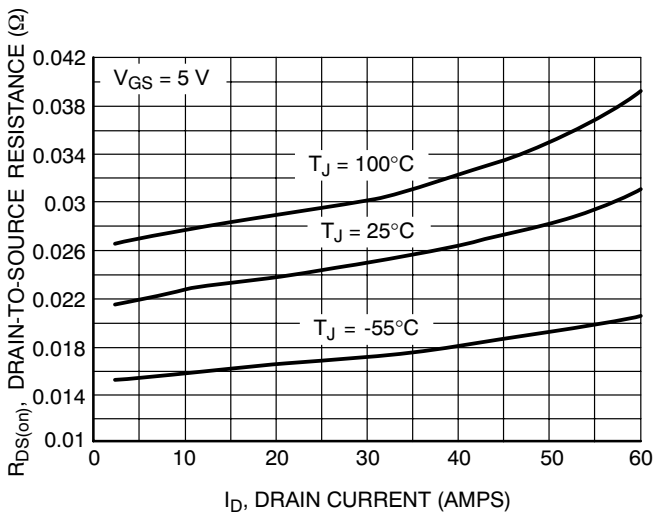
# NTD32N06L



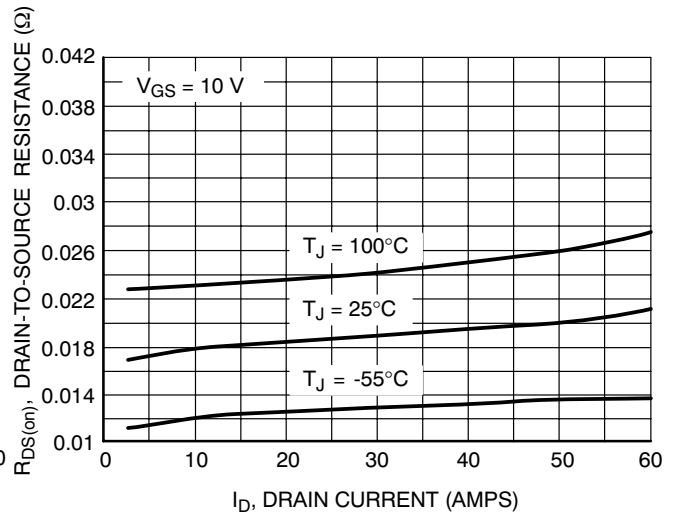
**Figure 1. On-Region Characteristics**



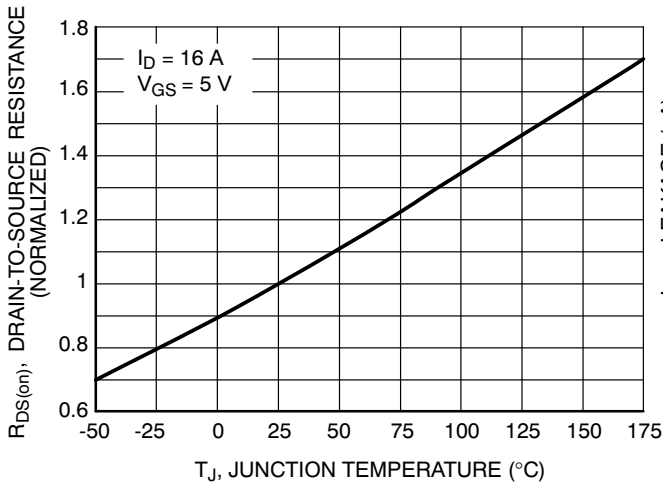
**Figure 2. Transfer Characteristics**



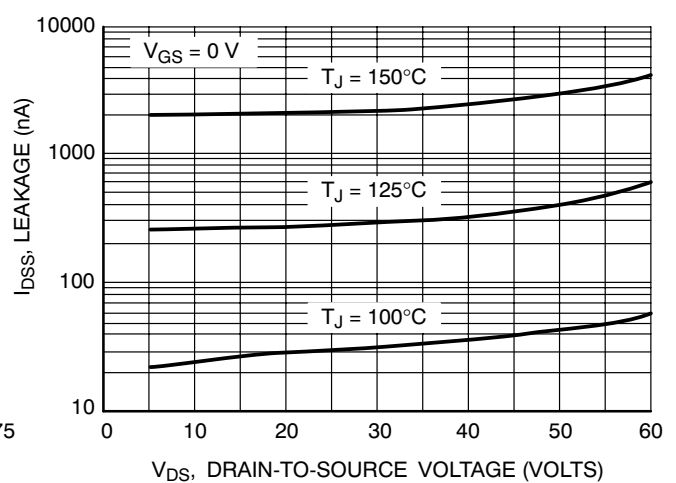
**Figure 3. On-Resistance vs. Drain Current**



**Figure 4. On-Resistance vs. Drain Current**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

# NTD32N06L

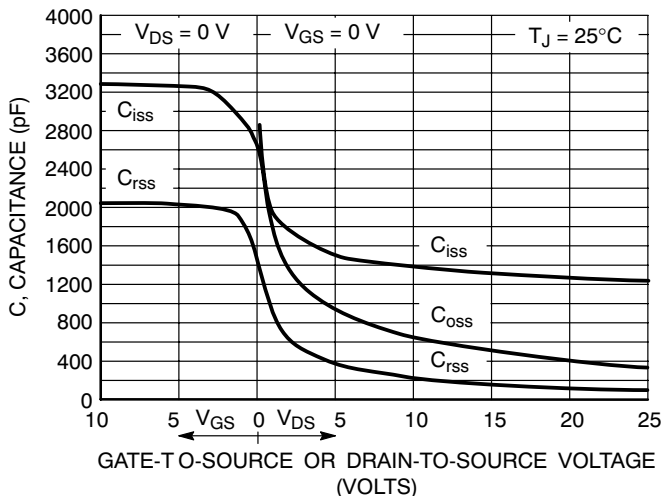


Figure 7. Capacitance Variation

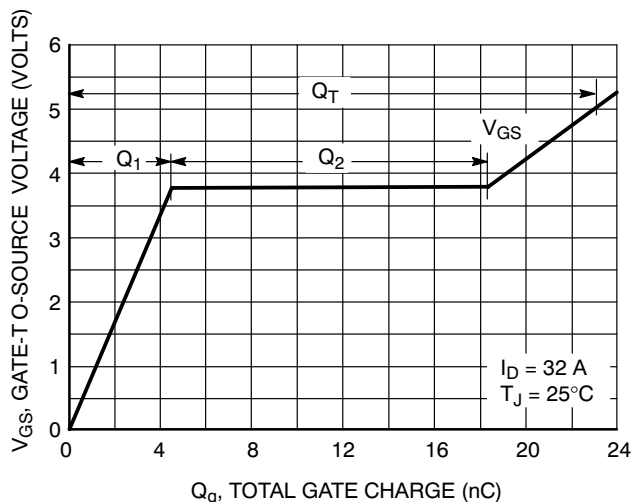


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

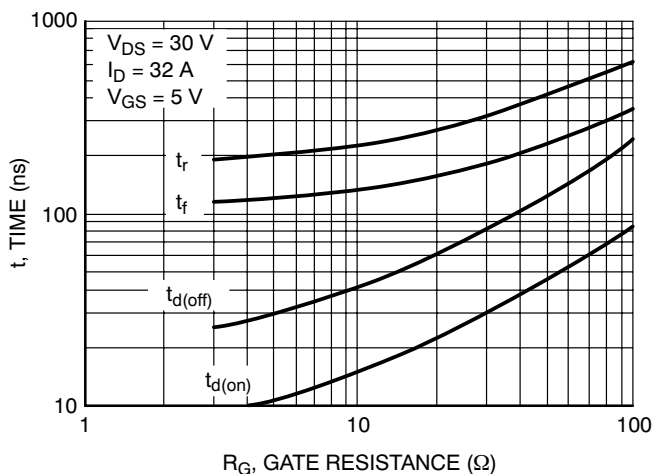


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

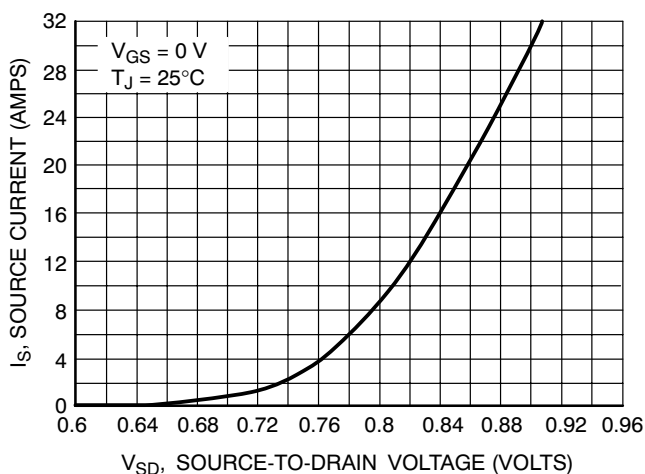


Figure 10. Diode Forward Voltage vs. Current

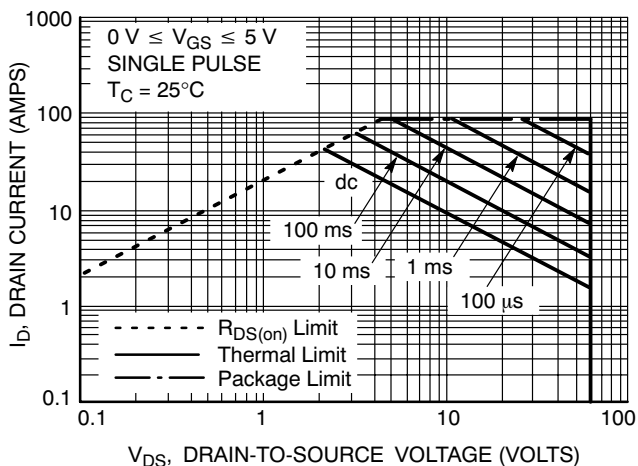


Figure 11. Maximum Rated Forward Biased Safe Operating Area

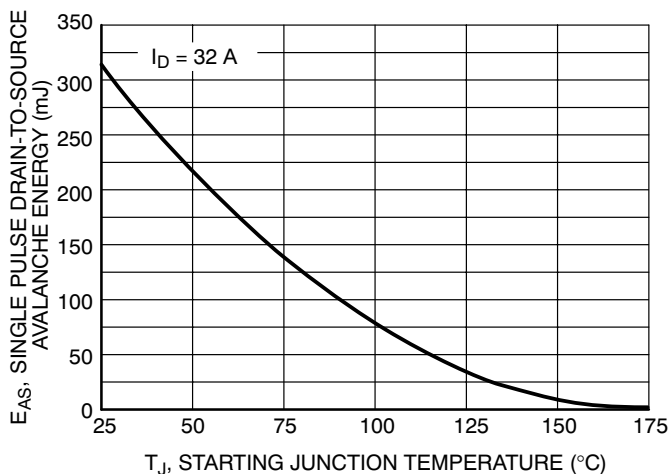


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

# NTD32N06L

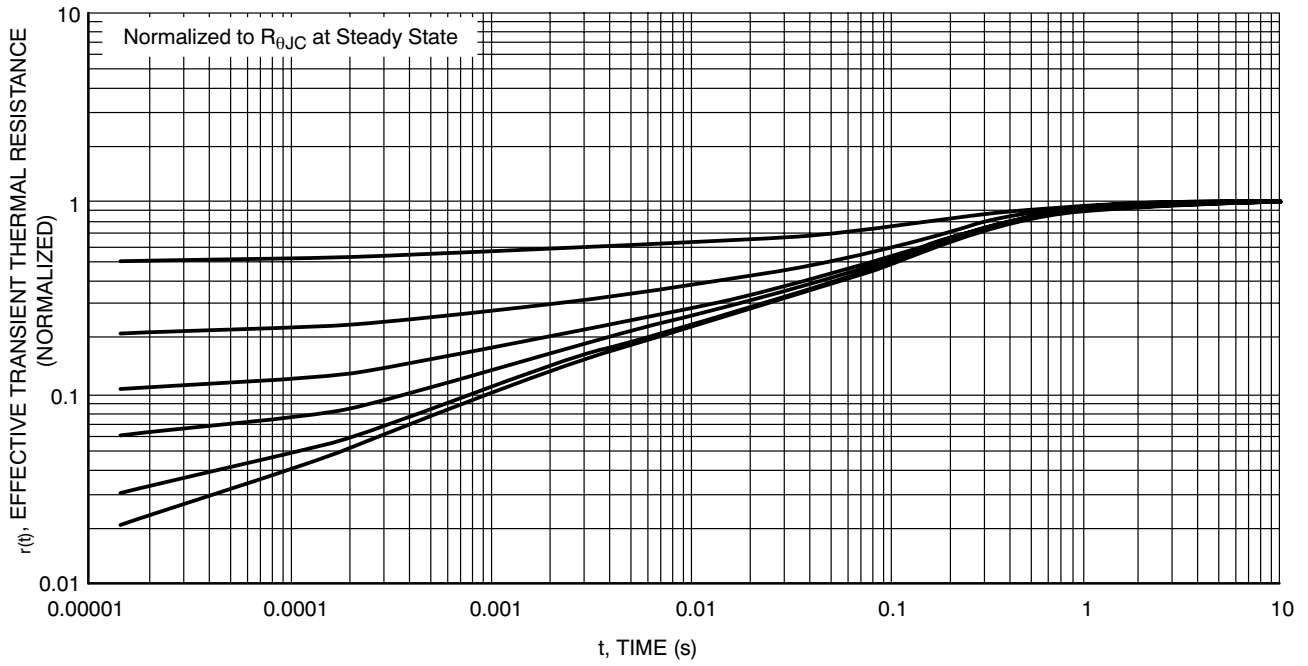


Figure 13. Thermal Response

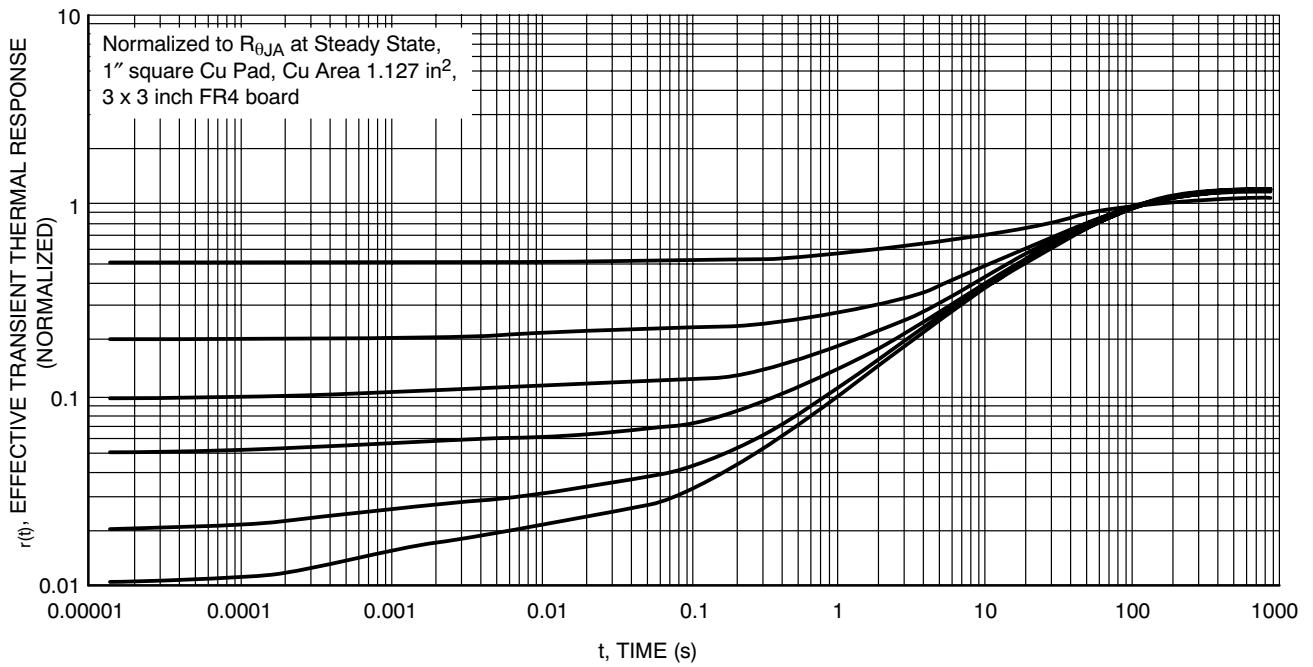
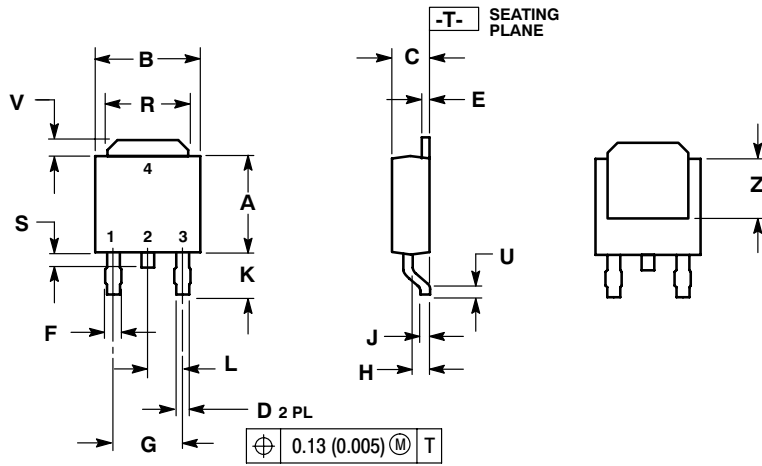


Figure 14. Thermal Response

# NTD32N06L

## PACKAGE DIMENSIONS

DPAK  
CASE 369C-01  
ISSUE O

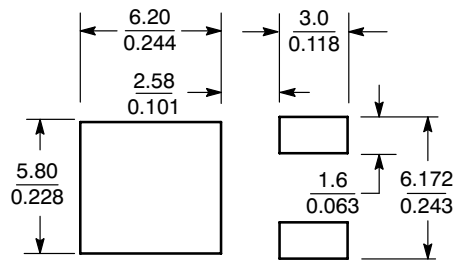


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC	4.58 BSC		
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC	2.29 BSC		
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

## SOLDERING FOOTPRINT\*



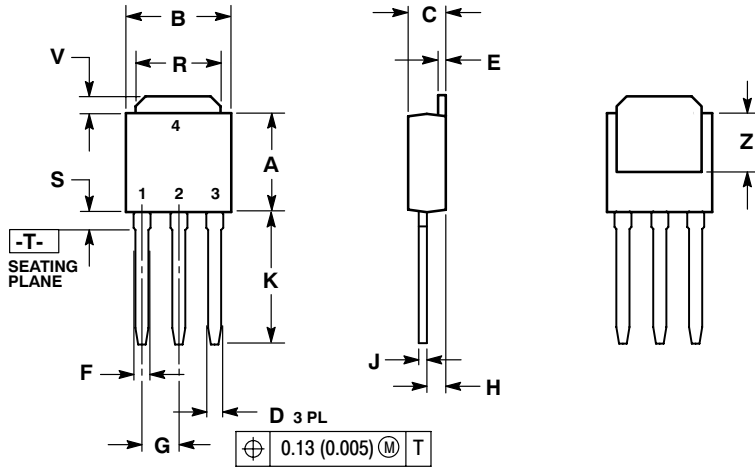
SCALE 3:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTD32N06L

## PACKAGE DIMENSIONS

DPAK  
CASE 369D-01  
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative