
Document Title

512Kx36 & 1Mx18-Bit Synchronous Burst SRAM

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	March. 17 . 1999	Preliminary
0.1	1. Update ICC & ISB values.	May. 27. 1999	Preliminary
0.2	1. Change tOE from 3.5ns to 4.0ns at -8 . 2. Change tOE from 3.5ns to 4.0ns at -9 . 3. Change tOE from 3.5ns to 4.0ns at -10 .	June. 22. 1999	Preliminary
0.3	1. Change ISB value from 130mA to 80mA at -8 . 2. Change ISB value from 120mA to 70mA at -9 . 3. Change ISB value from 120mA to 60mA at -10 .	Sep. 04. 1999	Preliminary
0.4	1. Change tCYC value from 12ns to 10ns at -9 .	Oct. 28. 1999	Preliminary
1.0	1. Final Spec Release.	Dec. 08. 1999	Final
2.0	1. Remove -10 bin (tCD=10ns)	Feb. 23. 2001	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

512Kx36 & 1Mx18 Synchronous SRAM

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A /119BGA(7x17 Ball Grid Array Package)

The K7B163625M and K7B161825M are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP and 119BGA package. Multiple power and ground pins are utilized to minimize ground bounce.

PARAMETER	Symbol	-85	-90	Unit
Cycle Time	tcyc	10	10	ns
Clock Access Time	tcd	8.5	9.0	ns
Output Enable Access Time	toE	4.0	4.0	ns

The block diagram illustrates the internal architecture of the 512Kx36, 1Mx18 memory array system. The components and their interconnections are as follows:

- Inputs:** CLK, LBO, ADV, ADSC, ADSP, CS1, CS2, GW, BW, WEx (x=a,b,c,d or a,b), OE, and ZZ.
- Control Register:** Receives CLK, LBO, ADV, and ADSC. It outputs to the Burst Control Logic and the Control Logic.
- Burst Control Logic:** Receives signals from the Control Register and the Address Register. It outputs to the Burst Address Counter and the Control Logic.
- Burst Address Counter:** Receives signals from the Burst Control Logic and the Address Register. It outputs A'0-A'1 to the 512Kx36, 1Mx18 Memory Array.
- Address Register:** Receives signals from the Burst Control Logic and the Address Register. It outputs A0-A18 or A0-A19 to the Address Register and the Control Logic.
- Control Logic:** Receives signals from the Control Register, Burst Control Logic, Address Register, and the 512Kx36, 1Mx18 Memory Array. It outputs to the Data-In Register and the Output Buffer.
- Data-In Register:** Receives signals from the Control Logic and the 512Kx36, 1Mx18 Memory Array. It outputs to the Output Buffer.
- Output Buffer:** Receives signals from the Control Logic and the Data-In Register. It outputs the final data to the DQ and DOP pins.

The output is labeled $DQa0 \sim DQd7$ or $DQa0 \sim DQb7$ and $DOPa \sim DOPd$ or $DOPa, DOPb$.

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100 Pin TQFP
(20mm x 14mm)

K7B163625M(512Kx36)

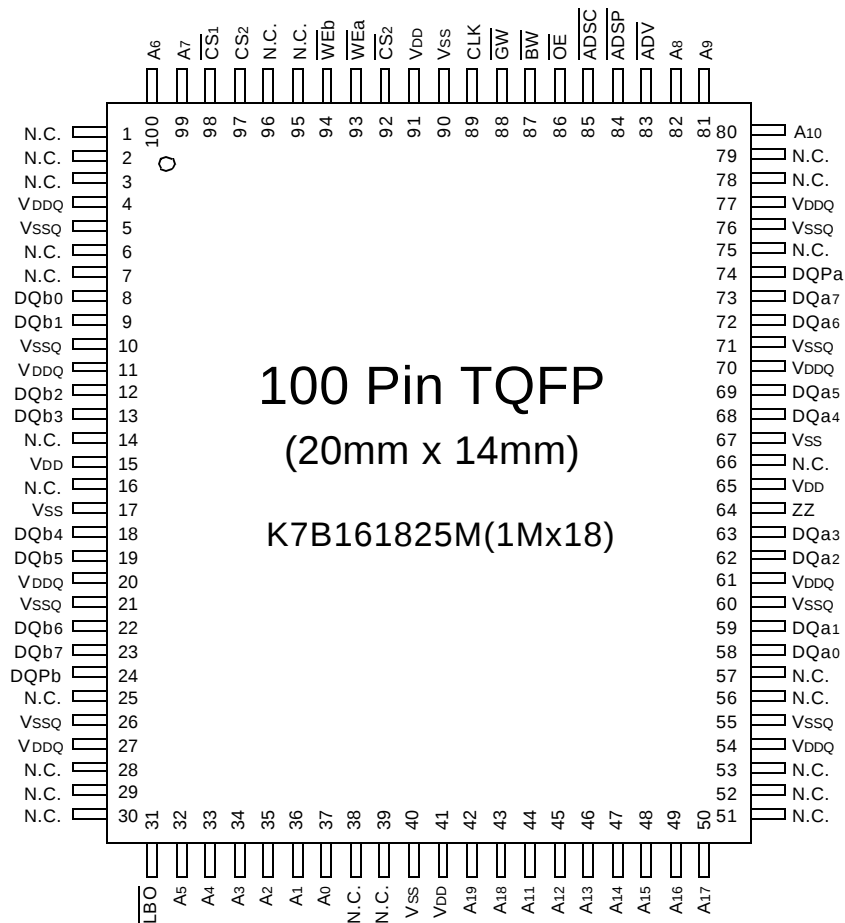
SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85			
CLK	Clock	89	DQa0-a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CS1	Chip Select	98	DQb0-b7		68,69,72,73,74,75,78,79
CS2	Chip Select	97	DQc0-c7		2,3,6,7,8,9,12,13
CS2	Chip Select	92	DQd0-d7		18,19,22,23,24,25,28,29
WEx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	DQP a-Pd		51,80,1,30
OE	Output Enable	86			
GW	Global Write Enable	88	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
BW	Byte Write Enable	87			
ZZ	Power Down Input	64	VSSQ	Output Ground	5,10,21,26,55,60,71,76
LBO	Burst Mode Control	31			



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PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29, 30,38,39,51,52,53,56,57, 66,75,78,79,95,96
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85			
CLK	Clock	89	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS1	Chip Select	98	DQb0 ~ b7		8,9,12,13,18,19,22,23
CS2	Chip Select	97	DQPa, Pb		74,24
CS2	Chip Select	92			
WEx(x=a,b)	Byte Write Inputs	93,94	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
OE	Output Enable	86		(2.5V or 3.3V)	
GW	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Notes : 1. A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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512Kx36 & 1Mx18 Synchronous SRAM

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7B163625M(512Kx36)

	1	2	3	4	5	6	7
A	VDDQ	A	A	$\overline{\text{ADSP}}$	A	A	VDDQ
B	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQPc	VSS	NC	VSS	DQPb	DQb
E	DQc	DQc	VSS	$\overline{\text{CS}}_1$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{\text{OE}}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{\text{WE}}_c$	$\overline{\text{ADV}}$	$\overline{\text{WE}}_b$	DQb	DQb
H	DQc	DQc	VSS	$\overline{\text{GW}}$	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	$\overline{\text{WE}}_d$	NC	$\overline{\text{WE}}_a$	DQa	DQa
M	VDDQ	DQd	VSS	$\overline{\text{BW}}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A ₁ *	VSS	DQa	DQa
P	DQd	DQPd	VSS	A ₀ *	VSS	DQPa	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	VDDQ	NC	NC	NC	NC	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A ₀ , A ₁	Burst Count Address	VSS	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller		
CLK	Clock	DQa	Data Inputs/Outputs
$\overline{\text{CS}}_1$	Chip Select	DQb	Data Inputs/Outputs
WEx	Byte Write Inputs	DQc	Data Inputs/Outputs
(x=a,b,c,d)		DQd	Data Inputs/Outputs
		DQPa~Pd	Data Inputs/Outputs
$\overline{\text{OE}}$	Output Enable		
$\overline{\text{GW}}$	Global Write Enable	VDDQ	Output Power Supply
BW	Byte Write Enable		(2.5V or 3.3V)
ZZ	Power Down Input		
$\overline{\text{LBO}}$	Burst Mode Control		

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119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7B161825M(1Mx18)

	1	2	3	4	5	6	7
A	VDDQ	A	A	$\overline{\text{ADSP}}$	A	A	VDDQ
B	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb	VSS	$\overline{\text{CS}}_1$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{\text{OE}}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{\text{WE}}_b$	$\overline{\text{ADV}}$	VSS	NC	DQa
H	DQb	NC	VSS	$\overline{\text{GW}}$	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	$\overline{\text{WE}}_a$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{\text{BW}}$	VSS	NC	VDDQ
N	DQb	NC	VSS	A ₁ *	VSS	DQa	NC
P	NC	DQPb	VSS	A ₀ *	VSS	NC	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VDDQ	NC	NC	NC	NC	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A ₀ ,A ₁	Burst Count Address	VSS	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller	DQa	Data Inputs/Outputs
CLK	Clock	DQb	Data Inputs/Outputs
$\overline{\text{CS}}_1$	Chip Select	DQPa-Pb	Data Inputs/Output
$\overline{\text{WE}}_x$	Byte Write Inputs		
(x=a,b)		VDDQ	Output Power Supply (2.5V or 3.3V)
$\overline{\text{OE}}$	Output Enable		
$\overline{\text{GW}}$	Global Write Enable		
$\overline{\text{BW}}$	Byte Write Enable		
ZZ	Power Down Input		
$\overline{\text{LBO}}$	Burst Mode Control		

K7B163625M K7B161825M

512Kx36 & 1Mx18 Synchronous SRAM

FUNCTION DESCRIPTION

The K7B163625M and K7B161825M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and $\overline{ZZ}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When $\overline{ZZ}$ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When $\overline{ZZ}$ returns to low, the SRAM normally operates after 2cycles of wake up time. $\overline{ZZ}$ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$ (or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$, and $\overline{WEd}$ are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$ (or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.

All byte write occurs by enabling $\overline{GW}$ (independent of $\overline{BW}$ and $\overline{WEx}$), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In K7B163625M, a 512Kx36 organization, $\overline{WEa}$ controls DQa0 ~ DQa7 and DQPa, $\overline{WEb}$ controls DQb0 ~ DQb7 and DQPb, $\overline{WEc}$ controls DQc0 ~ DQc7 and DQPc and $\overline{WEd}$ controls DQd0 ~ DQd7 and DQPd.

$\overline{CS1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBOPIN}$	HIGH	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{\text{LBO}}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE (x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

Notes : 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE (x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTES
L	X	X	X	WRITE ALL BYTES

Notes : 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

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ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	OE	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to VSS	VDDQ	VDD	V
Voltage on Input Pin Relative to VSS	VIN	-0.3 to 4.6	V
Voltage on I/O Pin Relative to VSS	VIO	-0.3 to VDDQ+0.5	V
Power Dissipation	PD	1.6	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O(0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	3.135	3.3	3.465	V
Ground	VSS	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	2.375	2.5	2.9	V
Ground	VSS	0	0	0	V

CAPACITANCE*(TA=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	7	pF
Output Capacitance	COUT	VOUT=0V	-	9	pF

*Note : Sampled not 100% tested.

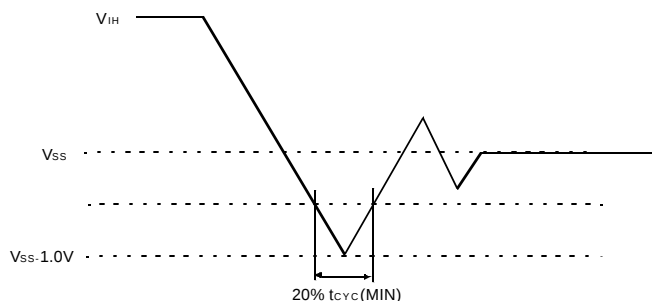
DC ELECTRICAL CHARACTERISTICS($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	I _{IL}	V _{DD} =Max ; V _{IN} =V _{SS} to V _{DD}		-2	+2	μA	
Output Leakage Current	I _{OL}	Output Disabled, V _{out} =V _{SS} to V _{DDQ}		-2	+2	μA	
Operating Current	I _{CC}	Device Selected, I _{OUT} =0mA, ZZ≤V _{IL} , Cycle Time ≥ t _{CYC} Min	-85	-	350	mA	1,2
			-90	-	300		
Standby Current	I _{SB}	Device deselected, I _{OUT} =0mA, ZZ≤V _{IL} , f=Max, All Inputs≤0.2V or ≥ V _{DD} -0.2V	-85	-	80	mA	
			-90	-	70		
	I _{SB1}	Device deselected, I _{OUT} =0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V _{DD} -0.2V or 0.2V)	-	30	mA		
	I _{SB2}	Device deselected, I _{OUT} =0mA, ZZ≥V _{DD} -0.2V, f=Max, All Inputs≤V _{IL} or ≥V _{IH}	-	30	mA		
Output Low Voltage(3.3V I/O)	V _{OL}	I _{OL} =8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V _{OH}	I _{OH} =-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V _{OL}	I _{OL} =1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V _{OH}	I _{OH} =-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V _{IL}			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V _{IH}			2.0	V _{DD} +0.5**	V	3
Input Low Voltage(2.5V I/O)	V _{IL}			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V _{IH}			1.7	V _{DD} +0.5**	V	3

Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.

2. Data states are all zero.

3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V



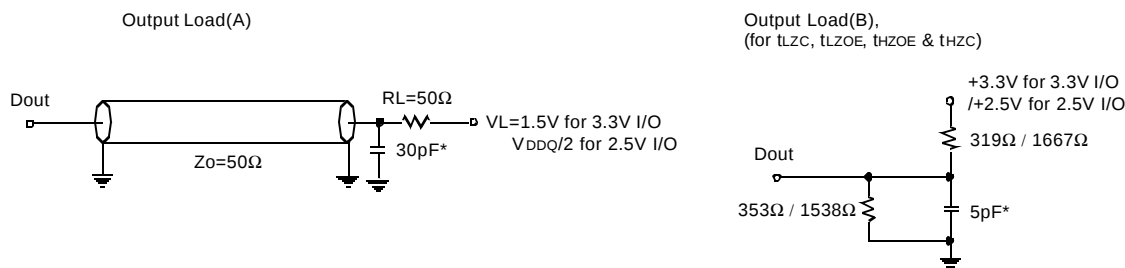
TEST CONDITIONS

($V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=3.3V+0.165V/-0.165V$ or $V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=2.5V+0.4V/-0.125V$, $T_A=0$ to $70^{\circ}C$)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V _{DDQ} /2
Output Load	See Fig. 1

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512Kx36 & 1Mx18 Synchronous SRAM



* Including Scope and Jig Capacitance

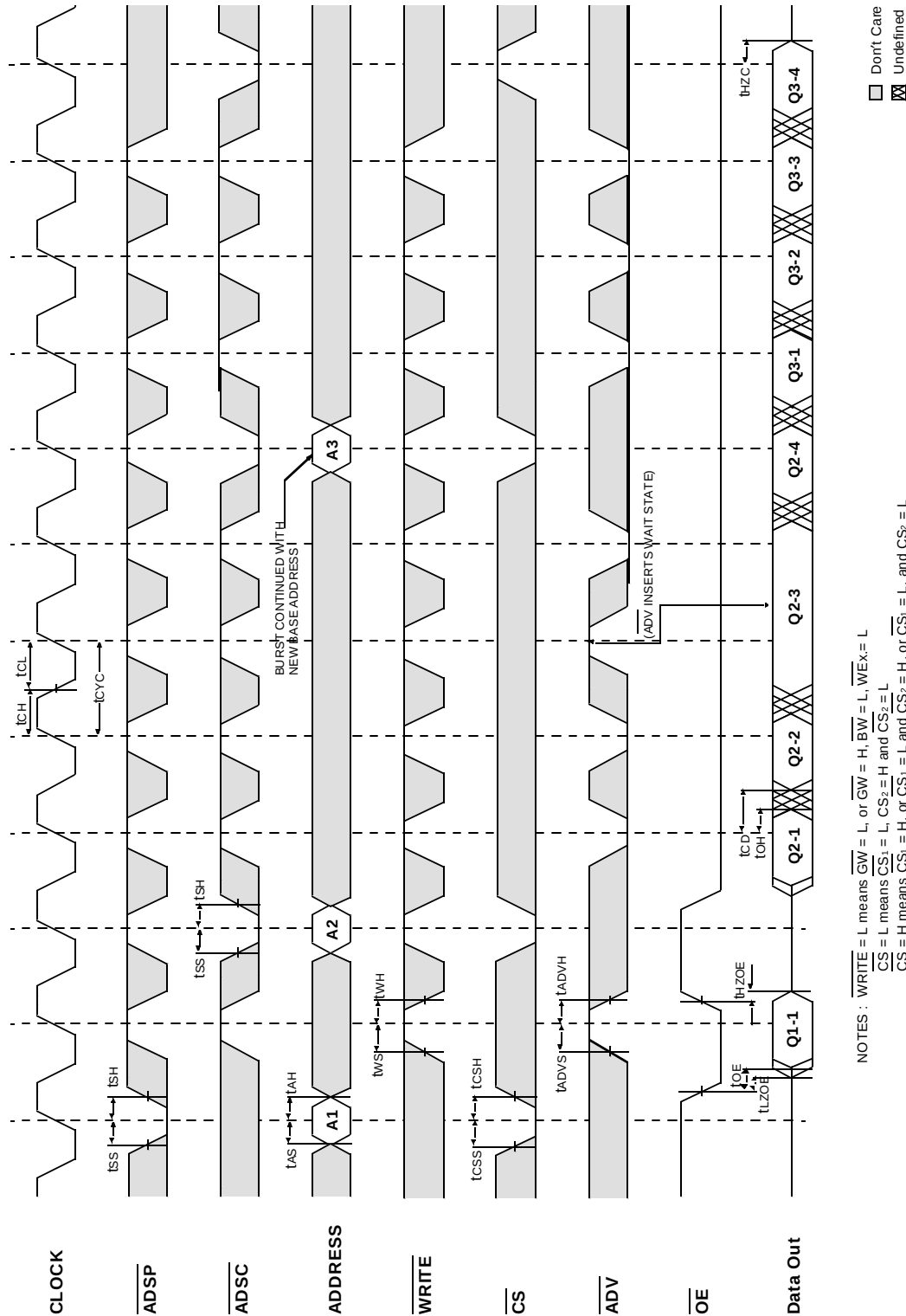
Fig. 1

AC TIMING CHARACTERISTICS(VDD=3.3V+0.165V/-0.165V, TA=0°C to +70°C)

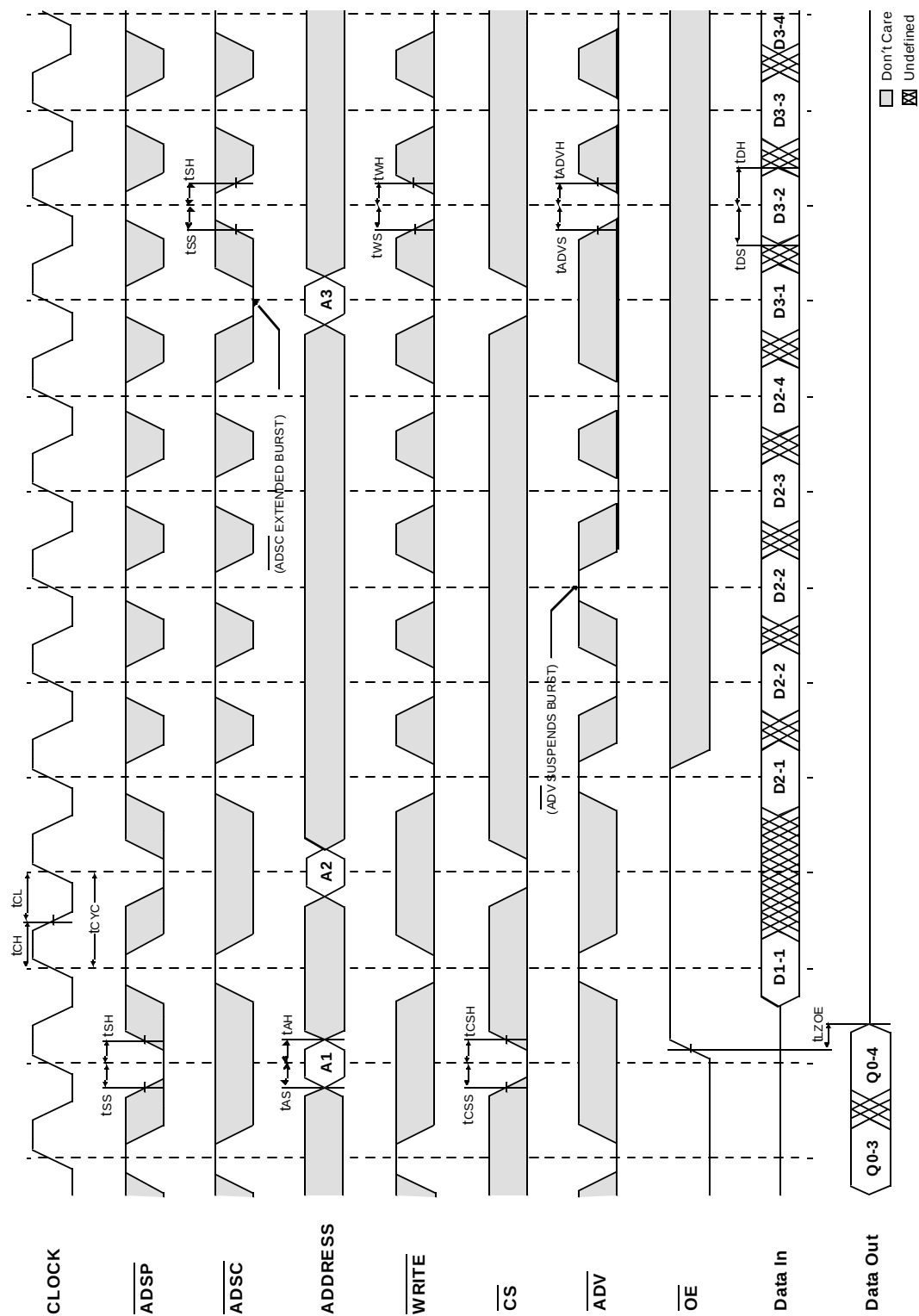
PARAMETER	SYMBOL	-85		-90		UNIT
		MIN	MAX	MIN	MAX	
Cycle Time	tCYC	10	-	10	-	ns
Clock Access Time	tCD	-	8.5	-	9.0	ns
Output Enable to Data Valid	tOE	-	4.0	-	4.0	ns
Clock High to Output Low-Z	tLZC	2.5	-	2.5	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	-	5.0	-	5.0	ns
Clock High Pulse Width	tCH	3.0	-	3.0	-	ns
Clock Low Pulse Width	tCL	3.0	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$)	tWS	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

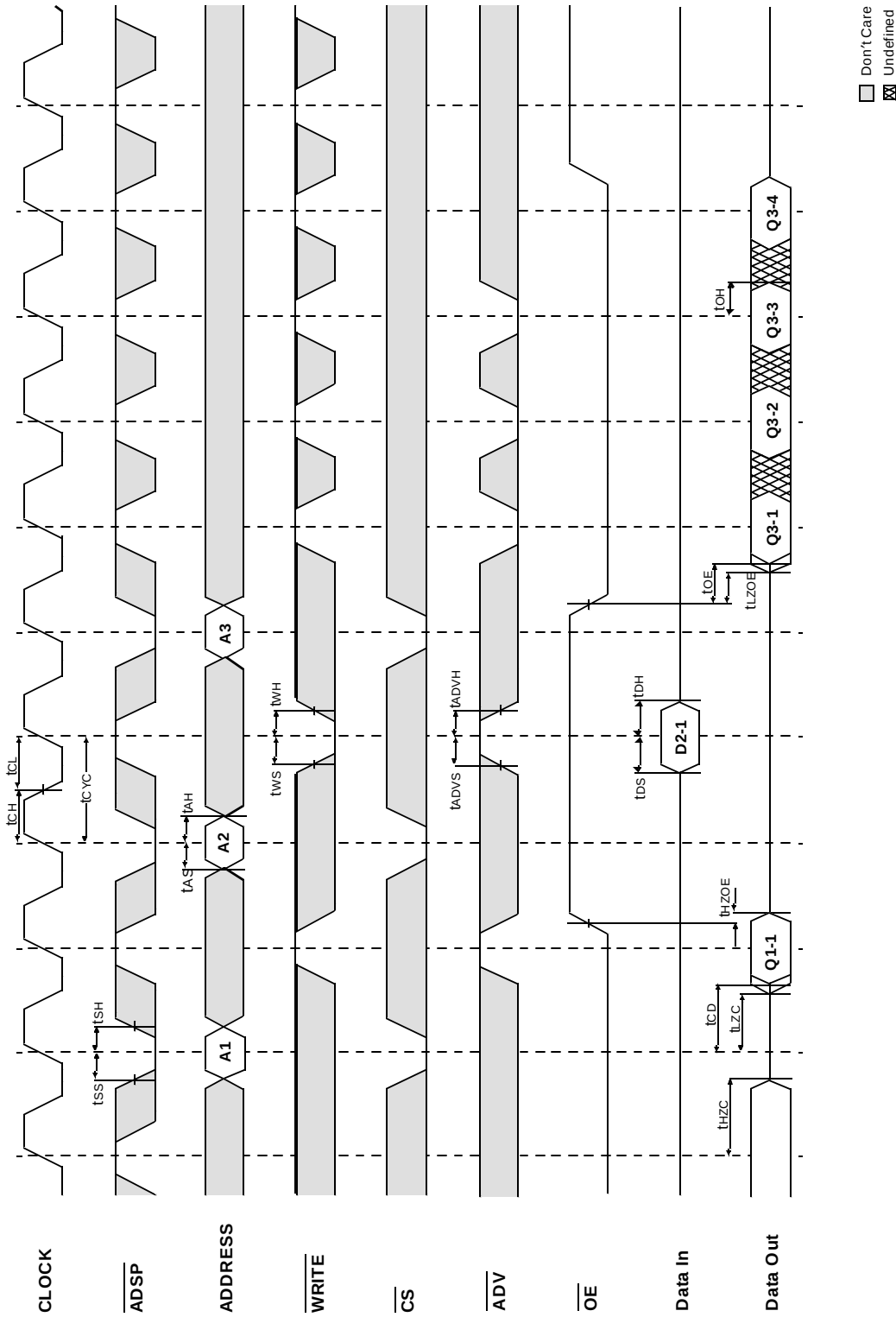
TIMING WAVEFORM OF READ CYCLE

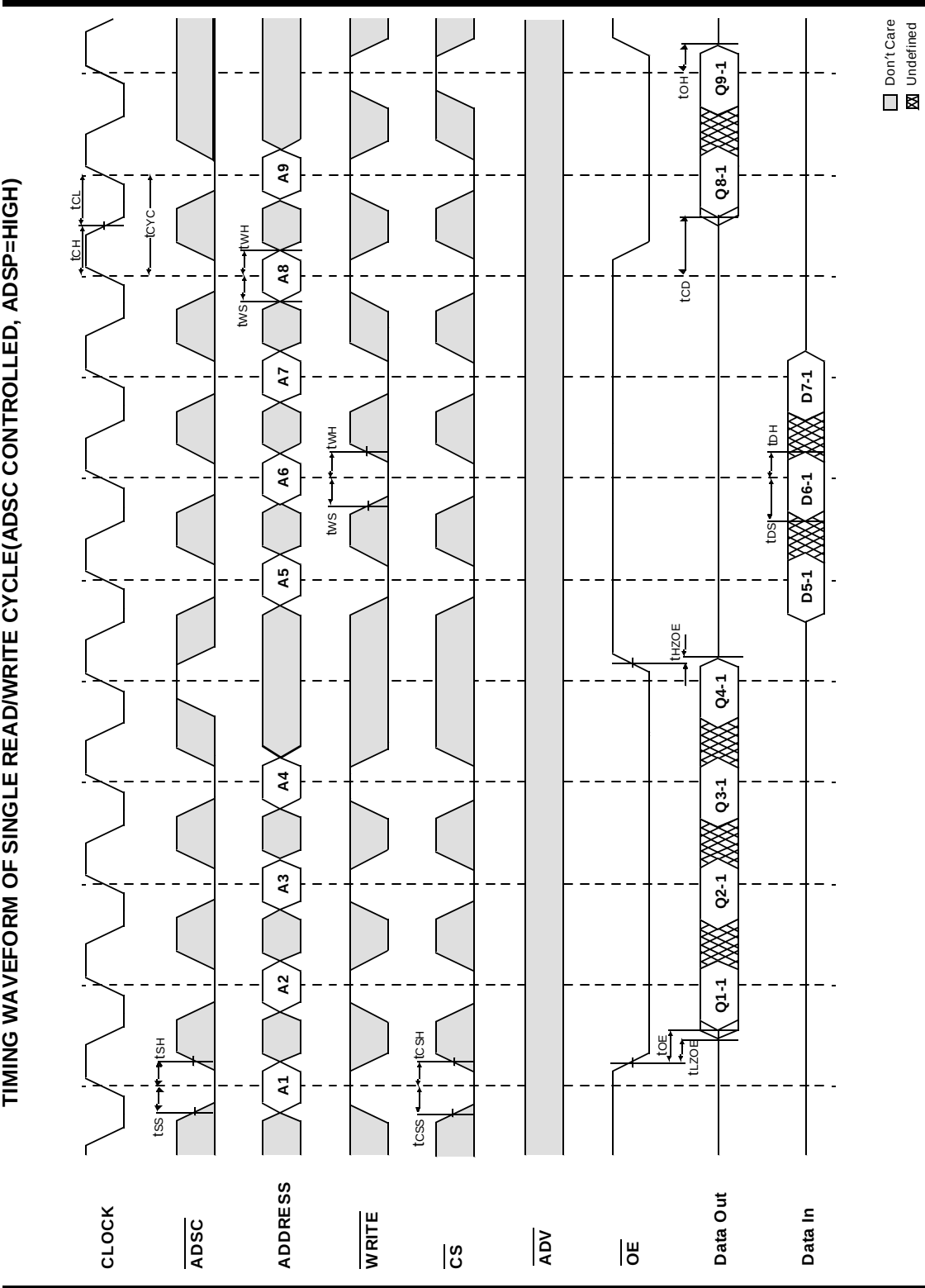


TIMING WAVEFORM OF WRTE CYCLE

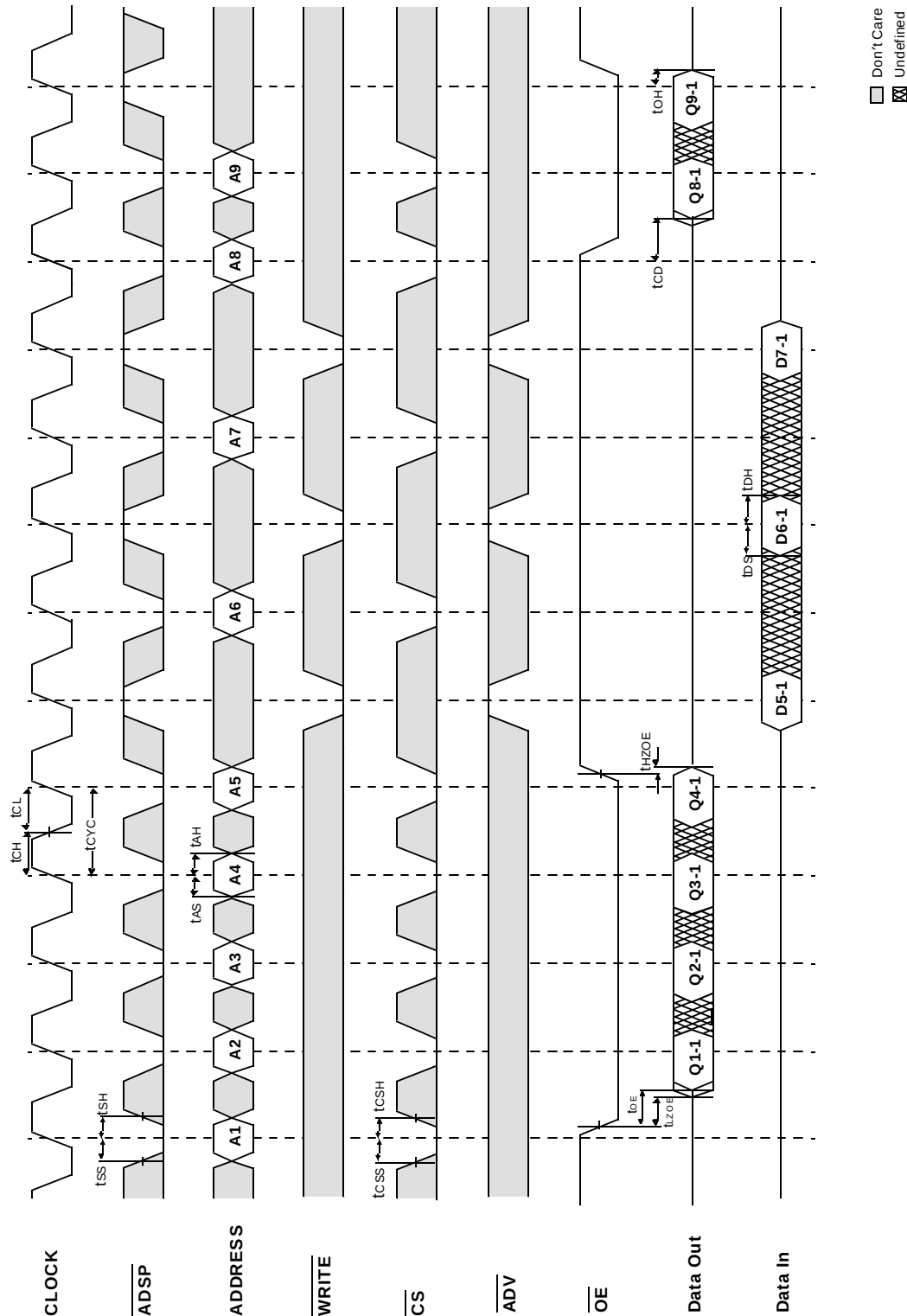


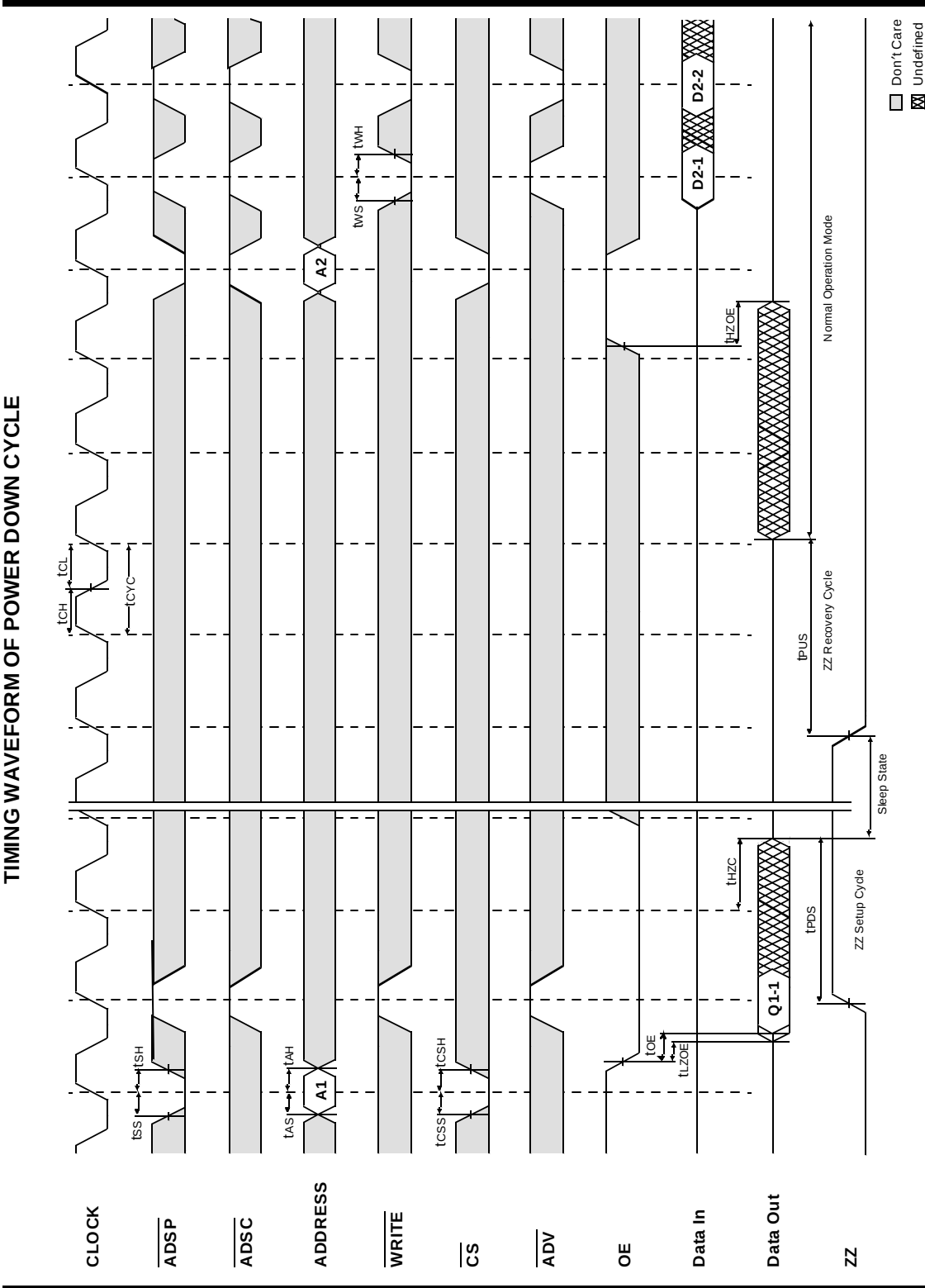
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)





TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, $\overline{\text{ADSC}}=\text{HIGH}$)

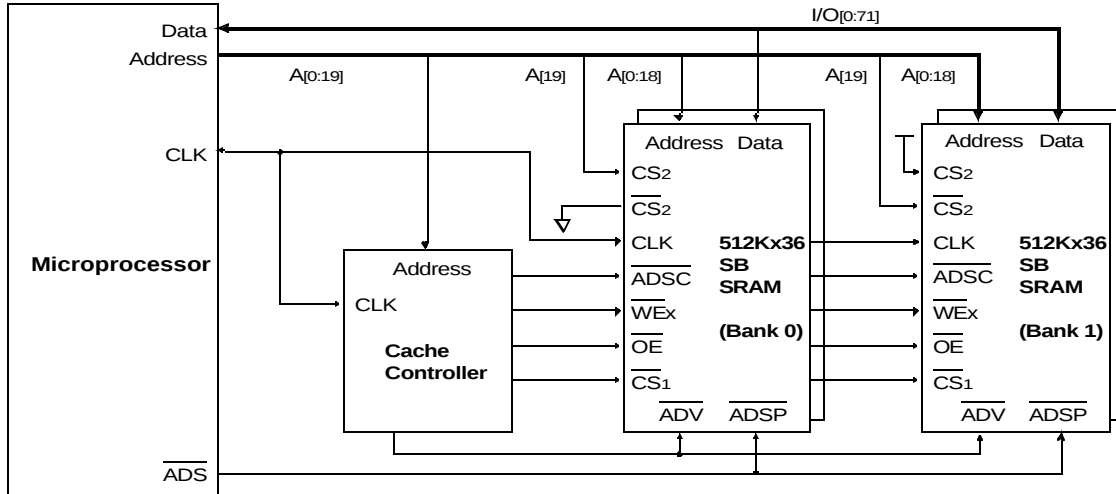




APPLICATION INFORMATION

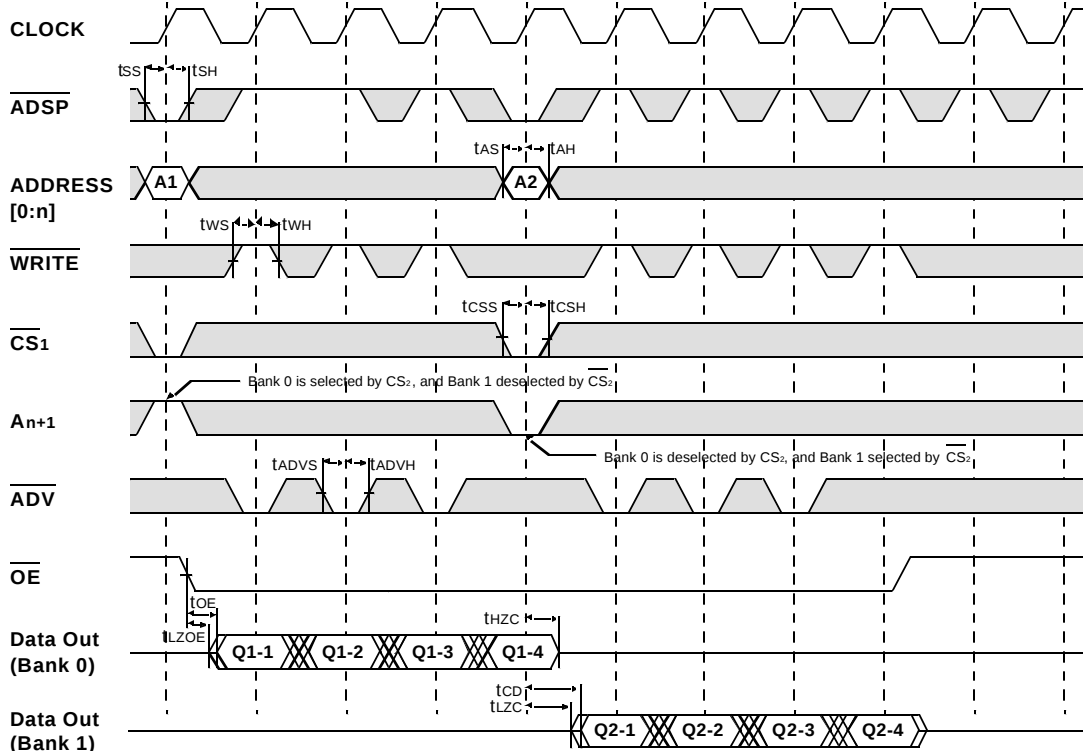
DEPTH EXPANSION

The Samsung 512Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



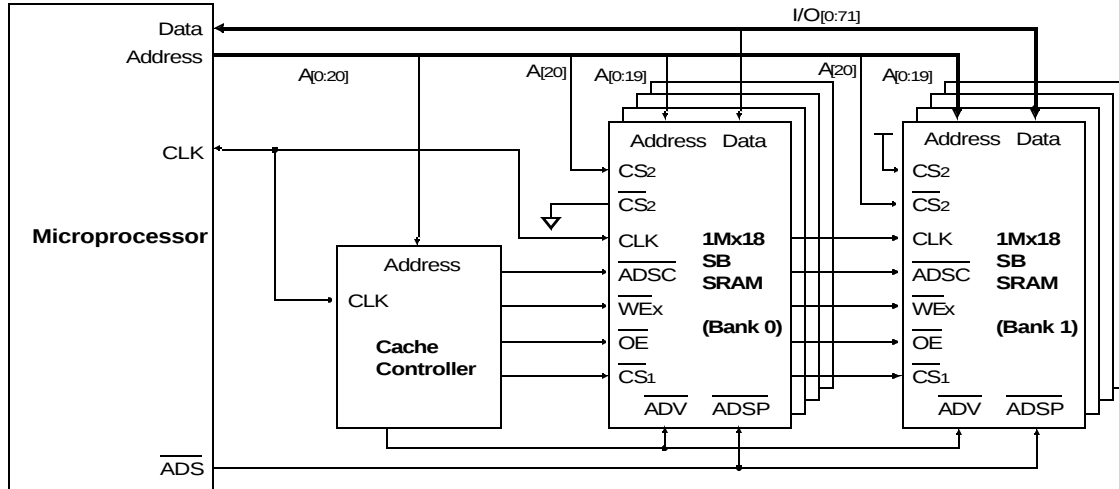
*Notes : n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth

□ Don't Care ⊗ Undefined

APPLICATION INFORMATION

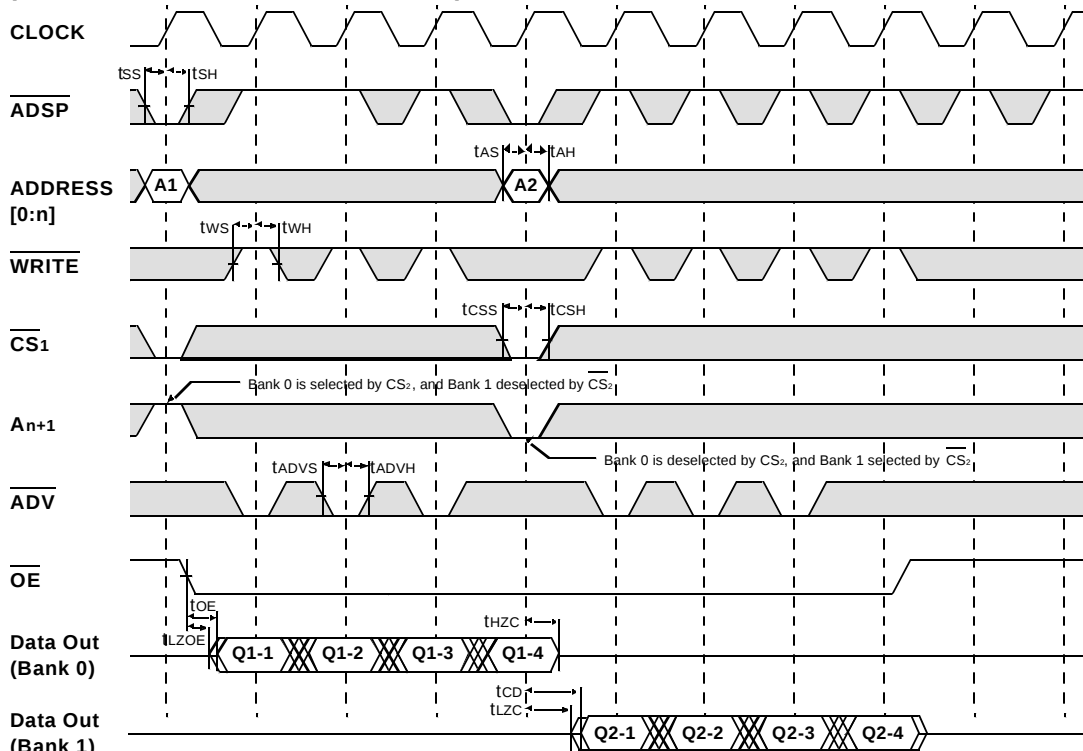
DEPTH EXPANSION

The Samsung 1Mx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



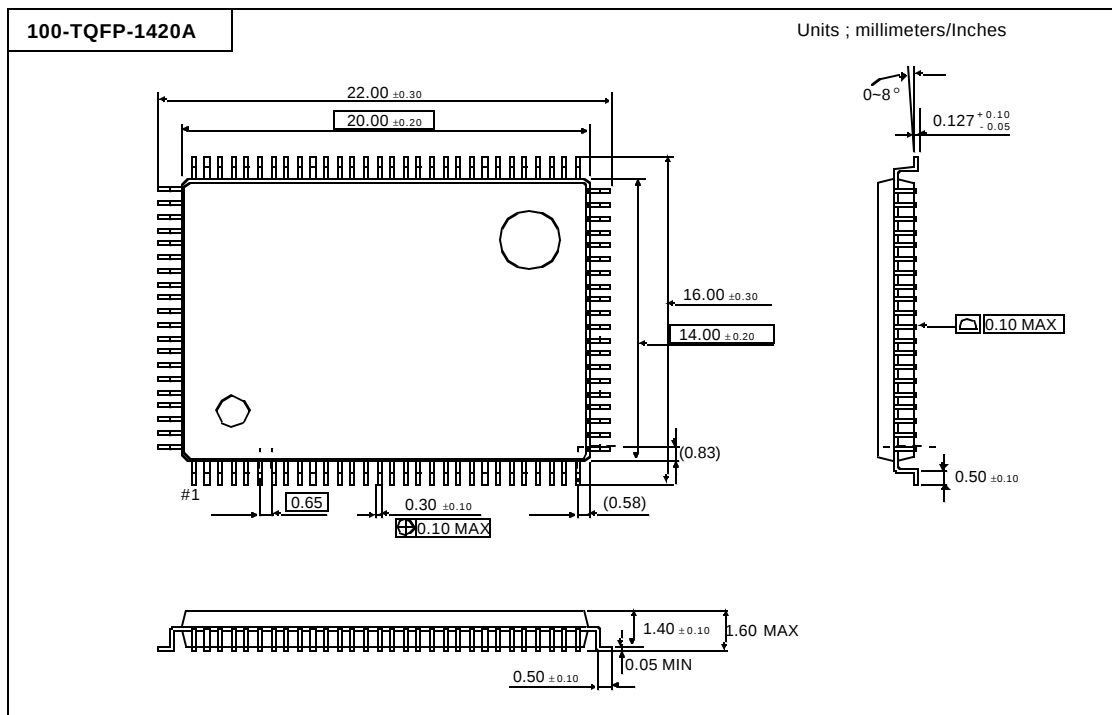
*Notes : n = 14 32K depth, 15 64K depth
16 128K depth, 17 256K depth
18 512K depth, 19 1M depth
20 2M depth

□ Don't Care ⊗ Undefined

K7B163625M
K7B161825M

512Kx36 & 1Mx18 Synchronous SRAM

PACKAGE DIMENSIONS



K7B163625M
K7B161825M

512Kx36 & 1Mx18 Synchronous SRAM

119BGA PACKAGE DIMENSIONS

