Integrated
Circuit
Systems, Inc.

ICS9158-04

Frequency Generator and Integrated Buffer

General Description

The **ICS9158-04** is a low cost frequency generator designed specifically for desktop and notebook PC applications. Up to six copies of the CPU clock are available, and five or six copies of the BUS clock are available depending on the status of the frequency select pins, which eliminates the need for an external buffer.

Each high drive (25mA) output is capable of driving a 30pF load and has a typical duty cycle of 50/50. The clock outputs are skew controlled to within ±250ps.

The **ICS9158-04** makes a gradual transition between frequencies, so that it meets the Intel cycle-to-cycle timing specification for 486 and Pentium™ systems.

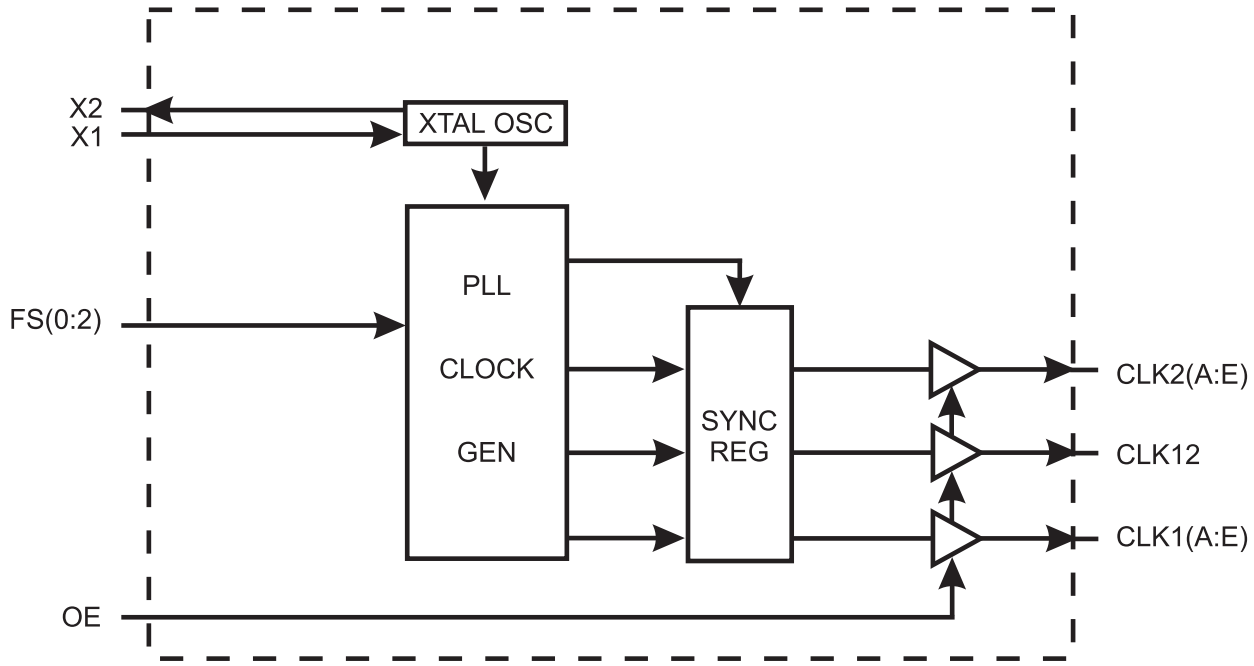
Features

- 11 skew-free, high drive CPU/BUS clocks
- Up to 66 MHz at 3.3V
- ±250ps skew between all outputs
- Outputs can drive up to 30pF load and 25mA
- 50±10% duty cycle
- Compatible with 486 and Pentium CPUs
- Selectable 5/6 or 6/5 CPU/BUS output ratio
- On-chip loop filter components
- 3.0V - 5.5V supply range
- 24-pin SOIC package

Applications

- Ideal for RISC or CISC systems such as 486, Pentium, PowerPC,™ etc., requiring multiple CPU and BUS clocks.

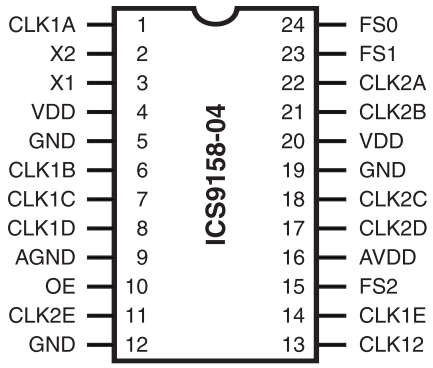
Block Diagram



Pentium is a trademark of Intel Corporation.
PowerPC is a trademark of Motorola Corporation.

NOTE: THIS DATA SHEET, ICS9158-04, IS AN ADDENDUM TO THE EXISTING ICS9158 DATA SHEET. ALL INFORMATION IN THIS DATA SHEET SUPERSEDES THE DATA FOUND IN THE ORIGINAL ICS9158 DATA SHEET.

Pin Configuration



24-Pin SOIC

Pin Description

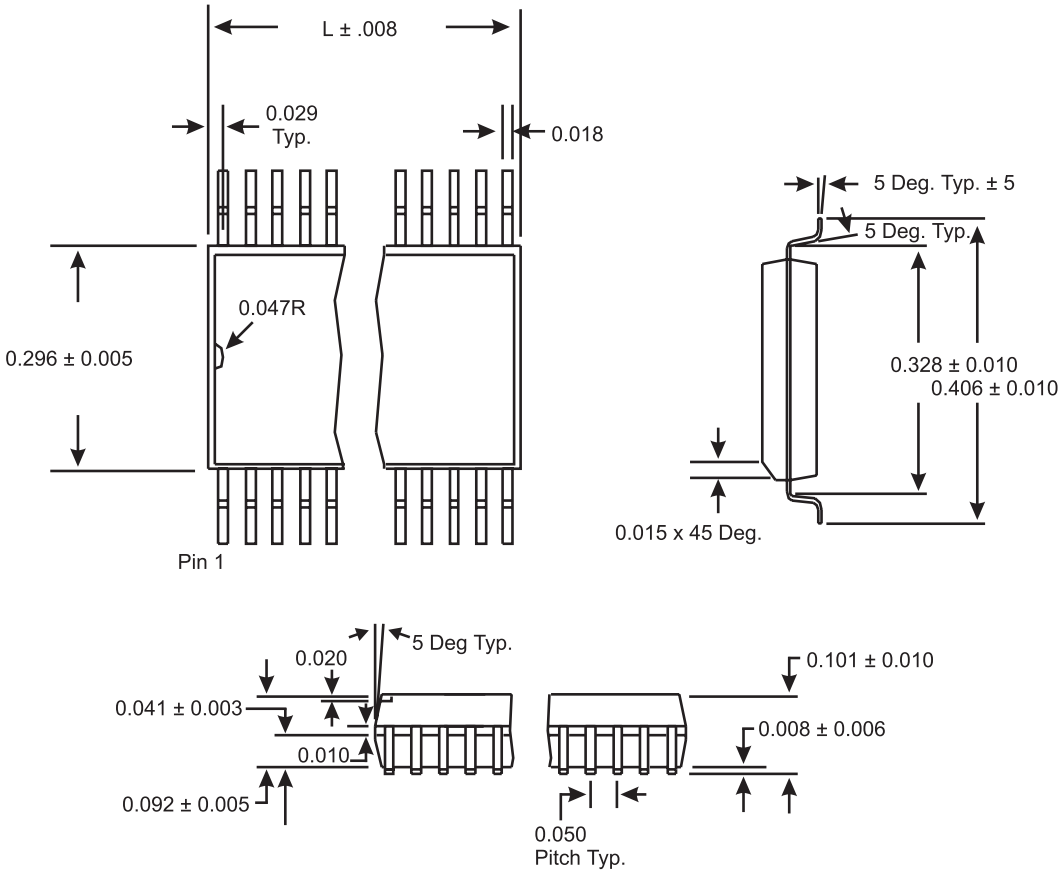
PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	CLK1A	OUT	CPU clock output.
2	X2	OUT	Crystal connection output, which includes output crystal load capacitance.
3	X1	IN	Crystal connection input, which includes crystal load capacitance and feedback bias for a nominal 14.31818 MHz parallel-resonance 12pF crystal.
4	VDD	PWR	Digital POWER SUPPLY.
5	GND	PWR	Digital GROUND.
6	CLK1B	OUT	CPU clock output.
7	CLK1C	OUT	CPU clock output.
8	CLK1D	OUT	CPU clock output.
9	AGND	PWR	ANALOG GROUND.
10	OE	IN	OUTPUT ENABLE. Tristates all outputs when low.*
11	CLK2E	OUT	2X CPU clock output.
12	GND	PWR	Digital GROUND.
13	CLK12	OUT	CPU clock output.
14	CLK1E	OUT	CPU clock output.
15	FS2	OUT	CPU clock frequency select 2.*
16	AVDD	PWR	ANALOG power supply.
17	CLK2D	OUT	2X CPU clock output.
18	CLK2C	OUT	2X CPU clock output.
19	GND	PWR	Digital GROUND.
20	VDD	PWR	Digital POWER SUPPLY.
21	CLK2B	OUT	2X CPU clock output.
22	CLK2A	OUT	2X CPU clock output.
23	FS1	IN	CPU clock frequency select #1.*
24	FS0	IN	CPU clock frequency select #0.*

* Input pin has internal pull-up to VDD.

Functionality

VDD=5V±10% or 3.3V±10%, TEMP=0-70°C

OE	FS2	FS1	FS0	CLK2 (MHz)	X1, X2 (MHz)	CLK2(A:E) (MHz)	CLK1(A:E) (MHz)	CLK12 (MHz)
1	0	0	0	14/6 x X1	14.318	33.3	16.6	33.3
1	0	0	1	14/4 x X1	14.318	50	25	50
1	0	1	0	14/3 x X1	14.318	66.6	33.3	66.6
1	0	1	1	42/10 x X1	14.318	60	30	60
1	1	0	0	14/6 x X1	14.318	33.3	16.6	16.6
1	1	0	1	14/4 x X1	14.318	50	25	25
1	1	1	0	14/3 x X1	14.318	66.6	33.3	33.3
1	1	1	1	42/10 x X1	14.318	60	30	30
0	X	X	X	--	14.318	Tristate	Tristate	Tristate



LEAD COUNT	24L
DIMENSION L	0.604

24 Lead SOIC

Ordering Information

ICS9158-04M

Example:

ICS XXXX-PPP M

Package Type
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device