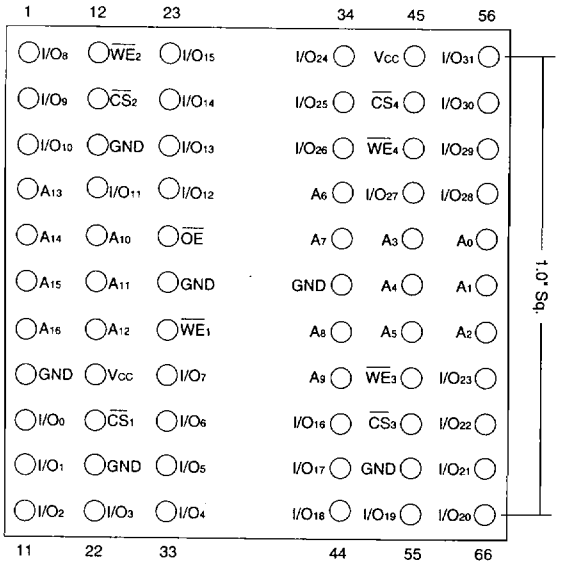


FIGURE 1 — Pin Configuration

I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

Pin Description

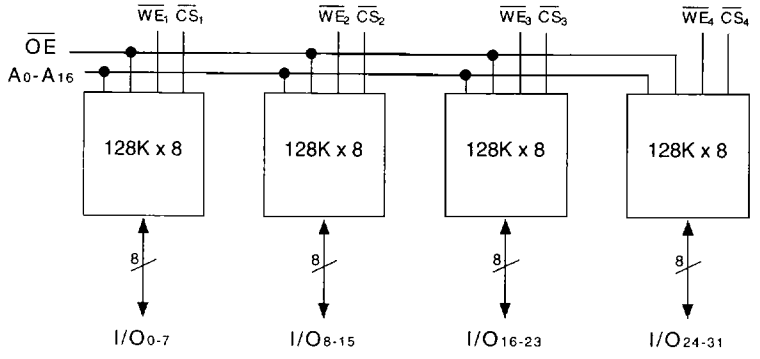


FIGURE 2 — Block Diagram

WE-128K32-XHX

4 Megabit CMOS EEPROM Module

FEATURES

- **Access Time of 150nS and 200nS**
- **66-pin, PGA Type, 1.185 inch square HIP, Hermetic Ceramic Package**
- **User Configurable as 128Kx32, 256Kx16 or 512Kx8**
- **Commercial, Industrial and Military Temperature Ranges**
- **Low Power CMOS, 10mA Standby Typical**
- **Automatic Page Write Operation**
- **Page Write Cycle Time: 10 mS Max.**
- **Data Polling for End of Write Detection**
- **Hardware and Software Data Protection**
- **TTL Compatible Inputs and Outputs**
- **5 Volt Power Supply**
- **Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation**

DESCRIPTION

The White Technology WE-128K32-XHX is a 4 megabit CMOS EEPROM module organized as 128K words by 32 bits, 256K x 16 or 512K x 8. The module is constructed on a multilayer ceramic substrate, hermetically sealed, with a welded metal cover, on a hex-in-line package (HIP) utilizing four 128K x 8 EEPROM devices.

This device is part of White Technology's "WHIP" family of memory subsystems. These modules are compatible with most 66-pin HIP packaged EEPROM, SRAM and Flash memory modules.

The WE-128K32-XHX is available with access time of 150nS over the commercial and military temperature ranges.

ABSOLUTE MAXIMUM RATINGS*

Rating	Symbol	Industrial	Military	Unit
Operating Temperature	T_A	-40 to +85	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +125	-65 to +150	°C
Signal Voltage Relative to GND	V_G	-0.6 to +6.25	-0.6 to +6.25	V

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0-A16	Mode	Data I/O	Device Current
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data Out	Active
L	H	L	Stable	Write	Data In	Active
X	H	X	X	Out Disable	High Z	Active
X	X	H	X	Write Inhibit		Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(@ T_A = 25°C)

Parameter	Symbol	Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	30	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	30	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	-150		-200		Unit
			Min.	Max.	Min.	Max.	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}		80		80	µA
Output Leakage Current	I_{LOx32}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		20		20	µA
Operating Supply Current x 32 Mode	I_{CCx32}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		250		200	mA
Operating Supply Current x 16 Mode	I_{CCx16}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		160		125	mA
Operating Supply Current x 8 Mode	I_{CCx8}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		80		70	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		5		5	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		0.45		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -400µA	2.4		2.4		V

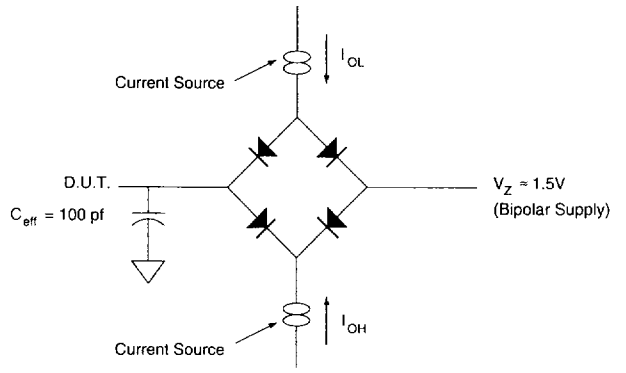


FIGURE 3 — AC Test Circuit

AC TEST CONDITIONS

Parameter	Typ.	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Load Capacitance	100	pF

Notes:

V_Z is programmable from -2V to +7V

I_{OL} & I_{OH} programmable from 0 to 16mA

Tester Impedance Z_0 = 75 Ω

V_Z is typically the midpoint of V_{OH} and V_{OL} (i.e. (2.4 + 0.4)/2 = 1.4V)

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE Tester Includes Jig Capacitance

WRITE

A write cycle is initiated when $\overline{OE}$ is high and a low pulse is on $\overline{WE}$ or $\overline{CS}$ with $\overline{CS}$ or $\overline{WE}$ low. The address is latched on the falling edge of $\overline{CS}$ or $\overline{WE}$ whichever occurs last. The data is latched by the rising edge of $\overline{CS}$ or $\overline{WE}$, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 4 and 5 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the $\overline{CS}$ line low. Write enable consists of setting the $\overline{WE}$ line low. The write cycle begins when the last of either $\overline{CS}$ or $\overline{WE}$ goes low.

The $\overline{WE}$ line transition from high to low also initiates an internal 150 µSec delay timer to permit page mode operation. Each subsequent $\overline{WE}$ transition from high to low that occurs before the completion of the 150 µSec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Min.	Max.	Unit
WRITE CYCLE				
Write Cycle Time, TYP = 6 mS	t_{WC}		10	mS
Address Set-up Time	t_{AS}	0		nS
Write Pulse Width ($\overline{WE}$ or $\overline{CS}$)	t_{WP}	150		nS
Chip Select Set-up Time	t_{CS}	0		nS
Address Hold Time	t_{AH}	100		nS
Data, $\overline{OE}$ Hold Time	t_{DH}	0		nS
Chip Select Hold Time	t_{CH}	0		nS
Data Set-up Time	t_{DS}	100		nS
Output Enable Set-up Time	t_{OES}	10		nS
Output Enable Hold Time	t_{OEH}	10		nS

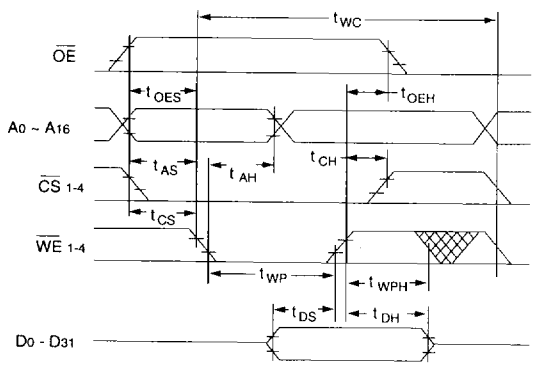


FIGURE 4 – Write Waveforms – $\overline{WE}$ Controlled

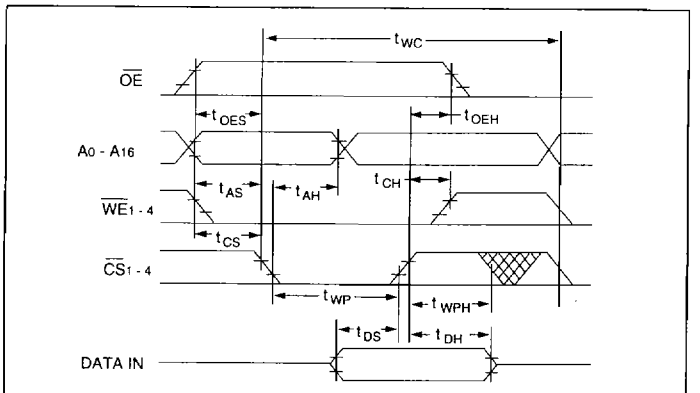


FIGURE 5 – Write Waveforms – $\overline{CS}$ Controlled

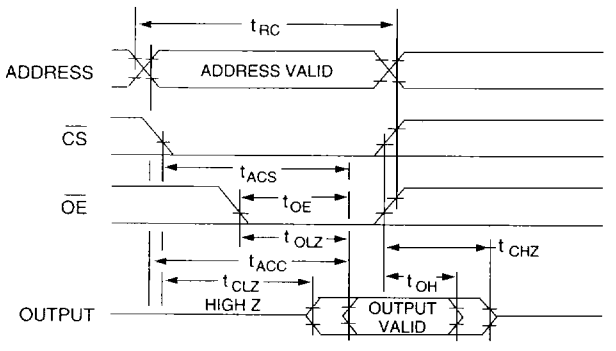
READ

The WE-128K32-XHX stores data at the memory location determined by the address pins. When $\overline{CS}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, this data is present on the outputs. When $\overline{CS}$ and $\overline{OE}$ are high, the outputs are in a high impedance state. This 2 line control prevents bus contention.

AC READ CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Sym	-150		-200		Unit
READ CYCLE		**Min**	**Max**	**Min**	**Max**	
Read Cycle Time	tRC	150		200		nS
Address Access Time	tACC		150		200	nS
$\overline{CS}$ Access Time	tACS		150		200	nS
Output Hold from Add. Change, $\overline{OE}$ or $\overline{CS}$	tOH	0		0		nS
Output Enable to Output Valid	tOE	0	85	0	125	nS
Chip Select to Output in Low Z	tCLZ	0		0		nS
Chip Select to Output in High Z	tCHZ		70		150	nS
Output Enable to Output in Low Z	tOLZ	0		0		nS



Notes: 1) $\overline{OE}$ may be delayed up to t_{ACS} - t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{OE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.

2) t_{CHZ}, t_{OHZ} are specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first (C_L = 5 pF).

3) All I/O transitions are measured ±200 mV from steady state with loading as specified in "Load Test Circuits."

FIGURE 6 – Read Waveforms

DATA POLLING

The WE-128K32-XHX offers a data polling feature which allows a faster method of writing to the device. Figure 7 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on I/07. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

DATA POLLING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Min.	Max.	Unit
Write Start	t_{DW}	150		nS
$\overline{OE}$ Hold Time	t_{OEH}	0		nS
$\overline{OE}$ To Output Delay	t_{OE}		150	nS
Write Cycle Time	t_{WC}		10	mS

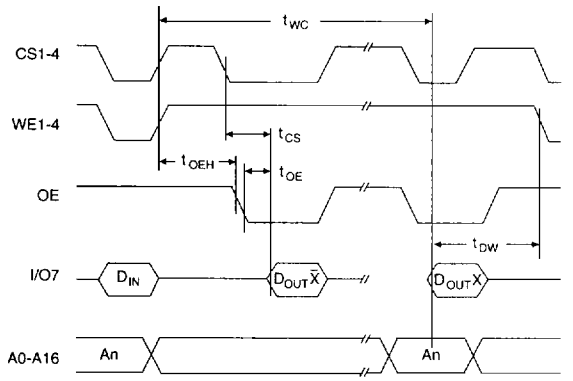


FIGURE 7 – Data Polling Waveforms

PAGE WRITE OPERATION

The WE-128K32-XHX has a page write operation that allows one to 128 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µS or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A6 at each write cycle. In this manner a page of up to 128 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µS time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

PAGE WRITE CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Min.	Max.	Unit
PAGE MODE WRITE CHARACTERISTICS				
Write Cycle Time, TYP = 6 mS	t_{WC}		10	mS
Address Set-up Time	t_{AS}	10		nS
Address Hold Time (1)	t_{AH}	100		nS
Data Set-up Time	t_{DS}	100		nS
Data Hold Time	t_{DH}	10		nS
Write Pulse Width	t_{WP}	150		nS
Byte Load Cycle Time	t_{BLC}		150	µS
Write Pulse Width High	t_{WPH}	50		nS

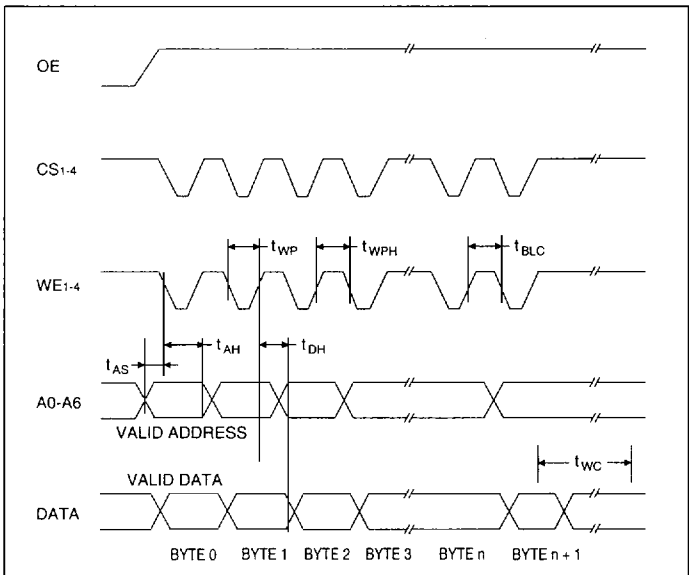


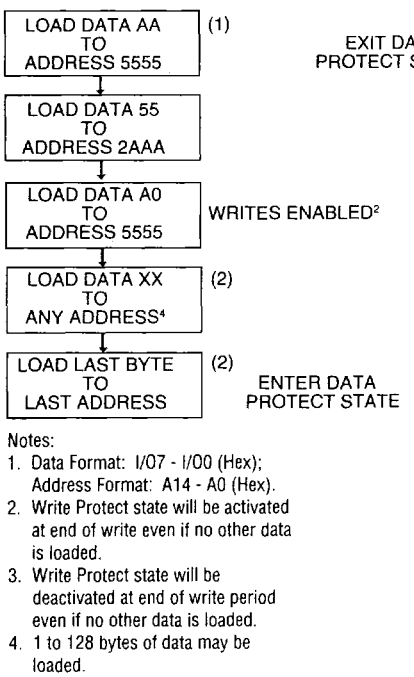
FIGURE 8 – Data Polling Waveforms

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Technology, the WE-128K32-XHX has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 128K byte block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.



Notes:
1. Data Format: I/O7 - I/O0 (Hex); Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

FIGURE 9 – Software Block Data Protection Enable Algorithm

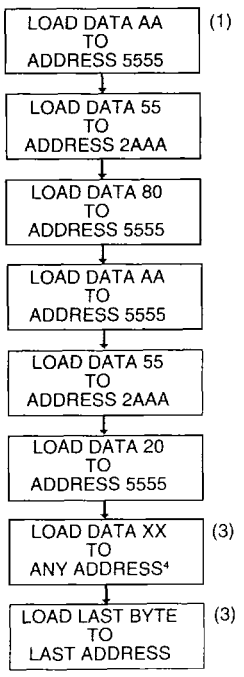


FIGURE 10 – Software Block Data Protection Disable Algorithm

HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the WE-128K32-XHX. These are included to improve reliability during normal operation:

a) V_{CC} power on delay - As V_{CC} climbs past 3.8V the device will wait 5 mSec before allowing write cycles.

b) V_{CC} sense - While below 3.8V write cycles are inhibited.

c) Write inhibiting - Holding $\overline{OE}$ low and either $\overline{CS}$ or $\overline{WE}$ high inhibits write cycles.

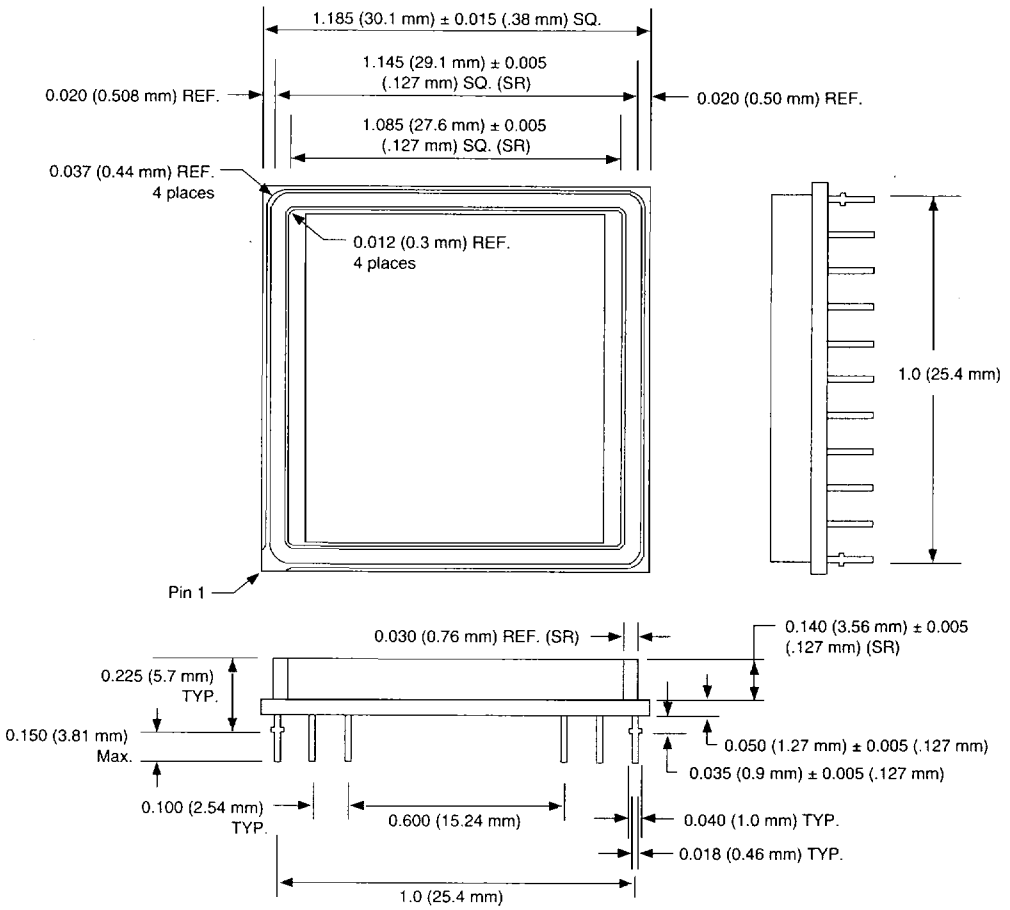


FIGURE 11 — Package Dimensions

ORDERING INFORMATION

W E - 128K 32 - XXX H X

DEVICE GRADE:
Q = MIL-STD-883 Compliant
M = Mil, -55°C to 125°C
I = Industrial, -40°C to 85°C
C = Commercial, 0 to 70°C

PACKAGE TYPE:
H = Ceramic Hex in line package

ACCESS TIME IN nS

BITS PER WORD:
x8, x16, x32

NUMBER OF WORDS:
512K, 256K, 128K

EEPROM

WHITE TECHNOLOGY

White Technology, Inc.
A wholly owned subsidiary of Bowmar Instrument Corporation
4246 East Wood Street Phoenix, Arizona 85040
Tel: 602-437-1520 Fax: 602-437-9120

NOTES:

OTHER PRODUCTS FROM WHITE TECHNOLOGY, INC.

Application Specific Multichip Modules for Military, Industrial and Commercial Applications

- Customer specified processors, coprocessors, memory, temperature ranges, packaging and other application specific requirements.
- Engineering support from circuit design through final package assembly.
- Facility certified to MIL-STD-1772.
- Military screening available to meet requirements of MIL-H-38534 and Test Method 5008 of MIL-STD-883.

Custom Memory Modules

- **MCMMs** with customer defined memory capacities and packaging. Our customers can specify the amount and organizations needed for unique applications.

Standard SRAM Modules

- 25 to 120 nS speeds
- 512K x 8, 256K x 8, 128K x 8, 128K x 32, 512K x 32 MCMMs
- 32 pin JEDEC DIP pinouts (DESC qualified, QML-38534 per EQC-92-138)
- Hex-in-line 66 pin PGA-type modules, configurable as 128K x 32, 256K x 16 or 512K x 8
- 64M SRAM configurable to 8M x 8, 4M x 16 or 2M x 32
- Military, Industrial and Commercial grade devices
- Military screening available
- Low power CMOS

Standard EEPROM Modules

- 512K x 8, 256K x 8, 128K x 8 DIP modules
- 150 nS access time
- Low power CMOS
- 32 pin JEDEC DIP pinouts (DESC qualified, QML-38534 per EQC-92-070)
- Hex-in-line 66 pin PGA-type modules, configurable as 128K x 32, 256K x 16 or 512K x 8
- Military, Industrial and Commercial temperatures
- Military screening available

Standard Flash Modules

- 1024K x 8, 200nS, 34 pin DIP module
- Hex-in-line 66 pin PGA-type modules, configurable as 128K x 32, 256K x 16 or 512K x 8
- 128M Flash PROM configurable to 16M x 8, 8M x 16 or 4M x 32

Standard Microcontroller Modules

- 80C31 based with 64Kbytes Flash and 8Kbytes SRAM
- 80C88 based with 16K x 8 SRAM and 16K x 8 EEPROM
- 68020 based with 32K x 32 SRAM, 32K x 32 EEPROM, optional 68881FPC, RS232/422/485
- i486™ based with 512K x 32 SRAM, 1M x 32 EEPROM; advanced info

Represented by: