

## Highly Accurate, Ultra Small, Low Power Consumption Voltage Detector

### GENERAL DESCRIPTION

The XC6120 series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies. With low power consumption and high accuracy, the series is suitable for precision mobile equipment. The XC6120 in ultra small packages are ideally suited for high-density mounting. The XC6120 is available in both CMOS and N-channel open drain output configurations.

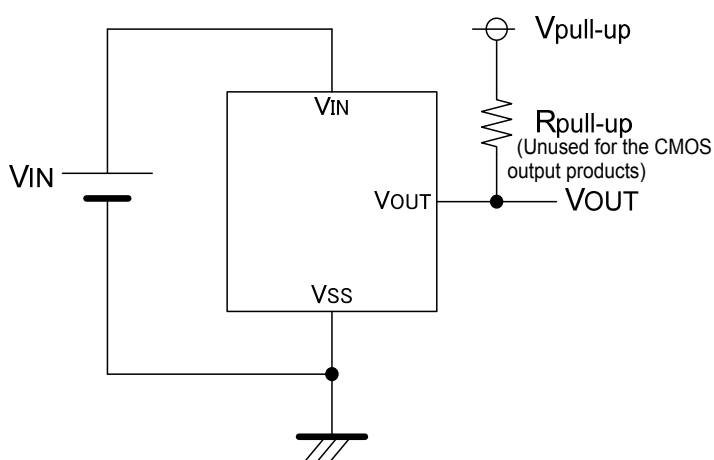
### APPLICATIONS

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

### FEATURES

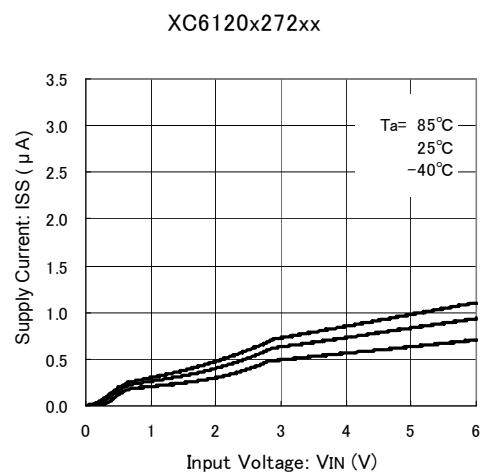
- Highly Accurate** :  $\pm 2\%$  ( $V_{DF(T)} = 1.5V$ )  
:  $\pm 30mV$  ( $V_{DF(T)} < 1.5V$ )
- Low Power Consumption** :  $0.6 \mu A$  (TYP.) [ $V_{DF(T)} = 2.7V, V_{IN} = 2.97V$ ]
- Detect Voltage Range** :  $1.0V \sim 5.0V$  in  $0.1V$  increments
- Operating Voltage Range** :  $0.7V \sim 6.0V$
- Detect Voltage Temperature Characteristics**  
:  $\pm 100ppm/^\circ C$  (TYP.)
- Output Configuration** : CMOS (XC6120C)  
: N-channel open drain (XC6120N)
- Operating Temperature Range** :  $-40 \sim 85$
- Ultra Small Packages** : USP-3, SSOT-24

### TYPICAL APPLICATION CIRCUIT

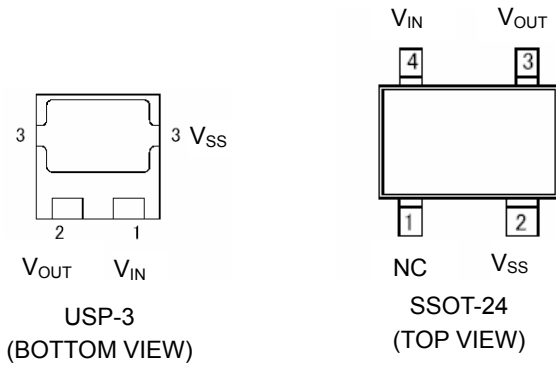


### TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs. Input Voltage



## PIN CONFIGURATION



## PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
USP-3	SSOT-24		
1	4	V <sub>IN</sub>	Power Input
3	2	V <sub>SS</sub>	Ground
2	3	V <sub>OUT</sub>	Output
-	1	NC	No Connection

## PRODUCT CLASSIFICATION

Ordering Information

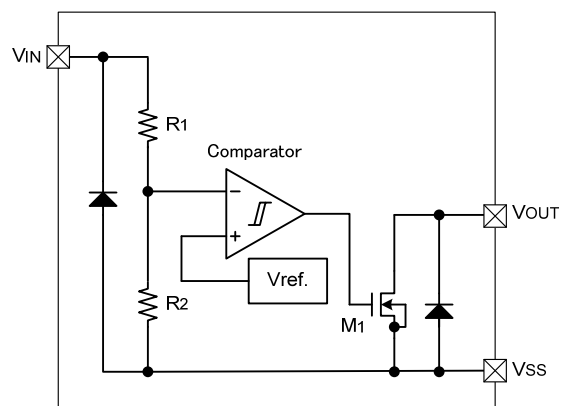
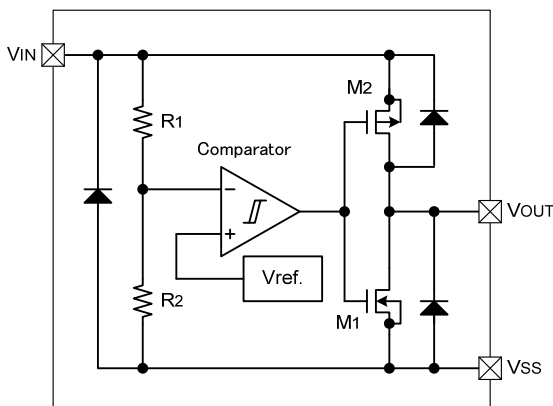
XC6120

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
	Output Configuration	C	: CMOS output
		N	: N-ch open drain output
	Detect Voltage (V <sub>DF</sub> )	10~50	: For example 1.0V    1,    0
	Detect Accuracy	2	: ± 2%
	Packages	H	: USP-3 (1 reel=3,000 pcs)
		N	: SSOT-24 (SC-82) (1 reel=3,000 pcs)
	Device Orientation	R	: Embossed tape, standard feed
		L	: Embossed tape, reverse feed

## BLOCK DIAGRAMS

(1) XC6120C

(2) XC6120N



## ABSOLUTE MAXIMUM RATINGS

Ta=25

PARAMETER	SYMBOL	RATING	UNITS
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.3~7.0	V
Output Current	I <sub>OUT</sub>	10	mA
Output Voltage	CMOS Output	V <sub>SS</sub> -0.3~V <sub>IN</sub> +0.3	V
	N-ch Open Drain Output	V <sub>SS</sub> -0.3~7.0	
Power Dissipation	USP-3	120	mW
	SSOT-24	150	
Operating Temperature Range	Ta	-40~+85	
Storage Temperature Range	Tstg	-55~+125	

## ELECTRICAL CHARACTERISTICS

XC6120 Series

Ta=25

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Operating Voltage	V <sub>IN</sub>	V <sub>DF(T)</sub> =1.0 ~ 5.0V <sup>(*1)</sup>	0.7	-	6.0	V	-
Detect Voltage	V <sub>DF</sub>	V <sub>DF(T)</sub> =1.0V ~ 5.0V	E-1			V	
Hysteresis Width	V <sub>HYS</sub>	V <sub>DF(T)</sub> =1.0V ~ 5.0V	V <sub>DF</sub> × 0.03	V <sub>DF</sub> × 0.05	V <sub>DF</sub> × 0.07	V	
Supply Current 1	I <sub>SS1</sub>	V <sub>IN</sub> =V <sub>DF(T)</sub> × 1.1	E-2			μA	
Supply Current 2	I <sub>SS2</sub>	V <sub>IN</sub> = V <sub>DF(T)</sub> × 0.9V	E-3			μA	
Output Current	I <sub>OUTN</sub>	V <sub>IN</sub> =0.7V	V <sub>OUT</sub> =0.5V	0.09	0.57	-	mA
			V <sub>OUT</sub> =0.3V	0.08	0.56	-	
			V <sub>OUT</sub> =0.1V	0.05	0.30	-	
	I <sub>OUTP</sub> <sup>(*2)</sup>	V <sub>IN</sub> =6.0V, V <sub>OUT</sub> =5.5V	-	-0.95	-0.60	mA	
I <sub>LEAK</sub>	V <sub>IN</sub> =6.0V, V <sub>OUT</sub> =6.0V	XC6120C	-	0.001	-	μA	
		XC6120N	-	0.001	0.100		
Temperature Characteristics	$\frac{V_{DF}}{Ta \cdot V_{DF}}$	-40 °C Ta 85 °C	-	± 100	-	ppm/°C	
Detect Delay Time <sup>(*3)</sup>	T <sub>DF</sub>	V <sub>IN</sub> =6.0V 0.7V V <sub>IN</sub> =V <sub>DF</sub> to V <sub>OUT</sub> =0.5V	-	30	100	μs	
Release Delay Time <sup>(*5)</sup>	T <sub>DR</sub>	V <sub>IN</sub> =0.7V 6.0V V <sub>IN</sub> =V <sub>DR</sub> to V <sub>OUT</sub> =V <sub>DR</sub> <sup>(*4)</sup>	-	20	100	μs	

\*1: V<sub>DF (T)</sub>: Setting detect voltage

\*2: For XC6120C Series only

\*3: A time taking from the time at V<sub>IN</sub> = V<sub>DF</sub> to the time at V<sub>OUT</sub>=0.5V when V<sub>IN</sub> falls from 6.0V to 0.7V.

\*4: V<sub>DR</sub>: Release voltage (V<sub>DR</sub> = V<sub>DF</sub> + V<sub>HYS</sub>)

\*5: A time taking from the time at V<sub>IN</sub> = V<sub>DR</sub> to the time at V<sub>OUT</sub> = V<sub>DR</sub> when V<sub>IN</sub> rise from 0.7V to 6.0V.

XC6120N Series recommended pull-up resistance

Input Voltage Range	Pull-up Resistance
0.7V~6.0V	220k
0.8V~6.0V	100k
1.0V~6.0V	33k

## ELECTRICAL CHARACTERISTICS (Continued)

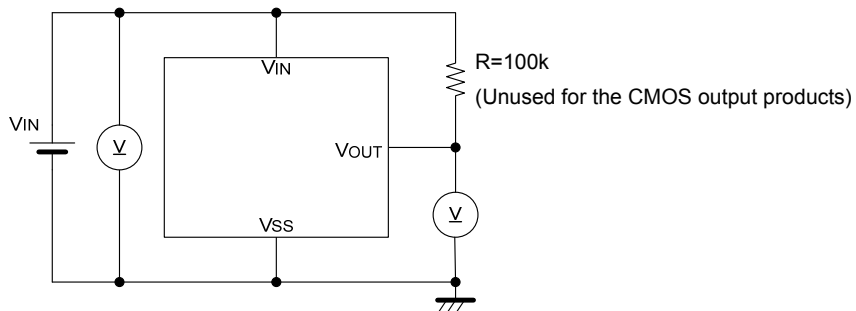
### DETECT VOLTAGE ACCURACY AND SUPPLY CURRENT SPECIFICATIONS

SYMBOL	E-1		E-2		E-3	
PARAMETER	DETECT VOLTAGE		SUPPLY CURRENT 1		SUPPLY CURRENT 2	
SETTING DETECT VOLTAGE	V <sub>DF</sub> (V) XC6120xxx2 Series		I <sub>SS1</sub> (μA)		I <sub>SS2</sub> (μA)	
V <sub>DF(T)</sub>	MIN.	MAX.	TYP.	MAX.	TYP.	MAX.
1.0	0.970	1.030	0.5	1.4	0.4	1.35
1.1	1.070	1.130				
1.2	1.170	1.230				
1.3	1.270	1.330				
1.4	1.370	1.430				
1.5	1.470	1.530				
1.6	1.568	1.632				
1.7	1.666	1.734				
1.8	1.764	1.836				
1.9	1.862	1.938				
2.0	1.960	2.040	0.6	1.7	0.5	1.60
2.1	2.058	2.142				
2.2	2.156	2.244				
2.3	2.254	2.346				
2.4	2.352	2.448				
2.5	2.450	2.550				
2.6	2.548	2.652				
2.7	2.646	2.754				
2.8	2.744	2.856	0.7	1.9	0.6	1.80
2.9	2.842	2.958				
3.0	2.940	3.060				
3.1	3.038	3.162				
3.2	3.136	3.264				
3.3	3.234	3.366				
3.4	3.332	3.468				
3.5	3.430	3.570				
3.6	3.528	3.672				
3.7	3.626	3.774				
3.8	3.724	3.876				
3.9	3.822	3.978				
4.0	3.920	4.080				
4.1	4.018	4.182				
4.2	4.116	4.284				
4.3	4.214	4.386				
4.4	4.312	4.488				
4.5	4.410	4.590				
4.6	4.508	4.692				
4.7	4.606	4.794				
4.8	4.704	4.896				
4.9	4.802	4.998				
5.0	4.900	5.100				

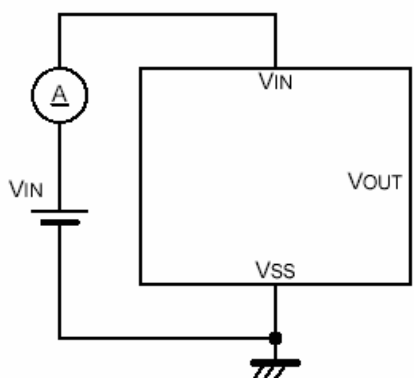
(6) When setting detect voltage is 1.0V V<sub>DF(T)</sub> < 1.5V, detect accuracy is ±30mV.  
 When setting detect voltage is 1.5V V<sub>DF(T)</sub> 5.0V, detect accuracy is ±2%.

## TEST CIRCUITS

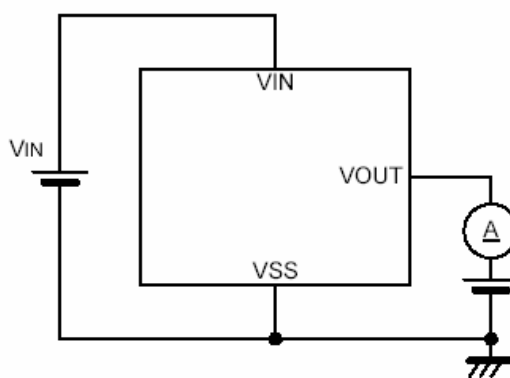
Circuit 1



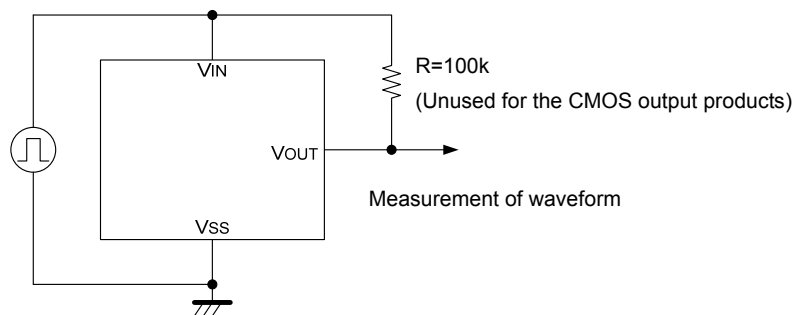
Circuit 2



Circuit 3

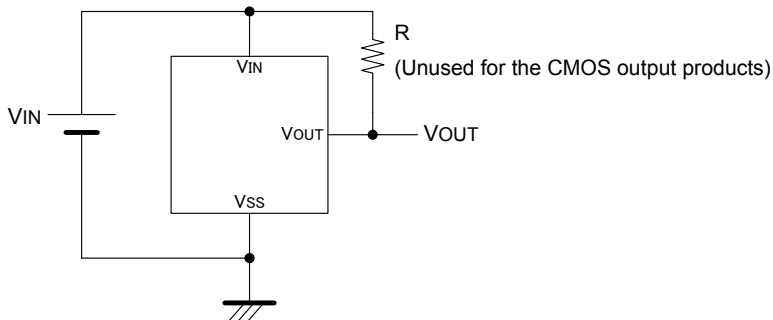


Circuit 4

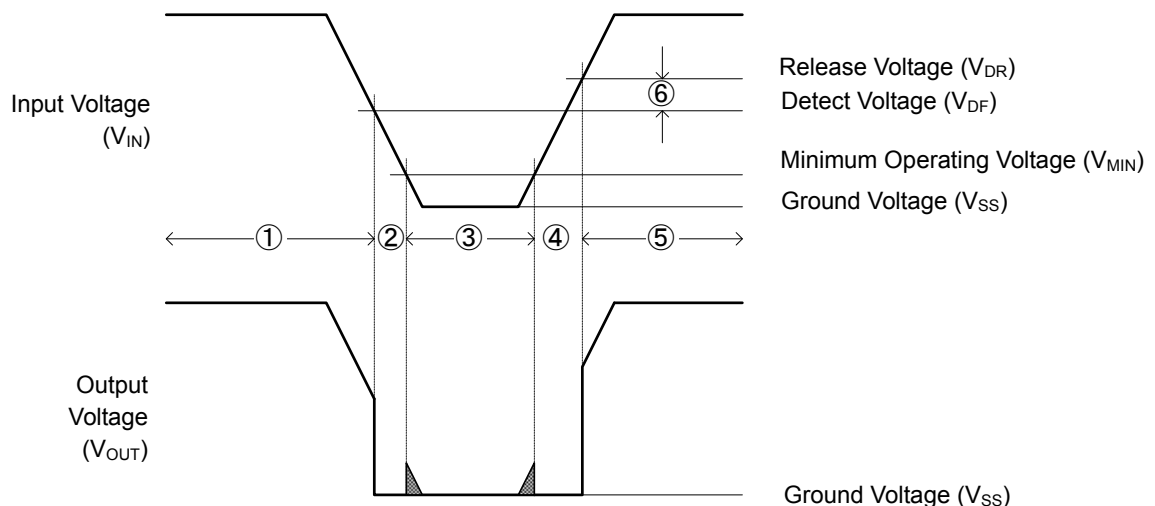


## OPERATIONAL EXPLANATION

### Typical Application Circuit



### Timing Charge



Note: For explaining in a simplified case, an operation time of the circuit is not counted.

The following explains the operation of the typical application circuit along number symbols shown in the timing chart.

When input voltage ( $V_{IN}$ ) rises above detect voltage ( $V_{DF}$ ), output voltage ( $V_{OUT}$ ) will be equal to input voltage ( $V_{IN}$ ). (A condition of high impedance exists with N-ch open drain output configurations.)

When input voltage ( $V_{IN}$ ) falls below detect voltage ( $V_{DF}$ ), output voltage ( $V_{OUT}$ ) will be equal to the ground voltage ( $V_{SS}$ ) level.

When input voltage ( $V_{IN}$ ) falls to a level below that of the minimum operating voltage ( $V_{MIN}$ ), output will become unstable. If in this condition,  $V_{IN}$  will equal the pulled-up output (should output be pulled-up.) (Input voltage,  $V_{IN}$ , in the typical application circuit.)

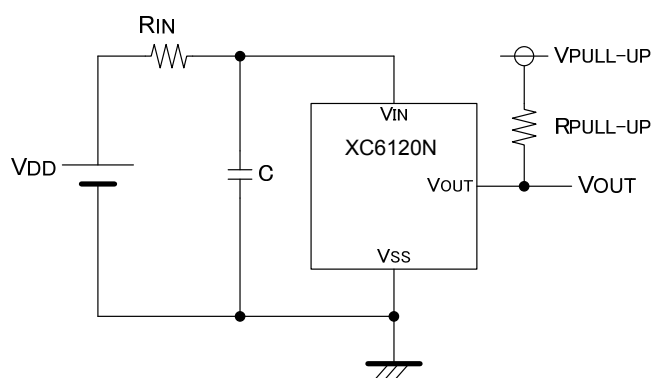
When input voltage ( $V_{IN}$ ) rises above the minimum operating voltage ( $V_{MIN}$ ) level until it achieves a release voltage ( $V_{DR}$ ), output keeps the ground voltage level ( $V_{SS}$ ).

When the input voltage ( $V_{IN}$ ) rises above the release voltage ( $V_{DR}$ ), output voltage ( $V_{OUT}$ ) will be equal to input voltage ( $V_{IN}$ ). (A condition of high impedance exists with N-ch open drain output configurations.)

The difference between  $V_{DR}$  and  $V_{DF}$  represents the hysteresis width.

## NOTE ON USE

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. In order to stabilize the IC's operations, please ensure that  $V_{IN}$  pin's input frequency's rise and fall times are more than several  $\mu s / V$ .
3. With a resistor connected between the  $V_{IN}$  pin and the power supply  $V_{DD}$  some errors may be observed from the input voltage at the detect and release voltage. Those errors are not constant because of the fluctuation of the supply current.
4. When a resistor is connected between the  $V_{IN}$  pin and the power supply  $V_{DD}$ , oscillation may occur as a result of through current and voltage drop at the  $R_{IN}$  at the time of voltage release. (refer to the Oscillation Description (1) below ) Especially in the CMOS output configurations, oscillation may occur regardless of detect/release operation if load current ( $I_{OUT}$ ) exists. (refer to the Oscillation Description (2) below)
5. Please use N-ch open drains configuration, when a resistor  $R_{IN}$  is connected between the  $V_{IN}$  pin and the power supply  $V_{DD}$  power source. In such cases, please ensure that  $R_{IN}$  is less than  $10k\Omega$  and that  $C$  is more than  $0.1 \mu F$ .



[Figure 1: Circuit connected with the input resistor]

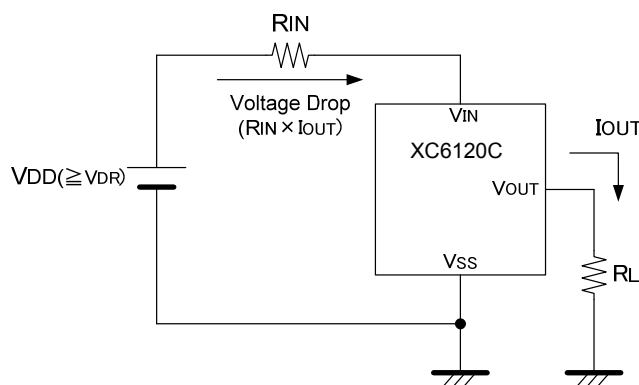
### Oscillation Description

#### (1) Oscillation as a result of through current

Since the XC6120 series are CMOS ICs, transient through current will flow when the IC's internal circuit switching operates regardless of output configuration. Consequently, oscillation is liable to occur as a result of the similar operations as in (1) above. This oscillation does not occur during the detect operation.

#### (2) Output current oscillation with the CMOS output configuration

As shown in figure 2, when the voltage applied at the power supply ( $V_{DD}$ ) rises from below detect voltage to above release voltage, the IC commence release operations and the internal P-ch driver transistor will be on. The output current ( $I_{OUT}$ ) flows the input resistor ( $R_{IN}$ ) via the P-ch driver transistor. Because of the input resistor ( $R_{IN}$ ) and the output current ( $I_{OUT}$ ), an input pin voltage drops  $R_{IN} \times I_{OUT}$ . If the voltage drop level is larger than the IC's hysteresis width ( $V_{HYS}$ ), the input pin voltage will falls below the  $V_{DF}$  and detect operations will commence so that the internal P-ch driver transistor will be off. The voltage drop will stop because the output current ( $I_{OUT}$ ) which was flowing the P-ch driver transistor will run down. The input pin voltage will become the same voltage level as the input voltage ( $V_{IN}$ ). For this, the input pin voltage will rise above the release voltage ( $V_{DR}$ ), therefore, the release operations will begin over again. Oscillation may occur with this repetition. Further, this condition will also appear via means of a similar mechanism during detect operations.

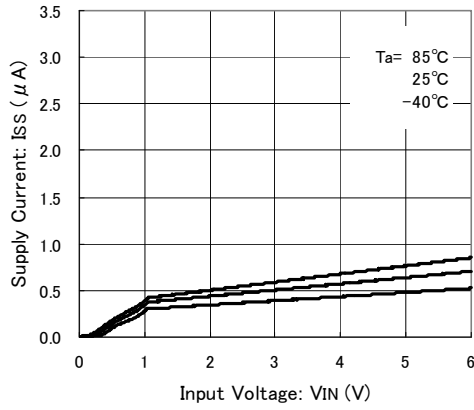


[Figure 2: Oscillation caused by the input resistor of the CMOS output product and the output current]

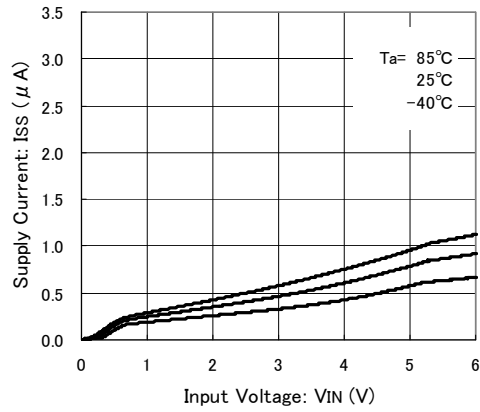
## TYPICAL PERFORMANCE CHARACTERISTICS

### (1) Supply Current vs. Input Voltage

XC6120x102xx

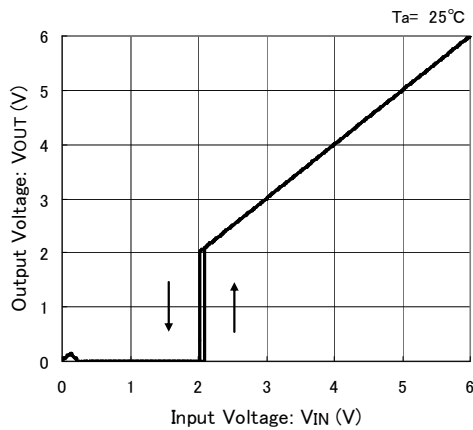


XC6120x502xx

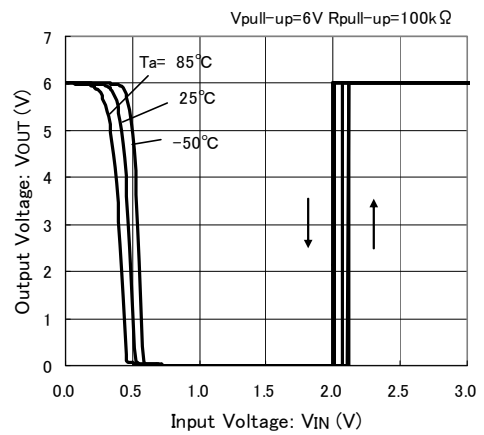


### (2) Output Voltage vs. Input Voltage

XC6120C202xx

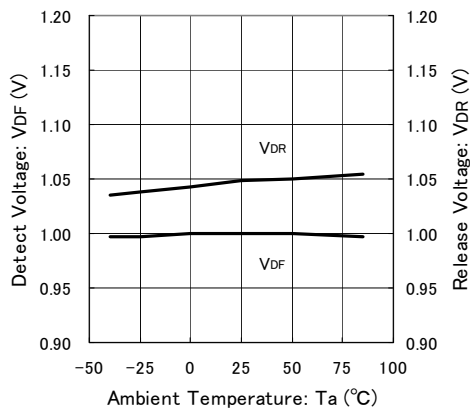


XC6120N202xx

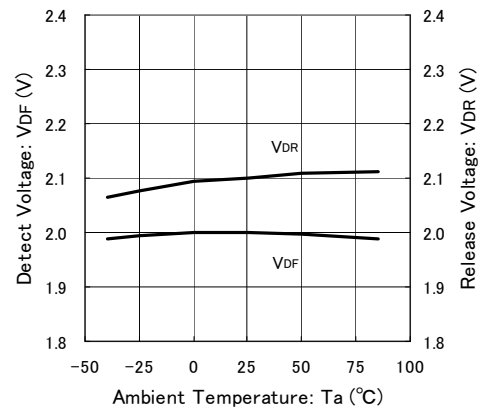


### (3) Detect Voltage, Release Voltage vs. Ambient Temperature

XC6120x102xx



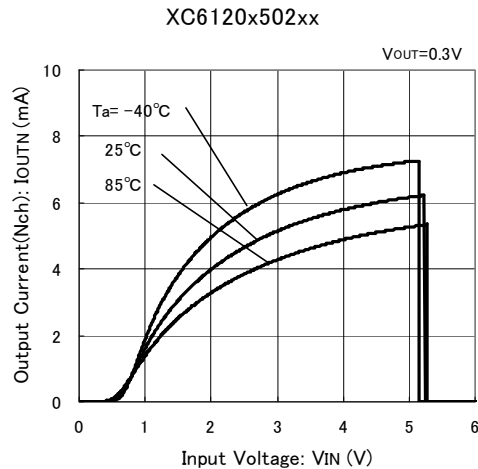
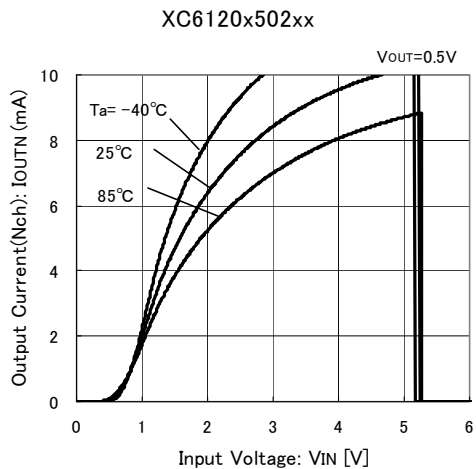
XC6120x202xx



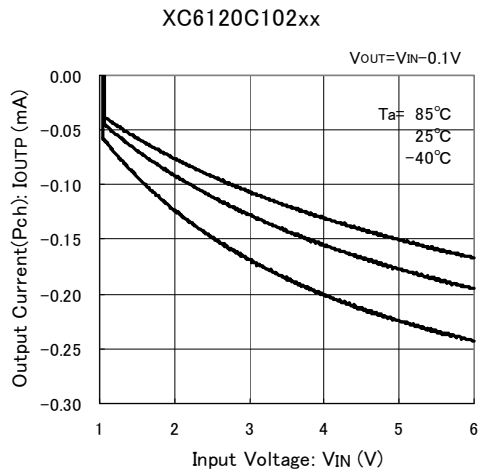
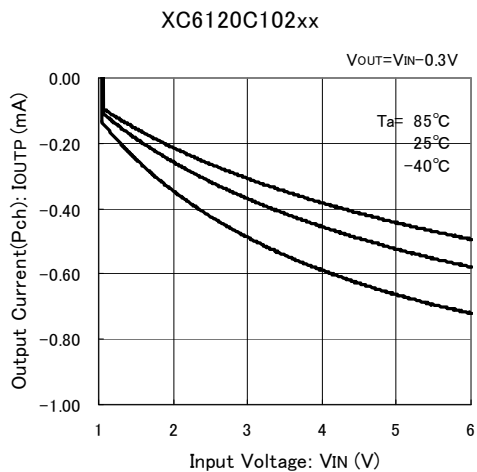
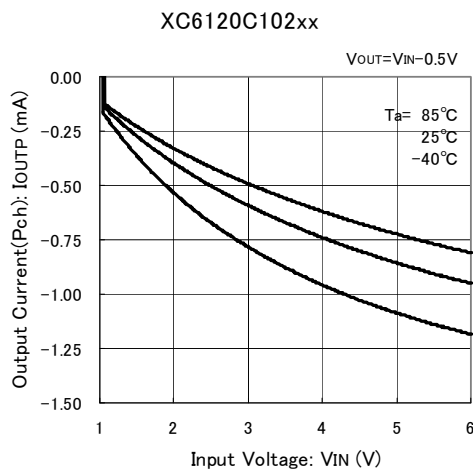
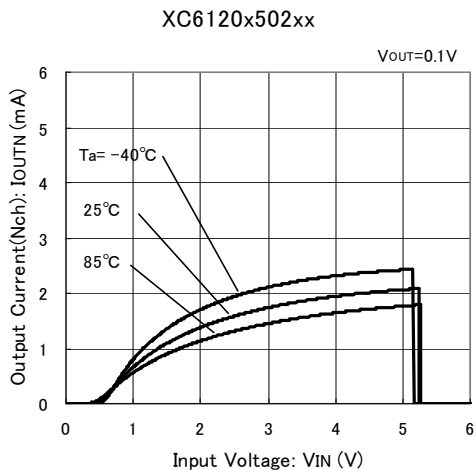


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (4) Output Current (Nch Driver) vs. Input Voltage

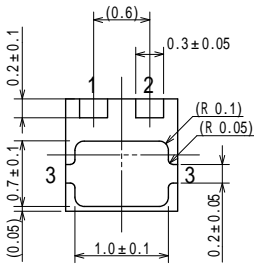
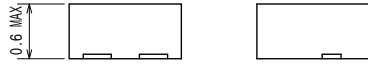
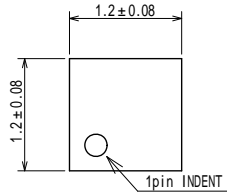


### (5) Output Current (Pch Driver) vs. Input Voltage



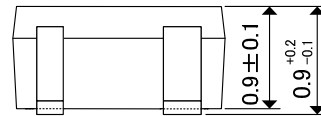
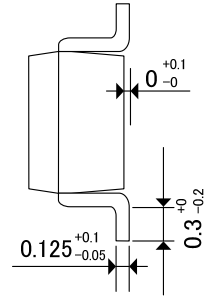
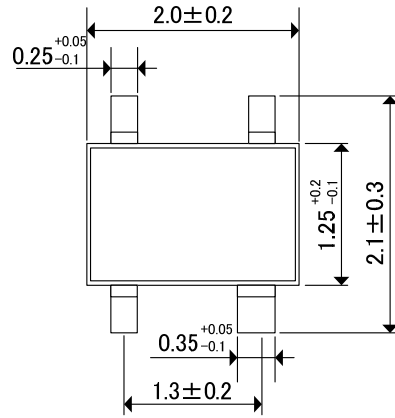
## PACKAGING INFORMATION

USP-3

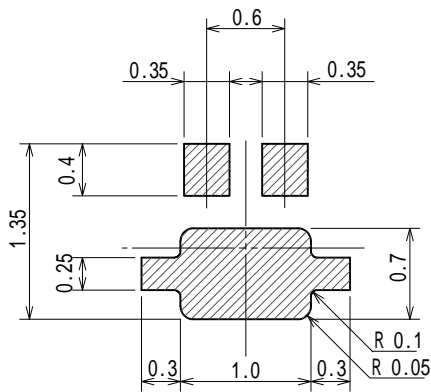


\*Solder fillet is not formed because of no plating at the lead side

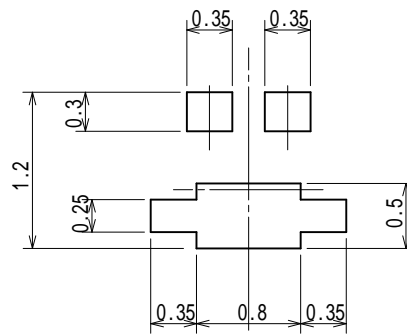
SSOT-24



USP-3 Reference Pattern Layout



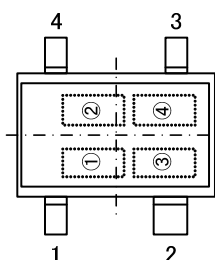
USP-3 Reference Metal Mask Design



\*Thickness of solder paste : 120  $\mu$ m ( recommended )

## MARKING RULE

SSOT-24



Represents output configuration and detect voltage Range

MARK	OUTPUT CONFIGURATION	OUTPUT VOLTAGE	PRODUCT SERIES
K	CMOS	1.0V ~ 2.9V	XC6120C
L		3.0V ~ 5.0V	
M	Nch open drain	1.0V ~ 2.9V	XC6120N
N		3.0V ~ 5.0V	

**SSOT-24**  
(TOP VIEW)

Represents detect voltage

MARK	DETECT VOLTAGE (V)		MARK	DETECT VOLTAGE (V)	
0	-	3.0	F	1.5	4.5
1	-	3.1	H	1.6	4.6
2	-	3.2	K	1.7	4.7
3	-	3.3	L	1.8	4.8
4	-	3.4	M	1.9	4.9
5	-	3.5	N	2.0	5.0
6	-	3.6	P	2.1	-
7	-	3.7	R	2.2	-
8	-	3.8	S	2.3	-
9	-	3.9	T	2.4	-
A	1.0	4.0	U	2.5	-
B	1.1	4.1	V	2.6	-
C	1.2	4.2	X	2.7	-
D	1.3	4.3	Y	2.8	-
E	1.4	4.4	Z	2.9	-

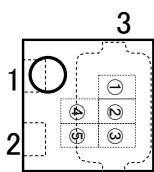
Represents production lot number

01 to 09, 10, 11, ..., 99, 0A, ..., 0Z, 1A, ...repeated.

(G, I, J, O, Q, W excluded. Reversed character is not used.)

## MARKING RULE (Continued)

USP-3



**USP-3  
(TOP VIEW)**

Represents product series

MARK	PRODUCT SERIES
0	XC6120*****

Standard : Represents output configuration and integer number of detect voltage

CMOS Output (XC6120C Series)

MARK	DETECT VOLTAGE (V)
A	1.X
B	2.X
C	3.X
D	4.X
E	5.X

Nch open drain (XC6120N Series)

MARK	DETECT VOLTAGE (V)
F	1.X
H	2.X
K	3.X
L	4.X
M	5.X

Standard : Represents decimal point of detect voltage

MARK	DETECT VOLTAGE (V)	PRODUCT SERIES
3	X.3	XC6120**3***
0	X.0	XC6120**0***

Represents production lot number

01 to 09, 10, 11, ..., 99, 0A, ..., 0Z, 1A, ...repeated.

(G, I, J, O, Q, W excepted.)

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