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Supertex inc.

VN02A

T-39-05

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package				
			TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP
40V	2Ω	3.0A	VN0204N2	—	VN0204N5	VN0240N6	VN0204N7
60V	2Ω	3.0A	VN0206N2	VN0206N3	VN0206N5	VN0206N6	VN0206N7
100V	2Ω	3.0A	VN0210N2	VN0210N3	VN0210N5	—	—

Features

- □ Freedom from secondary breakdown
- □ Low power drive requirement
- □ Ease of paralleling
- □ Low C_{ISS} and fast switching speeds
- □ Excellent thermal stability
- □ Integral Source-Drain diode
- □ High input impedance and high gain
- □ Complementary N- and P-Channel devices

Applications

- □ Motor control
- □ Converters
- □ Amplifiers
- □ Switches
- □ Power supply circuits
- □ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

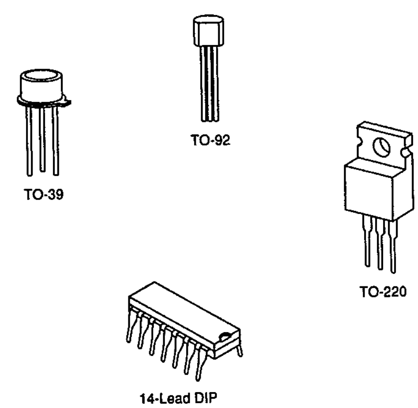
*Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	1.5A	4A	4W	25	125	2A	4A
TO-92	0.8A	4A	1W	125	170	0.8A	4A
TO-220	3.0A	4A	28W	4.8	70	3A	4A
Plastic Dip	Refer to Arrays and Special Functions section.						
Ceramic Dip							

*I_D (continuous) is limited by max rated T_j.

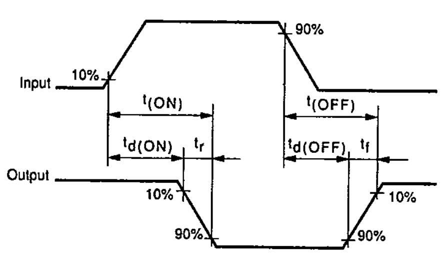
Electrical Characteristics (@ 25°C unless otherwise specified)

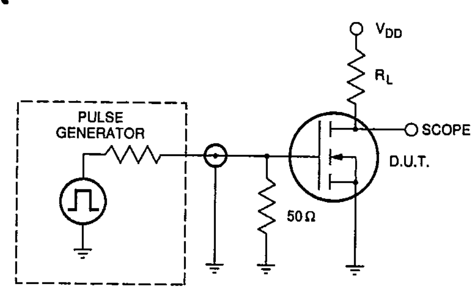
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0204	40			V	V_{GS} = 0, I_D = 2.5mA
		VN0206	60				
		VN0210	100				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 2.5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 2.5mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				25	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.2	1.6		A	V_{GS} = 5V, V_{DS} = 25V
			3.0	4.0			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.6	2.5	Ω	V_{GS} = 5V, I_D = 1A
				1.5	2		V_{GS} = 10V, I_D = 2A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.5	0.75	%/°C	V_{GS} = 10V, I_D = 2A
G_{FS}	Forward Transconductance		0.4	0.65		℧	V_{DS} = 25V, I_D = 2A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			12	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V I_D = 0.5A R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				13		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V_{GS} = 0, I_{SD} = 1.5A
t_{rr}	Reverse Recovery Time			330		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

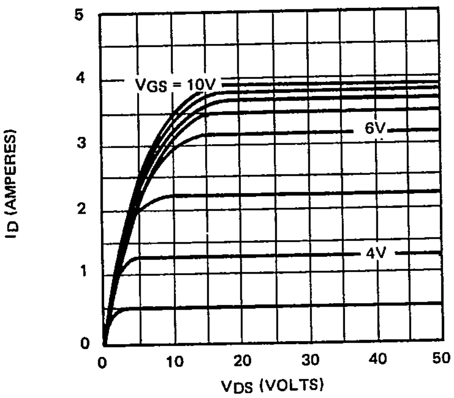
Switching Waveforms and Test Circuit



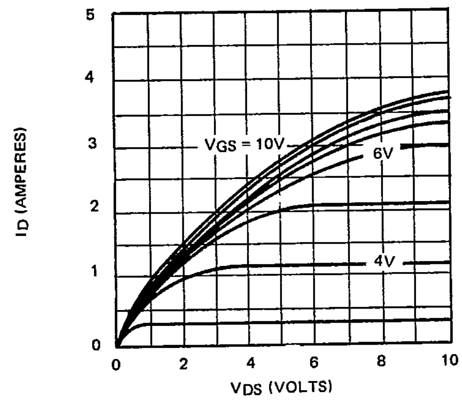


Typical Performance Curves

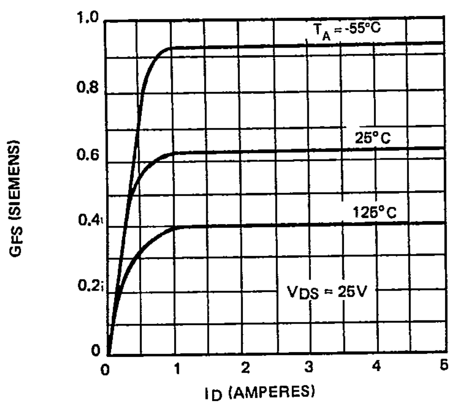
Output Characteristics



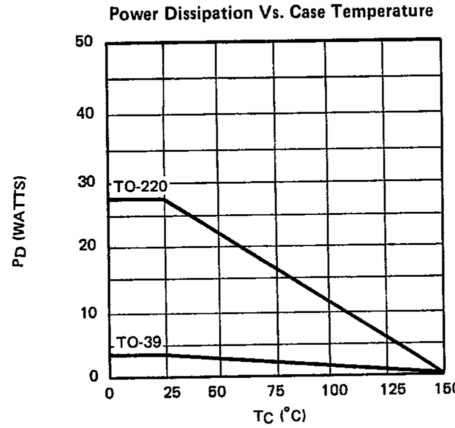
Saturation Characteristics



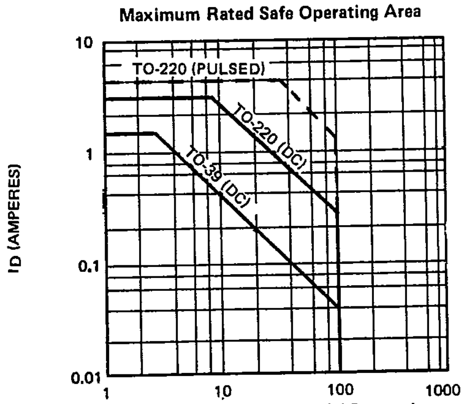
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

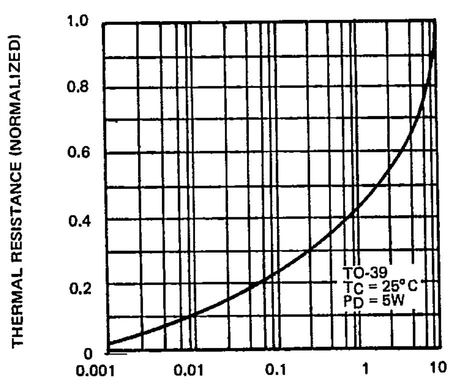


Maximum Rated Safe Operating Area



Pulse Condition: 300 μs, 2% Dutycycle.
VDS (VOLTS)

Thermal Response Characteristics



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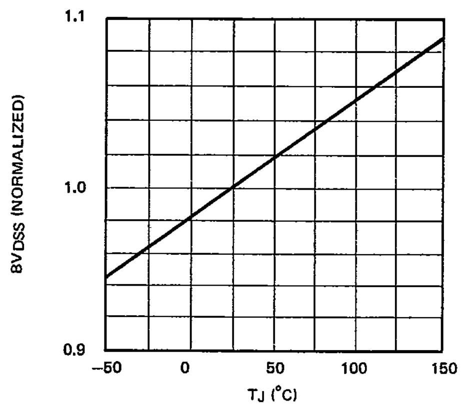
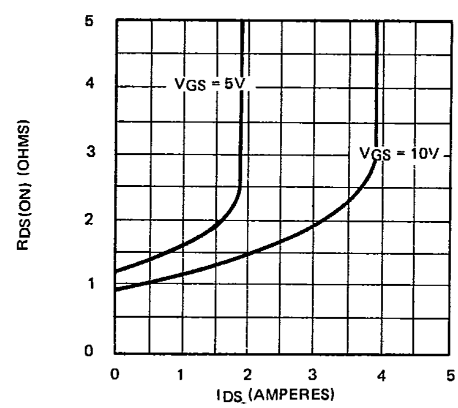
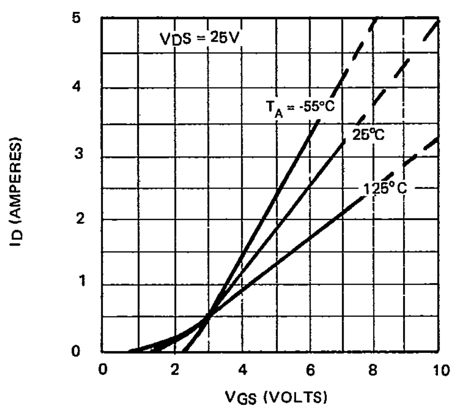
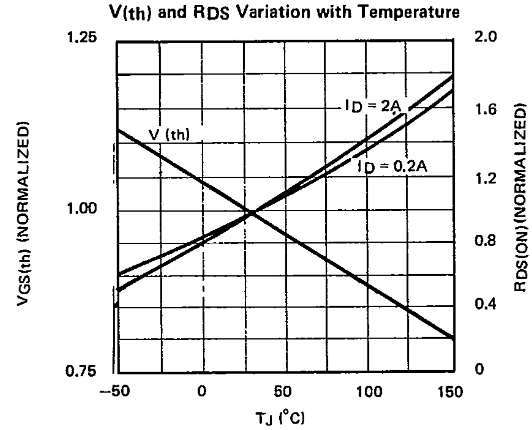
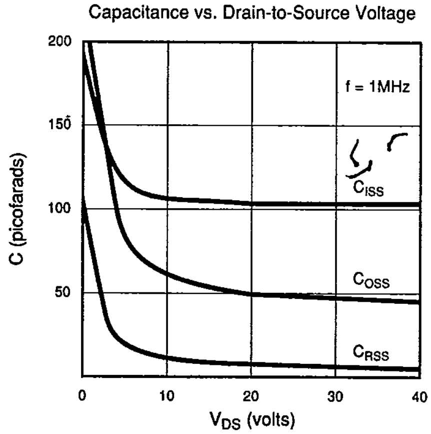
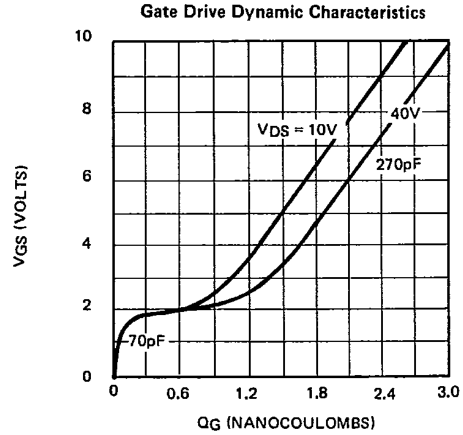

BVDSS Variation with Temperature
1.1
1.0
0.9
BVDSS (NORMALIZED)
−50
0
50
100
150
TJ (°C)


ON - Resistance Vs. Drain Current
VGS = 5V
VGS = 10V
RDS(ON) (OHMS)
IDS (AMPERES)


Transfer Characteristics
VDS = 25V
TA = -55°C
25°C
125°C
ID (AMPERES)
VGS (VOLTS)


V(th) and RDS Variation with Temperature
1.25
1.00
0.75
2.0
1.6
1.2
0.8
0.4
ID = 2A
V (th)
ID = 0.2A
VGS(th) (NORMALIZED)
RDS(ON) (NORMALIZED)
TJ (°C)


Capacitance vs. Drain-to-Source Voltage
200
150
100
50
f = 1MHz
CISS
COSS
CRSS
C (picofarads)
VDS (volts)


Gate Drive Dynamic Characteristics
VDS = 10V
40V
270pF
70pF
VGS (VOLTS)
0.6
1.2
1.8
2.4
3.0
QG (NANOCOULOMBS)