Description

The Reticon RA0100A and RA0128N are two-dimensional self-scanned optical sensor arrays with optimized characteristics. The discrete photodiodes are geometrically arranged in 100 x 100 and 128 x 128 matrices. In contrast to comparable CCD devices, discrete photodiode sensors require no surface electrodes, so there is no interference pattern or light loss and the full inherent sensitivity of a silicon photodiode is obtainable.

The scanning method permits pixel rates up to 10 MHz. Each line of pixel information is parallel-loaded into two high-speed bucket-brigade (BBD) analog shift registers and sequentially shifted out. The outputs of the registers are then combined externally to reconstruct the line information. All of the 100 or 128 lines may be sequentially accessed to give a single frame, or alternate odd or even lines may be selected to produce one-half of the lines per field in an odd and even pattern. The integration time is normally one frame period, giving maximum sensitivity.

The primary applications of these devices are in industrial and scientific instrumentation systems, such as:

- Noncontact optical measurements
- Pattern recognition
- Inspection and robotic systems
- Industrial process monitoring and control
- Laser profiling

Key Features

- 10,000 or 16,384 light-sensitive elements in a high-resolution 100 x 100 or 128 x 128 matrix, respectively
- 60 µm center-to-center element spacing in both X and Y directions
- Frame storage. Each diode integrates photocurrent for the entire frame.
- Self-scanned in both X and Y directions by high-speed on-chip circuitry, to provide either single frame or interlaced video output
- Variable data rates up to 10 MHz
- Low power dissipation, small size, and solid state reliability
- 24-pin dual-inline package with scratch resistant quartz window or optional fiber optic faceplate

Functional Description

The RA0100A and RA0128N are each packaged in a 24-pin ceramic side-brazed, dual-inline package with a ground and polished window covering the active area. Figure 1 is a pinout configuration of the devices and Figure 11 shows the package dimensions.

The devices are fabricated using a double-poly NMOS process. Each device consists of several functional elements, shown in Figure 2, to control the operation of the device. These elements have been indicated on Figure 2 by dotted lines. They are:

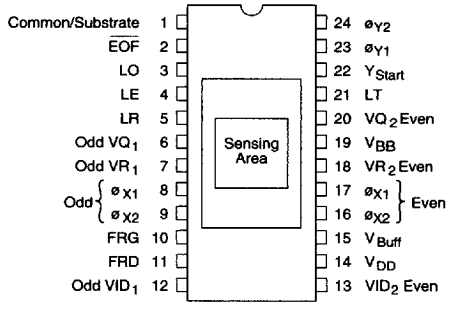


Figure 1. Pinout Configuration

1. Photodiode Array

The first element consists of a 100 x 100 or 128 x 128 diode array matrix, schematically indicated by the columns and rows of individual photodiodes. The diodes in each column are connected one at a time through multiplex switches to a video line, which is common to all diodes in that column. Parallel connection of the multiplex switches simultaneously selects one diode from each column. When a diode is selected by the multiplex switch, the reverse-bias of the diode is reset to a value of V_{GM}-V_{TM}, where V_{GM} (14.5V typical) and V_{TM} (2V typical) are the clock high voltage and threshold voltage of the multiplex switch, respectively. The signal charge removed from the selected diode will be transferred into an analog shift register through the column video line for readout. After the multiplex switch is turned off, the diode starts to integrate photon-generated charge and its reverse-bias decays. The total integration time of each diode is the time between two consecutive readouts of the same diode. Thus, the device operates in a frame storage mode.

2. Digital Dynamic Shift Register (Y Register)

The second element consists of a two phase (2ø) dynamic shift register which controls the multiplex switches. The register turns on each row of diodes in sequence and transfers the corresponding signal charge into the appropriate BBD analog shift register through each column video line. Thus, a complete row of information is loaded at one time. The dynamic shift register is driven by a two-phase clock denoted by $ø_{Y1}$ and $ø_{Y2}$ in Figure 2. It can be self-loaded for sequencing or controlled by an external start pulse Y_{Start}. These functions are performed by a "NOR" circuit. Tied to each output of the shift register (except for the 100th or 128th position) are inputs to a NOR gate which provides for the self-loading feature. When there is an output from any of the 99 (or 127) output positions, the NOR gate keeps the shift register from loading. Once the bit occupies the last position, the NOR gate's output goes high and the shift register loads with the rising edge of $ø_{Y1}$. Note that Y_{Start} is connected to the NOR gate. It can be used to inhibit the register from loading by pulling Y_{Start} to V_{DD}. Odd lines are accessed while $ø_{Y1}$ clock is high, even while $ø_{Y2}$ is high.

345 POTRERO AVENUE SUNNYVALE, CALIFORNIA 94086-4197 (408) 738-4266 FAX: (408) 738-6979

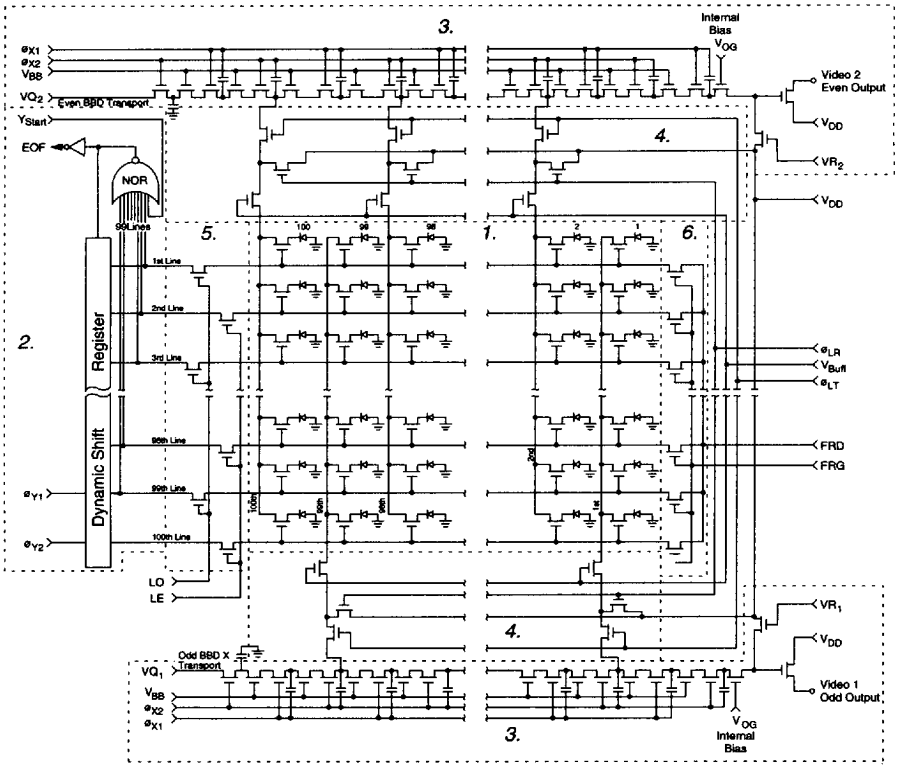


Figure 2. Schematic Diagram RA0100A (the RA0128N has a Similar Format with the Exception of 128 Lines and 128 Pixels Per Line)

The NOR gate output is connected to an external pin, EOF, through an open-drain inverter. This output is normally tied to V_{DD} through an 8.6KΩ resistor; therefore, when there is a bit in any row except the last, or if Y_{Start} is active, EOF will remain high. It goes immediately low on the rising edge of ϕ_{Y2} if Y_{Start} is low, and none of the rows 1-99 (or 1-127) are active.

3. Bucket-Brigade Analog Shift Register

Two tetrode-gate bucket-brigade shift registers, each with a gated charge-integrator output, form the third element. These are the odd and even transport registers which accept pixel information in parallel from their respective odd and even video diode columns and shift the pixel information sequentially to the output amplifier. Each shift register is driven by a two-phase clock, denoted by ϕ_{X1}, and ϕ_{X2} in Figure 2. A "fat zero" input is provided to improve the transfer efficiency of the register. The outputs from both shift registers are multiplexed off-chip to obtain one line of combined video information (refer to the RC0502A Evaluation Circuit).

As shown in Figure 2, there are several other terminals associated with the two BBD registers. V_{BB} is the tetrode-gate bias which is usually set at a DC voltage about 1V below the ϕ_{X1} and ϕ_{X2} high level. V_{Q1} and V_{Q2} are the biases for the "fat zero" input. These inputs control the bias level in the dark. Nominally, these terminals are set to approximately 10V. However, when the odd and even videos are summed together, either input bias voltage may be used to adjust the corresponding dark-level output to remove the odd and even pattern. Figure 3 shows the relationship between output dark signal level and V_{Q1}, V_{Q2} bias voltage. The shaded area represents the optimum bias range.

VR_1 and VR_2 are the reset clocks for the output gated-charge amplifiers. These terminals, shown in Figure 2, provide reset voltages for the gated-charge amplifiers at the outputs of both bucket brigades. On the even side, the signal appears at the gate of the output source follower when ϕ_{X1} drops to a low potential. While ϕ_{X1} is high before the next sample appears, this node is cleared by charging it to the reset voltage, V_{DD}. Thus, reset is accomplished when this terminal is clocked synchronously with ϕ_{X1}. The complementary situation applies to the odd output, with signal appearing while ϕ_{X2} is low and reset while ϕ_{X2} is high. The extra half-stage in the even side allows the alternating sequence desired. Normally, the synchronous relationship is obtained by direct connection of ϕ_{X1} to VR_2 and direct connection of ϕ_{X2} to VR_1.

VID_1 and VID_2 are the respective odd and even video output terminals. The video output is that of a source follower. Normally, the output of each source follower is connected to 2KΩ, which is referenced to ground. This configuration provides the proper bias current for the source follower. Figure

4 shows the output voltage across such a load resistor, showing the relationship of video pixel information relative to the superimposed reset clock amplitude. Figure 5 shows output impedance of the source follower as a function of the bias current. This graph can be used to design an interface circuit with suitable DC bias translation (e.g. an emitter-coupled transistor with the base biased near the video output line potential).

4. Line Transfer (LT), Line Reset (LR), and Buffer Gate (V_{Buff})

The fourth element consists of a video line reset switch, LR; a transfer switch, LT; and a buffer gate, V_{Buff}. The reset switch, LR, provides a reference bias for all video lines while all the sensor diodes are integrating. All charges collected on stray capacitances along the video lines and all excess signal charges leaked from the sensor diodes are drained into the sink voltage, V_{DD}, through the LR gate. Therefore, LR functions as an antiblooming and anticrosstalk gate.

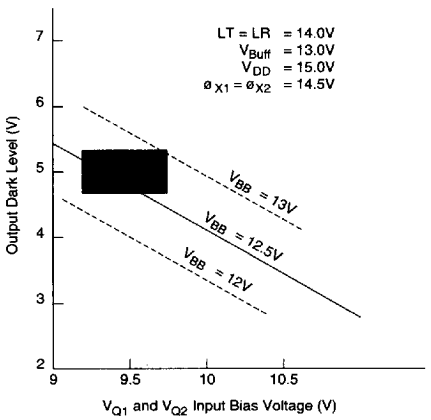


Figure 3. Operation Range of V_{Q1} and V_{Q2} Bias

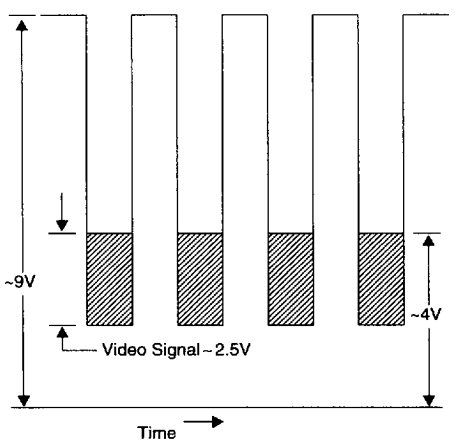


Figure 4. Typical Video Signal Seen Across 2KΩ Load Resistor

Prior to the moment when the dynamic register is to select another row of diodes, the LR gate is turned off and the transfer gate turned on. This makes conditions ready for the signal charge from the next row to be transferred into the BBD registers.

The voltage applied to the LR switch should be equal to or lower than that of LT. This will prevent possible loss of signal charge through LR as a result of threshold voltage mismatch between LR and LT transistors. The effect of different gate potentials on LR and LT results in adding a fixed amount of charge, Q_f, to the video signal, where $Q_f = (\Delta V_G + \Delta V_T)\, C_V$. These quantities ΔV_G and ΔV_T are the gate potential and threshold voltage differences of the LR and LT gates, respectively, and C_V is the capacitance of the video line.

To minimize Q_f a buffer gate V_{Buff} is introduced in front of the LR and LT switches. This buffer gate is biased at a DC potential below the LR and LT "high" potential. The function of this buffer gate is to isolate the video line capacitance C_V from the effect of ΔV_G and ΔV_T. With the introduction of this buffer gate, Q_f becomes $(\Delta V_G + \Delta V_T)\, C_j$, where C_j is the junction capacitance of the n+ diffusion between LR and LT. The capacitance C_j is much smaller than C_V and results in great reduction of Q_f. Normally LR is clocked synchronously

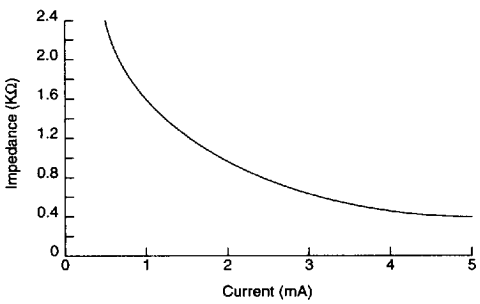
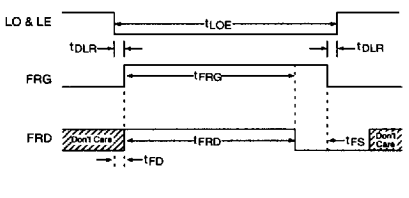


Figure 5. Typical Video Output Impedance Versus Bias Current



	Min	Typ	Max	Remark
t_{DLR}	100 ns			
t_{LOE}				To be consistant with t_{FRG}
t_{FRG}	1.5 ms		2.5 ms	
t_{FRD}	1.5 ms			
t_{FS}	2.50 µs			
t_{FD}	0.1 µs			

Note: Clock rise and fall times are not critical. However it is recommended not to exceed 0.5 µs. While frame reset is active, the reset takes place by performing at least 3 line scans using the BBD registers.

Figure 6. Timing Sequence for Frame Reset

with ϕ_{X1}. However, to avoid crosstalk and to permit adjustment for optimum blooming control, a separate driver is used for LR.

5. Field Select Switches (LO and LE)

The fifth functional element is the field select switches, LO and LE. The LO input terminal controls the gates that switch all the odd-numbered outputs from the Y shift register, and the LE terminal controls the gates that switch the even-numbered outputs. In turn, these Y register outputs control row selection. When the LO line is held at V_{DD}, the odd rows of diodes may be selected by the Y shift register. When the LE line is held at V_{DD}, even rows of diodes may be selected. The selected diodes are connected to the column video lines, which in turn are connected to transport bucket brigades through buffer transistors and the line transfer switches. Typically, the LO or LE, when selected, is switched from a low of 0.4V to a high of V_{DD}. For sequential scan of all lines, both LE and LO are continuously held at V_{DD}.

6. Frame Reset Gate (FRG) and Frame Reset Drain (FRD)

The sixth element consists of the frame reset gate, FRG, and frame reset drain, FRD. This switch provides access to the multiplex switches of all diodes in the matrix and allows the entire frame to be reset simultaneously. Since the diodes in each line are automatically reset when the line is accessed, the frame reset control is not normally used and is held low. However, when a particular exposure is desired, this control may be used to clear the diodes to start a fresh integration cycle by setting the FRG terminal to V_{DD}. When this mode is used, a shutter or pulsed-light input is required because the diodes are sequentially accessed and will thus differ in exposure time if light input is continued during the read-out sequence. With FRG and FRD active, 3 line scans are done to fully recharge both the pixels and video lines through the BBD registers. Depending on the timing or lighting, more line scans may be needed. LR could be used, but a line scan with the BBD registers is then needed to avoid excessive fixed-pattern noise (FPN).

The minimum timing requirements for the frame operation are shown in Figure 6. The longest of the control pulses are LE and LO which are pulsed off during this operation. They should be held negative 200 nanoseconds wider than the frame reset gate, with pulse width overlap as shown in the figure. The FRD can be continuously active, but within and before the trailing edge of FRG, FRD must be pulled to ground to allow the vertical shift register's multiplexing line to discharge. This operation ensures turn-off of the multiplexing switch. Except for FRD, all the clock voltages are set with the low swing at 0.0 +0.25/-0V and at V_{DD} +0/-1V on the high swing. FRD's clock is the same low as called out on the other clocks, but the high end is set to V_{DD} -3 ±0.5V.

Device Operation

Figure 7 shows the timing diagram for the devices in the noninterlaced and continuous mode of operation. It requires two sets of complementary clocks, namely ϕ_{Y1} and ϕ_{Y2} to drive the dynamic shift register, and ϕ_{X1} and ϕ_{X2} to drive the two BBD registers. It also requires an LT clock to control charge transfer from the column video line into the BBD registers. The line reset clock, LR, is the blooming control and has the same timing as ϕ_{X1}. The reset gates, VR_1 and VR_2, are to control the output charge integrators, and are directly tied to ϕ_{X2} and ϕ_{X1}, respectively. The timing relations and rise and fall times of the various clocks are summarized in Table 1.

Before a new row of diodes is selected by the Y shift register, which occurs when ϕ_{Y1} and ϕ_{Y2} change states, the line reset LR should be turned off to prevent signal charge being drained into V_{DD}. The requirement of a certain t_{YD} delay, as shown in Figure 7, warrants this condition. A minimum pulse width of LT is also required to accommodate complete charge transfer from the video line into the BBD register. During the time when the signal charge is being transferred into the BBD register, the clock driving the register must stop at high potential on the buckets receiving charge from the video line. This will cause a deep potential well for the signal charge to flow into. The buckets receiving charge for both the odd and

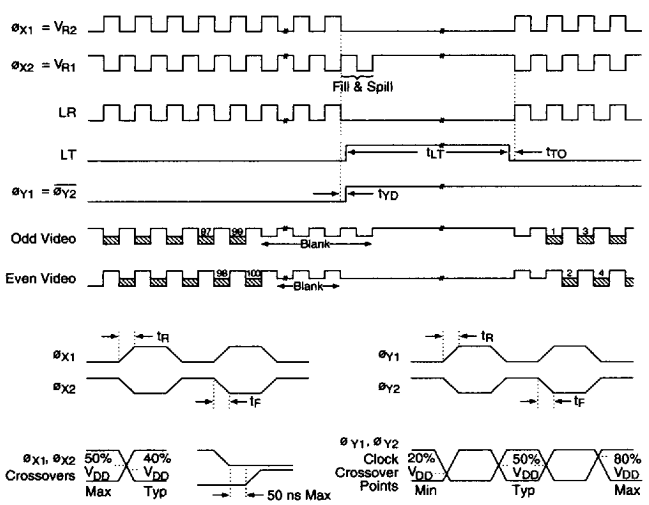


Figure 7. Timing Diagram for RA0100A/RA0128N Noninterlaced Continuous Operation

even transport registers are driven by ϕ_{X2}, and the charge transfer takes place simultaneously for both registers during the time ϕ_{X2} is held high. Note that there is an extra clock of ϕ_{X2} within the LT pulse. The function of this extra clock is to dump the "fat zero" charge of the BBD register into the video line, where it will combine with the signal charge and then spill back together into the BBD register. This "fill and spill" action significantly improves the transfer efficiency of the signal charge.

The LT clock is then shut off before the BBD register shifts the signal charge to the output amplifiers. On the readout, the odd BBD register produces the first pixel. It reads out on the second low-going ϕ_{X2} clock after the transfer period. The second pixel is produced by the even BBD register. Since this even pixel must transfer through an extra half-stage which is controlled by ϕ_{X1}, it is produced when ϕ_{X1} goes low. This provides an easily multiplexed signal by means of a simple external adder-amplifier.

Specifications

Table 1 summarizes the clock timing of Figure 7. Table 2 lists the mechanical specifications of the array. Table 3 and Table 4 are the operating biases and clock amplitudes in accordance with the timing diagram of Figure 7. The capacitances are listed in Table 5. With the exception of supply inputs, such as V_{DD}, the input terminal impedance is essentially capacitive.

Optical Performance

Table 6 lists the optical characteristics and Table 7 summarizes the array output characteristics. The circuit used to obtain the typical performance characteristics is essentially identical to the evaluation circuit offered by Reticon under the designation RC0502A. However, the video processing circuit has not been used. Instead, all measurements have been taken across a 2KΩ load to ground. The optical source for the performance data is a 2870°K tungsten lamp with a Fish-Schurman HA-11 filter. Illumination levels are measured using a detector with a flat response from 370 to 1040 nm.

The spectral response is the standard silicon photodiode response shown in Figure 8. In contrast with CCD detector arrays, no semi-transparent electrode covers the sensors, hence, no interference patterns appear in the pass band and no additional attenuation occurs at short wavelengths.

The transfer function, Figure 9, shows a linear optical-to-electrical relationship with dynamic range exceeding 100:1. This linear relationship depends on application of the proper electrode potentials, especially those for V_{Buff} and the line reset pulse level, LR. Improper potentials can cause substantial nonlinearity.

Antiblooming

Blooming is defined as excess charge integrated on the column video line during a sample period as a result of excess exposure. Blooming is generally less severe in the RA0100A and RA0128N type of structure as compared to typical CCD structures because the sensor elements are separate and distinct p-n junction photodiodes. However, since there are common video lines for each column of diodes, a vertical-blooming effect is observed when some excess charge is collected.

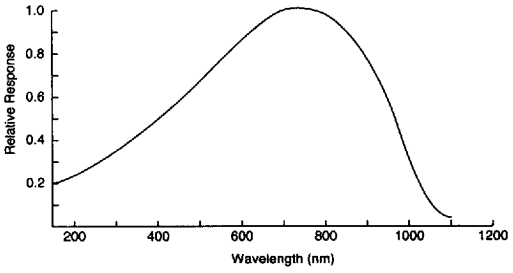


Figure 8. Spectral Response

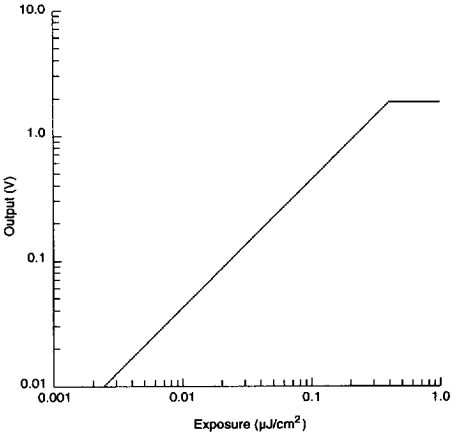


Figure 9. Typical Output Versus Exposure (2870°K Tungsten Lamp with HA-11 Filter)

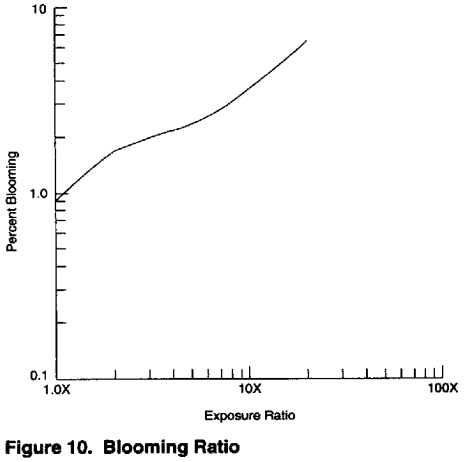


Figure 10. Blooming Ratio

Figure 10 is a curve of this ratio, i.e., points on the horizontal axis represent multiples of saturation exposure and points on the vertical axis represent the output of a nonexposed diode located 15 diodes away from the exposure center sharing the same column video line. The output is normalized to the output voltage of a saturated diode and plotted in percent of the saturation voltage. The exposed area is circular with a diameter of approximately 10 diodes.

Evaluation Circuit Board, RC0502A

The RC0502A evaluation circuit board is available from Reticon. It contains all required drive and amplifier circuitry and is recommended for first-time array evaluation. The circuit board measures approximately 4.5 x 6.5 inches in size and is terminated by a standard dual 22-pin printed circuit board edge connector.

Table 1. Clock and Control Line Timing

Parameters	Sym	Min	Typ	Max	Units
Continuous	t_{LT}	2.5		4	µs
operation	t_{TO}	0	30		ns
	t_{YD}	0	30		ns
$ø_{X1}$, $ø_{X2}$ rise time	t_R	20	60		ns
$ø_{X1}$, $ø_{X2}$ fall time	t_F	20	60		ns
$ø_{Y1}$, $ø_{Y2}$ rise time	t_R	20	60		ns
$ø_{Y1}$, $ø_{Y2}$ fall time	t_F	20	60		ns
Clock crossing $ø_{X1}$, $ø_{X2}$		0*	40	50	% V_{DD}
Clock crossing $ø_{Y1}$, $ø_{Y2}$		20	50	80	% V_{DD}

* Note: Clocks may be nonoverlapping with a maximum of 50 nanoseconds dead time between rising and falling edges.

Table 2. Array Mechanical Specifications

	RA0100A	RA0128N	Units
Number of diodes	10000	16384	
Diode X, Y center-to-center spacing	60/2.36	60/2.36	µm/mils
Diode sensing area	2562	2562	$µm^2$
Package size (24-pin DIP)	.6 x 1.2	.6 x 1.2	inch

Table 3. DC Voltage Requirements

Parameters	Sym	Min	Typ	Max	Units
Supply voltage	V_{DD}	12	15	16	V DC
Quiescent current	I_{DD}	6	8	10	mA
Transport bias	V_{BB}	V_{DD}-2V	V_{DD}-2.0V	V_{DD}-1V	V DC
Isolation gate	V_{Buff}	V_{DD}-2V	V_{DD}-1.5V	V_{DD}	V DC
BBD input	V_{Q1},V_{Q2}	9.2V	9.5V	10.5	

Note: All voltages are measured with respect to common (ground/substrate)

Table 4. Clock and Control Voltage Requirements

Parameters	Conditions	Sym	Min	Typ	Max	Units
X-Clock	High state	$ø_{X1}$,$ø_{X2}$	V_{DD}-1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			120		pF
Y-Clock	High state	$ø_{Y1}$, $ø_{Y2}$	V_{DD}-1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			25		pF
End-of-frame	High state	E_{OF}			V_{DD}	V DC
opendrain	Low state (sync current)				1.5	mA
	Capacitance			5		pF
Line transfer	High state	$ø_{LT}$	V_{DD}-1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			27		pF
Line reset	High state	$ø_{LR}$	V_{DD}-1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			27		pF
Video reset	High state	$ø_{VR1}$, $ø_{VR2}$	V_{BB}+1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			5		pF
Y-Start	High state					
	Low state					
	Capacitance			4		pF

Table 5. Typical Terminal Capacitance with 10V Bias

Pin	Sym	RA0100A	RA0128N	Units
2	EOF	5	5	pF
3	LO	20	22	pF
4	LE	20	22	pF
5	LR	22	27	pF
7	VR_1	5	5	pF
8	ϕ_{X1}	55	60	pF
9	ϕ_{X2}	55	60	pF
10	FR	14	15	pF
12	VID_1	5	5	pF
13	VID_2	5	5	pF
16	ϕ_{X2}	55	60	pF
17	ϕ_{X1}	55	60	pF
18	VR_2	5	5	pF
21	LT	22	27	pF
22	Y_{Start}	4	4	pF
23	ϕ_{Y1}	20	25	pF
24	ϕ_{Y2}	20	25	pF

Table 6. Optical Characteristics

Parameters	Conditions	Sym	Min	Typ	Max	Units
Responsitivity	Peak-to-peak			13.5		$V/\mu J/cm^2$
Saturation exposure [1,2]		E_{SAT}		.155		$\mu J/cm^2$
Noise equivalent exposure		E_{NE}		.0015		$\mu J/cm^2$
Photoresponse nonuniformity [1,2,3]					±10	% V_{SAT}

Notes:
1. Measured with typical clock and voltage requirements
2. Measured using 2870°K light source with HA-11 filter at 20 ms frame period
3. Ignoring first and last columns/first and last lines

Table 7. Output Characteristics

Parameters	Sym	Min	Typ	Max	Units
Impedance	Z_O		2		KΩ
Saturation voltage [1, 2]	V_{SAT}		2.5		V
Pixel rate	F_{SAMP}	0.2		10	MHz
Baseline reference [1, 4]		6		8	V
Fixed pattern noise [1, 4, 5]				20	mV
Average leakage [1, 3]			20	80	mV

Notes:
1. Measured with typical clock and voltage requirements
2. Measured using 2870°K light source with HA-11 filter at 20 ms frame period
3. Measured at 25°C, 40 ms frame period
4. Measured at 20 ms frame period
5. Ignoring first and last columns/first and last lines

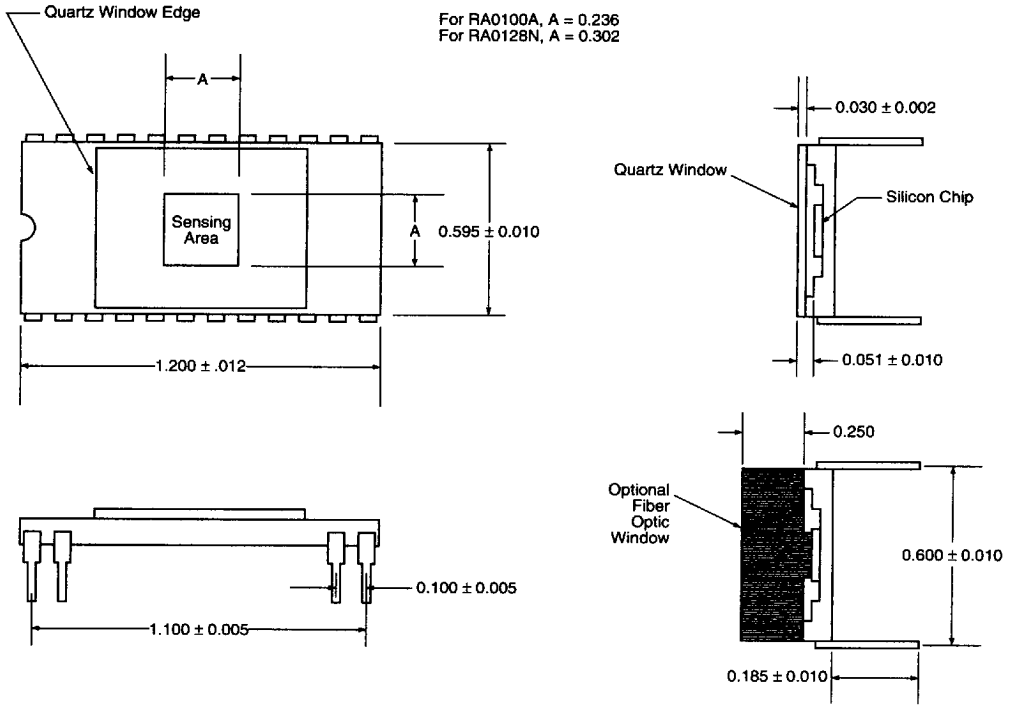


Figure 11. Package Dimensions. Dimensions are in inches except where millimeters (mm) are indicated.

Ordering Information

Array	Ordering Number	Evaluation Circuit
RA0100A (quartz) (0 defects)	RA0100AAQ-011	RC0502ANA-011
RA0100A (quartz) (1-9 defects)	RA0100AAQ-020	RC0502ANA-011
RA0100A (fiber optic) (0 defects)	RA0100AAF-011	RC0502ANA-011
RA0100A (fiber optic) (1-9 defects)	RA0100AAF-020	RC0502ANA-011
RA0128N (quartz) (0 defects)	RA0128NAQ-011	RC0502ANA-020
RA0128N (quartz) (1-9 defects)	RA0128NAQ-020	RC0502ANA-020
RA0128N-011(fiber optic) (0 defects)	RA0128NAF-011	RC0502ANA-020
RA0128N-020 (fiber optic) (1-9 defects)	RA0128NAF-020	RC0502ANA-020

Note: A defect is defined as any diode out of specification.

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