87C51GA/87C51GA-1/87C51GA-2 CHMOS 8-BIT MICROCONTROLLER WITH A/D CONVERTER AND 4 KBYTES OF EPROM

87C51GA—3.5 MHz to 12 MHz, V_{CC} = 5V ± 10%
87C51GA-1—3.5 MHz to 16 MHz, V_{CC} = 5V ± 10%
87C51GA-2—0.5 MHz to 12 MHz, V_{CC} = 5V ± 10%

- 8-Channel 8-Bit A/D Converter
- Oscillator Fail Detect
- 16-Bit Watchdog Timer
- Synchronous Serial Channel
- 2-Level Program Memory Lock
- Boolean Processor
- 128-Byte Data RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 7 Interrupt Sources
- High Performance CHMOS EPROM
- TTL- and CMOS-Compatible Logic
- Quick-Pulse Programming™
- Full-Duplex Serial Channel
- 64K External Program Memory Space
- 64K External Data Memory Space
- Idle and Power Down Modes
- ONCE™ Mode Facilitates System Testing
- DIP, CERQUAD and PLCC Packaging Available
- Hysteresis on Ports 1 and 3
- Program Memory Lock

The 87C51GA combines all the features of the 87C51 with these additional enhancements: an 8-channel, 8-bit A/D converter; a 16-bit watchdog timer; oscillator fail detect circuitry; and a half-duplex synchronous serial port. The 87C51 family features include: 4 Kbytes of EPROM; 128 bytes of RAM; 32 I/O lines; two 16-bit programmable timer/counters; a seven source two-level interrupt structure; a full-duplex serial port; on-chip oscillator and clock circuitry; and two power reduction modes. The 80C51GA is the ROMless part and the 83C51GA is the masked ROM part.

The 87C51GA is fabricated on Intel's CHMOS II-E process and is functionally compatible with the standard 8051 Family of HMOS and EPROM products. CHMOS II-E is a technology which combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. This combination expands the effectiveness of the powerful 8051 architecture and instruction set.

The 87C51GA EPROM array uses a modified Quick-Pulse Programming Algorithm, by which the entire 4-Kbyte array can be programmed in about 12 seconds. The on-chip Program Memory is electrically programmed and can be erased by exposure to ultra-violet light.

The extremely low operating power, along with the two software selectable reduced power modes, Idle and Power Down, make this part very suitable for low power applications. The Idle mode freezes the CPU while allowing the RAM, timer/counters, serial port, A/D converter, watchdog timer, oscillator fail detect and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

October 1988
Order Number: 270562-002

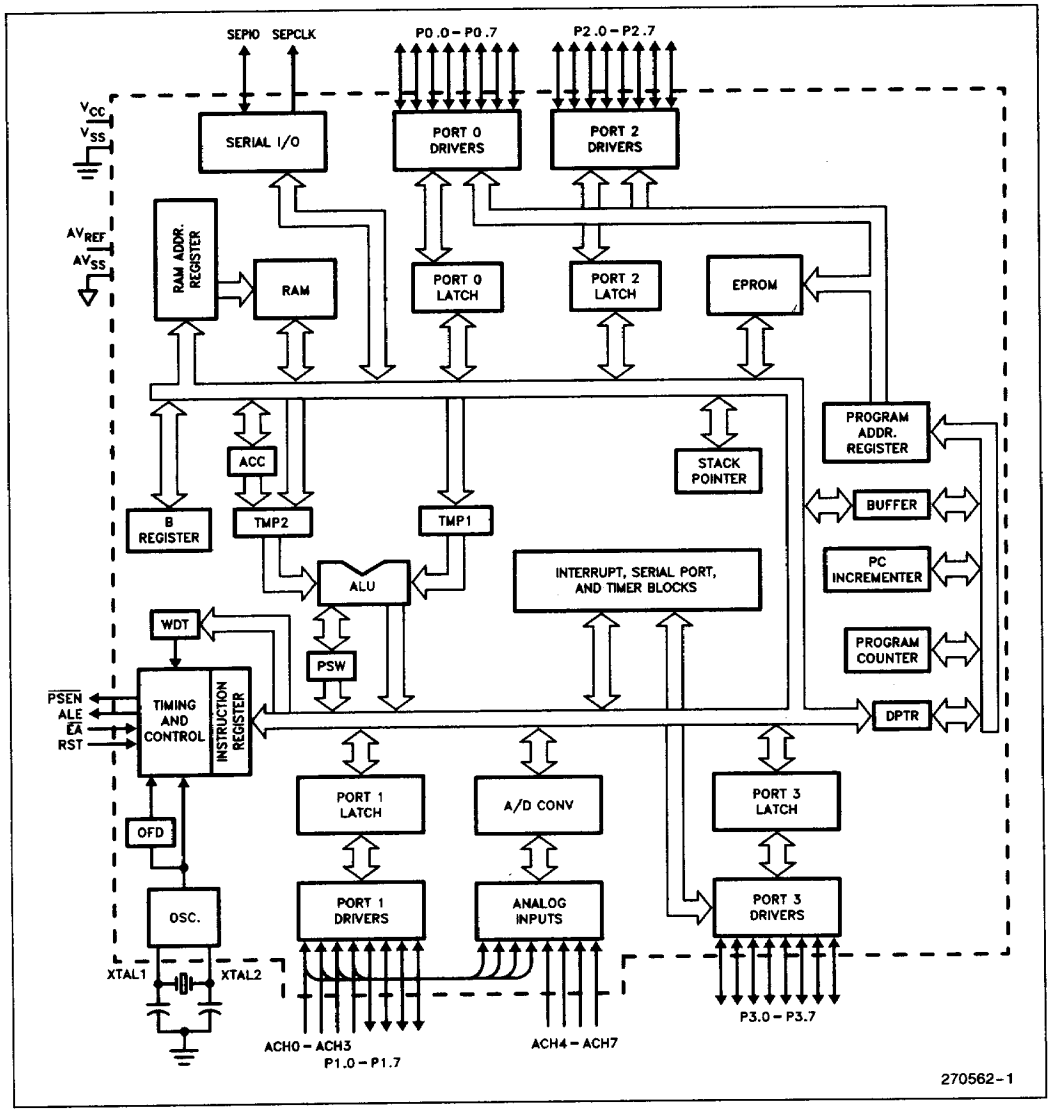


Figure 1. Block Diagram

PACKAGES

Part	Prefix	Package Type
87C51GA/	C	48-Pin Ceramic
87C51GA-1/	P	48-Pin Plastic
87C51GA-2	N	52-Pin PLCC
	J	52-Pin Cerquad

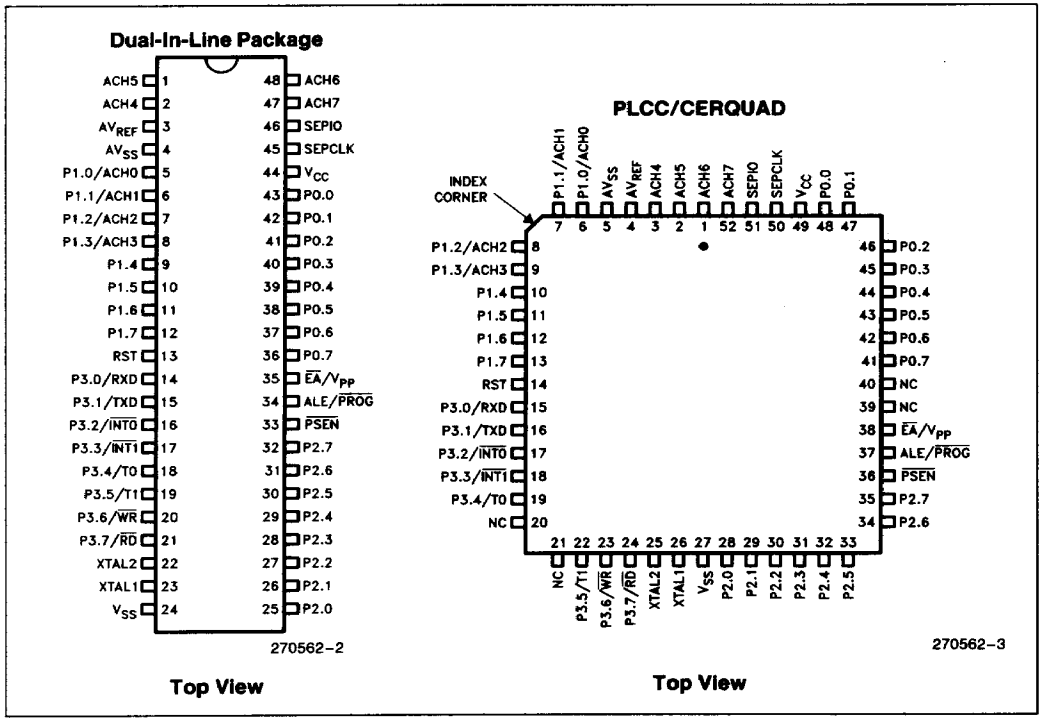


Figure 2. Pin Connections

PIN DESCRIPTION

V_{CC}: Supply voltage during normal, Idle, and Power Down operations.

V_{SS}: Circuit ground.

AV_{REF}: Analog reference voltage.

AV_{SS}: Analog ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit I/O port with internal pullups on the 4 high-order bits which can be used for normal I/O. The 4 low-order bits are shared with 4 of the analog inputs and as such, are input only. High-order Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state

can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL} on the data sheet) because of the internal pullups. Outputs to the 4 low-order bits have no effect and are ignored. Port 1 inputs are equipped with Schmitt trigger logic with 400 mV of hysteresis and TTL compatible input specifications. Port 1 I/O is explained in the following list:

P1.7—quasi-bidirectional
P1.6—quasi-bidirectional
P1.5—quasi-bidirectional
P1.4—quasi-bidirectional
P1.3—digital input/ACH3—Analog CHannel 3
P1.2—digital input/ACH2—Analog CHannel 2
P1.1—digital input/ACH1—Analog CHannel 1
P1.0—digital input/ACH0—Analog CHannel 0

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

ACH4–ACH7: Analog CHannel 4–7. These are the four high-order analog inputs which have dedicated input pins.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s.

During accesses to External Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives some control signals and the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL} on the data sheet) because of the pullups. Port 3 inputs are equipped with Schmitt Trigger logic with 400 mV of hysteresis and TTL compatible input specifications.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Pin	Name	Alternate Function
P3.0	RXD	Serial Input Line
P3.1	TXD	Serial Output Line
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 External Input
P3.5	T1	Timer 1 External Input
P3.6	$\overline{WR}$	External Data Memory Write Strobe
P3.7	$\overline{RD}$	External Data Memory Read Strobe

SEPIO: Serial Expansion Port I/O bit. This bit is an output for transmission and an input for reception of half-duplex synchronous serial data.

SEPCLK: Serial Expansion Port Clock (Output-only). This clocking signal is an output for transmission and reception of synchronous serial data.

RST: Reset Input. A logic high on this pin resets the device. An internal pulldown resistor permits a power-on reset to be generated using only an external capacitor to V_{CC}.

ALE/$\overline{PROG}$: Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to External Data Memory.

$\overline{PSEN}$: Program Store Enable is the Read strobe to External Program Memory. When the 87C51GA is executing from Internal Program Memory, $\overline{PSEN}$ is inactive (high). When the device is executing code from External Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory.

$\overline{EA}$/V_{PP}: External Access Enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the 87C51GA to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however that if either of the Lock Bits is programmed, the logic level at $\overline{EA}$ is internally latched during reset.

$\overline{EA}$ must be strapped to V_{CC} for internal program execution.

This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier and input to the internal clock generating circuits.

XTAL2: Output from the inverting oscillator amplifier.

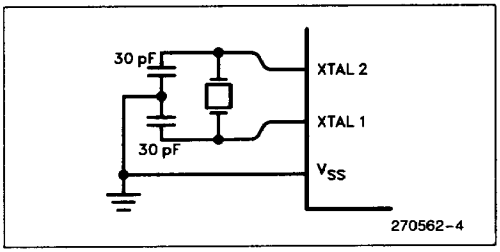


Figure 3. Using the On-Chip Oscillator

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the Special Function Registers remain

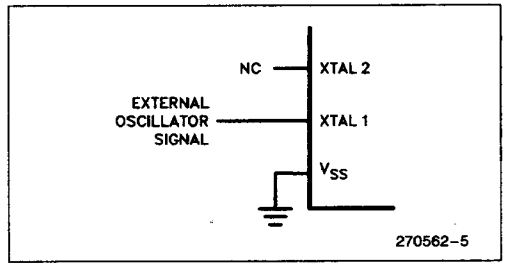


Figure 4. External Clock Drive

unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset. Note that the Watchdog Timer is active during Idle Mode. See Design Considerations.

POWER DOWN MODE

In Power Down Mode, the oscillator is stopped and all on-chip functions cease except that the on-chip RAM content is maintained. The mode is invoked by software. The Oscillator Fail Detect circuitry should be disabled before entering Power Down.

The Power Down Mode can be terminated only by a hardware reset. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

A/D Converter

The A/D Converter is an 8-bit successive approximation device with the following features:

8 User Selectable Analog Input Channels
User Selectable Internal Sample and Hold
User Selectable Conversion Speed Control
Nominal Conversion Speed: 22 μs at 12 MHz
Accuracy ± 1 LSB (LSB = 20 mV)
Input Signal Range, Nominally 0V to 5V (AV_{SS} to V_{REF})
Interrupt Driven

Table 1. Status of the External Pins during Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Like all 8051 Family functions, the A/D converter is controlled by reads and writes to the Special Function Registers. Refer to the *"Hardware Description of the 8XC51GA"* for further information.

Watchdog Timer (WDT)

The Watchdog Timer provides the ability to recover from hardware or software malfunctions by forcing the part into reset. It has the following features:

16-bit Synchronous Counter; Counts Machine Cycles
Asynchronous Reset when Counter = FFFFH (65.5 ms at 12 MHz)
Cleared and Initiated by Reset or Software Clear
Operates in Normal and Idle Mode

Oscillator Fail Detect (OFD)

The Oscillator Fail Detect circuitry triggers a reset if the oscillator frequency is lower than the OFD trigger frequency. It can be disabled by software during Power Down Mode and has the following features.

OFD Trigger Frequency: 20 KHz to 400 KHz
Asynchronous Reset for at Least 4 Machine Cycles
Functions in Normal and Idle Modes
Reactivated by Reset after Software Disable

Serial Expansion Port (SEP)

The Serial Expansion Port is a half-duplex synchronous serial interface with the following features:

Four Clock Frequencies
—XTAL/12
—XTAL/24
—XTAL/48
—XTAL/96

Four Interface Modes
—Rising Edges
—Falling Edges
—High Level
—Low Level
Interrupt Driven

ONCE™ MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 87C51GA without the 87C51GA having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pulling ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Holding ALE low as RST is deactivated.

While the device is in the ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 87C51GA is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

DESIGN CONSIDERATIONS

It should be noted that when Idle Mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

During Idle Mode, the Watchdog Timer must periodically be reset under program control to hold off a Watchdog timeout from generating a device reset.

Ambient light is known to affect the internal memory contents during operation. If the 87C51GA application requires the part to be run under ambient lighting, an opaque label should be placed over the window to exclude light.

In this device, ports are reset asynchronously: Port 0 resets to a high impedance (floating) and Ports 1.4–1.7, Port 2 and Port 3 reset to an output high even in the absence of an active internal clock. The 8 analog inputs, ACH0–7, are input-only high-impedance (tri-state) inputs.

ABSOLUTE MAXIMUM RATINGS (1)

Ambient Temperature under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin to V_{SS} ...−0.5V to V_{CC} + 0.5V
Voltage on V_{CC} to V_{SS} .....−0.5V to +6.5V
Maximum I_{OL} per I/O Pin .....15 mA
Power Dissipation.....1.0W*

* Based on package heat transfer limitations, not device power consumption.

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = 5V ±10%, V_{SS} = 0V

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
VT+	High-Going Threshold (Ports 1, 3)	1.1 (3)	2.0	V	
VT−	Low-Going Threshold (Ports 1, 3)	0.6	1.2 (3)	V	
V_{HYS}	Hysteresis (Ports 1, 3)	0.4 (3)		V	
V_{IL}	Input Low Voltage (except $\overline{EA}$)	−0.5	0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage ($\overline{EA}$)	−0.5	0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (4) (Ports 1, 2, 3)		0.3	V	I_{OL} = 100 μA (1)
			0.45	V	I_{OL} = 1.6 mA (1)
			1.0	V	I_{OL} = 3.5 mA (1)
V_{OL1}	Output Low Voltage (4) (Port 0, ALE, $\overline{PSEN}$)		0.3	V	I_{OL} = 200 μA (1)
			0.45	V	I_{OL} = 3.2 mA (1)
			1.0	V	I_{OL} = 7 mA (1)
V_{OH}	Output High Voltage (Ports 1, 2, 3)	V_{CC} − 0.3		V	I_{OH} = −10 μA
		V_{CC} − 0.7		V	I_{OH} = −30 μA
		V_{CC} − 1.5		V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in Ext Bus Mode, ALE, $\overline{PSEN}$) (2)	V_{CC} − 0.3		V	I_{OH} = −200 μA
		V_{CC} − 0.7		V	I_{OH} = −3.2 mA
		V_{CC} − 1.5		V	I_{OH} = −6.5 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)		−50	μA	V_{IN} = 0.45V
I_{TL}	Logical 1 to 0 Transition (Ports 1, 2, 3)		−650	μA	V_{IN} = 2V

ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

DC CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ (Continued)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current (Ports 0, $\overline{EA}$)		±10	µA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (ACH0–7)		±3	µA	$0 < V_{IN} < V_{REF}$
RRST	Reset Pulldown Resistor	50	225	KΩ	
CIO	Pin Capacitance		10	pF	Test Freq. = 1 MHz $T_A = 25°C$
	Power Supply Current				
I_{CC}	Operating, 12 MHz (5)		40	mA	
I_{DL}	Idle Mode, 12 MHz (5)		10	mA	(5)
I_{PD}	Power Down Mode		TBD	µA	
I_{REF}	Reference Voltage = 5.12V		10	mA	

NOTES:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OLS} of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst case (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. During reset, V_{OH1} for ALE and $\overline{PSEN}$ may fall below the specified value.
3. $VT+_{min}$ and $VT-_{max}$ cannot occur together in the same part as hysteresis is guaranteed to be 400 mV Minimum. See Figure 5.
4. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port —
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink current greater than the listed test conditions.
5. See Figure 6.
6. See Figures 7 through 10 for I_{CC} test conditions. Minimum V_{CC} for Power Down mode is 2.0V.

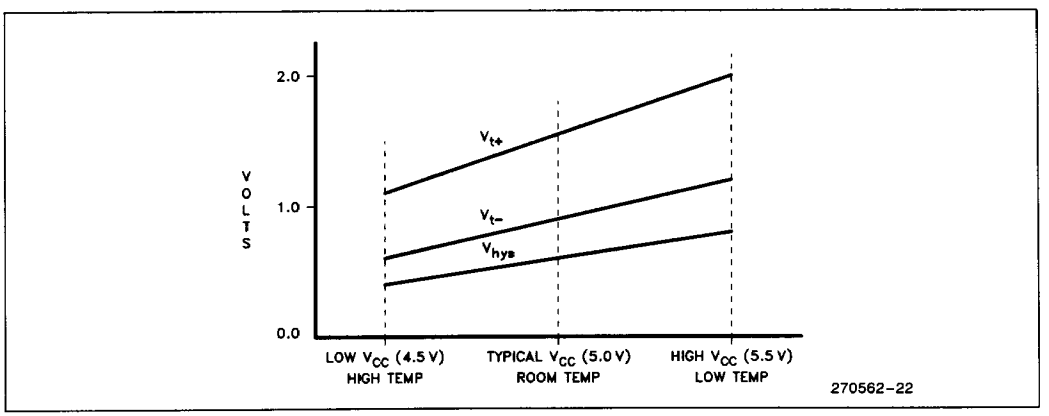
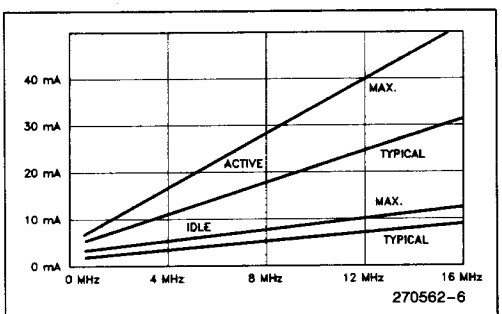


Figure 5. Port 1 and 3 Hysteresis



I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} MAX = 3.0 × FREQ + 4.1
Idle Mode
I_{CC} MAX = 0.65 × FREQ + 2.1
Where FREQ is in MHz, I_{CC} Max is given in mA.

Figure 6. I_{CC} vs Frequency valid only within frequency specifications of the device under test.

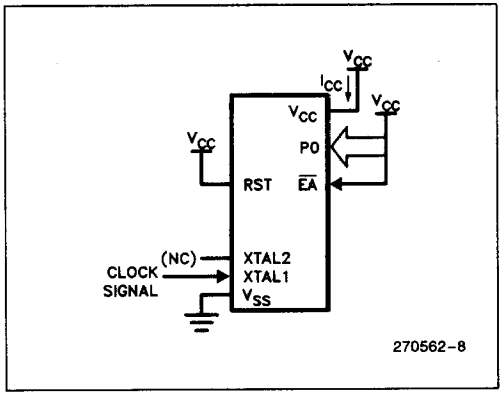


Figure 7. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

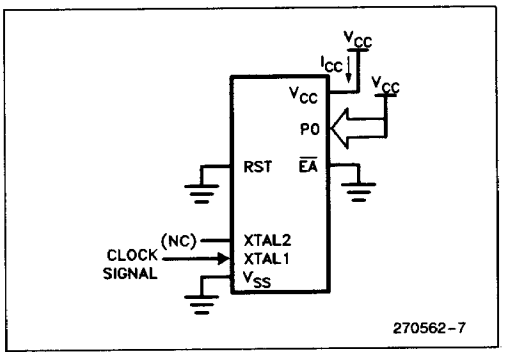


Figure 8. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

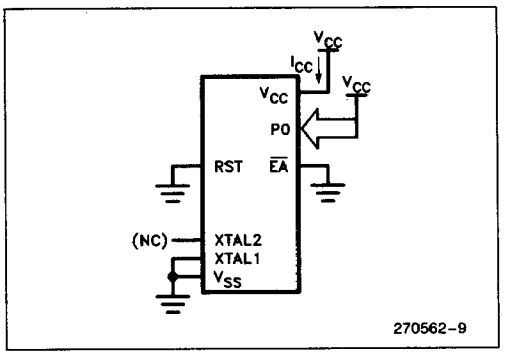


Figure 10. I_{CC} Test Condition, Power Down Mode. V_{CC} = 2.0V to 5.5V

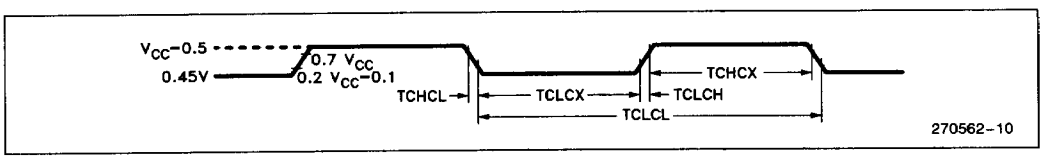


Figure 9. Clock Signal Waveform for I_{CC} tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

Example:

TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{PSEN}$ Low.

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V, load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF

ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

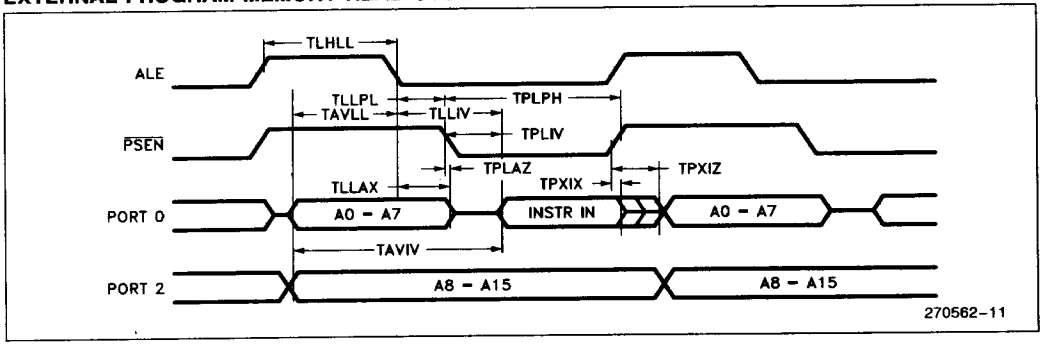
Symbol	Parameter	12 MHz Clock		Variable Clock		Unit
		Min	Max	Min	Max	
1/TCLCL	Oscillator Freqquency 87C51GA 87C52GA-1 87C51GA-2			 3.5 3.5 0.5	 12 16 12	MHz
TLHLL	ALE Pulse Width	127		2 TCLCL − 40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL − 40		ns
TLLAX	Address Hold after ALE Low	53		TCLCL − 30		ns
TLLIV	ALE Low to Valid Instr In		234		4 TCLCL − 100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	53		TCLCL − 30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3 TCLCL − 45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		145		3 TCLCL − 105	ns
TPXIX	Input Instr Hold after $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float after $\overline{PSEN}$		59		TCLCL − 25	ns
TAVIV	Address to Valid Instr In		312		5 TCLCL − 105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6 TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6 TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5 TCLCL − 165	ns
TRHDX	Data Hold after $\overline{RD}$	0		0		ns
TRHDZ	Data Float after $\overline{RD}$		107		2 TCLCL − 60	ns
TLLDV	ALE Low to Valid Data In		517		8 TCLCL − 150	ns
TAVDV	Address to Valid Data In		585		9 TCLCL − 165	ns

ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

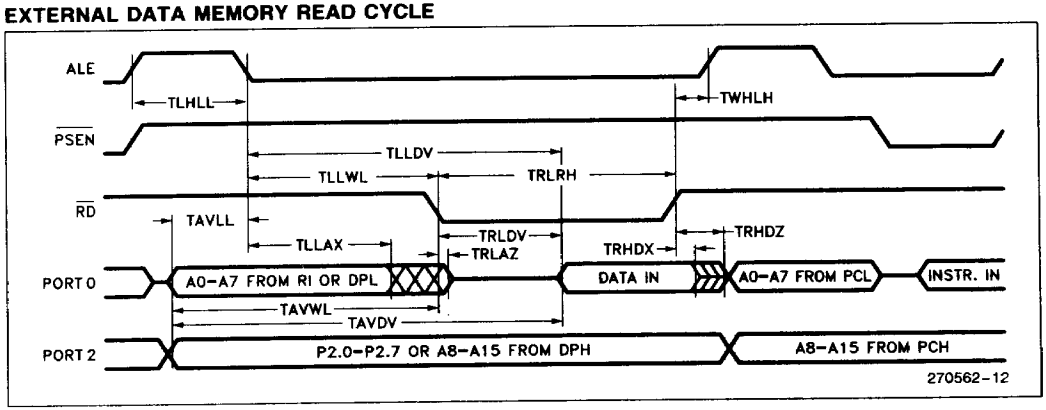
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS (Continued)

Symbol	Parameter	12MHz Clock		Variable Clock		Unit
		Min	Max	Min	Max	
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3 TCLCL − 50	3 TCLCL + 50	ns
TAVWL	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	203		4 TCLCL − 130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL − 50		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL − 50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL − 40	TCLCL + 40	ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL − 150		ns

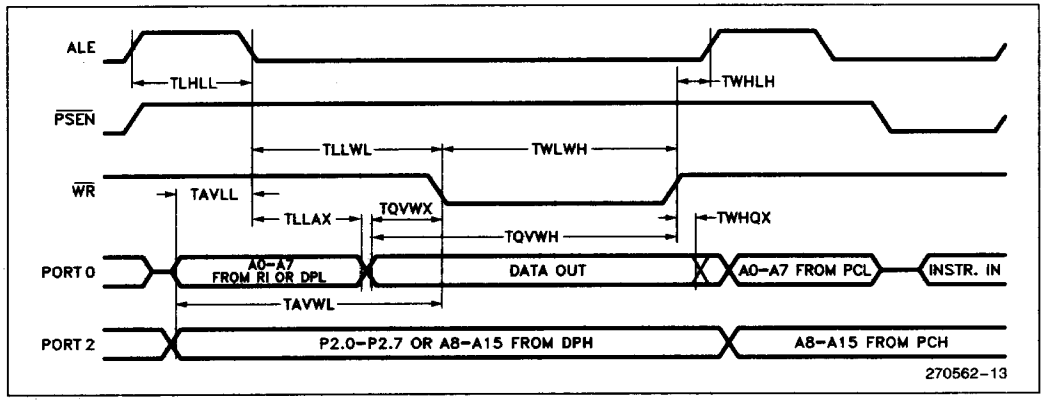
EXTERNAL PROGRAM MEMORY READ CYCLE



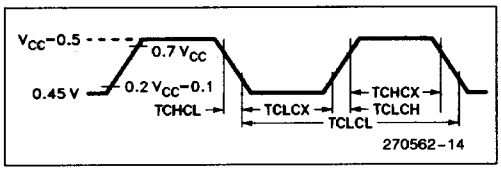
EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE



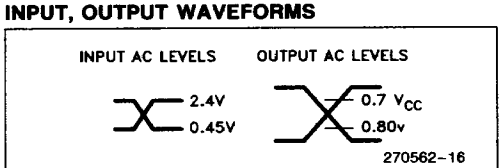
EXTERNAL CLOCK DRIVE WAVEFORM



EXTERNAL CLOCK DRIVE

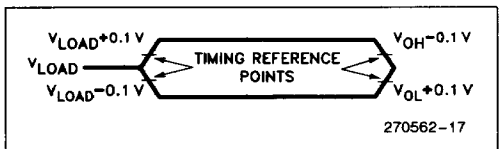
Symbol	Parameter	Min	Max	Unit
1/TCLCL	Oscillator Frequency			
	87C51GA	3.5	12	MHz
	87C51GA-1	3.5	16	MHz
	87C51GA-2	0.5	12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

A.C. TESTING INPUT: INPUT, OUTPUT WAVEFORMS



Input timings are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Output timing measurements are made at 0.7 V_{CC} for a logic "1" and 0.8V for a logic "0".

FLOAT WAVEFORM



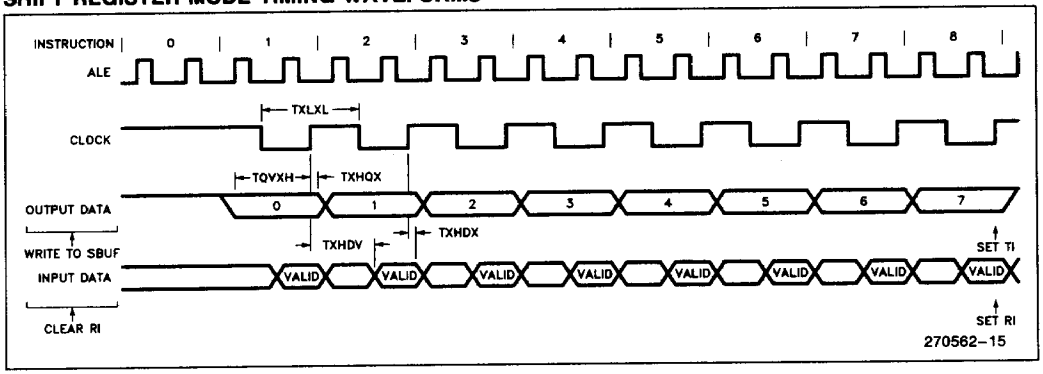
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

SERIAL TIMING—SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to 70°C; V_{CC} = 5V ±10%, V_{SS} = 0V; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Osc.		Variable Oscillator		Unit
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12 TCLCL		µs
TQVXH	Output Data Setup to Clock Rising Edge	700		10 TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2 TCLCL − 117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10 TCLCL − 133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



A TO D CHARACTERISTICS

The absolute conversion accuracy is dependent on the accuracy of V_{REF}. The specifications given below assume adherence to the Operating Conditions section of this data sheet. Testing is done at $V_{REF} = 5.12V$.

An A/D Glossary of Terms is available at the end of this data sheet.

OPERATING CONDITIONS

V_{CC}, V_{REF} ..... 4.5V to 5.5V
V_{SS}, AV_{SS} 0V
ACH0–7 ..... AV_{SS} to V_{REF}
T_A ..... 0°C to +70°C
F_{OSC} ..... 0.5 MHz to 16.0 MHz
Test Conditions: V_{REF} 5.12V
V_{CC} 5.0V

A/D CONVERTER SPECIFICATIONS

Parameter	Minimum	Typical	Maximum	Unit**	Notes
Resolution	256 8		256 8	Levels Bits	
Absolute Error	0		±1	LSB	
Full Scale Error		−0.5 ± 0.5		LSB	
Zero Offset Error		±0.5		LSB	
Non-Linearity	0		±1	LSB	
Differential Non-Linearity	0		±½	LSB	
Channel-to-Channel Variation	0		±0.4	LSB	
Repeatability		±0.25		LSB	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity		 0.003 0.003 0.003		 LSB/°C LSB/°C LSB/°C	 1 1 1
Off Isolation			−60	dB	1, 2, 3
Feedthrough		−60		dB	1, 2
V_{CC} Power Supply Rejection		−60		dB	1, 2
Input Resistance	1K		5K	Ω	1
D.C. Input Leakage	0		3.0	μA	

NOTES:
* These values are expected for most parts at 25°C
** An "LSB", as used here, has a value of approximately 20 mV.
1. These values are not tested in production and are based on theoretical estimates and laboratory tests.
2. DC to 100 KHz
3. Multiplexer Break-Before-Make Guaranteed.

EPROM CHARACTERISTICS

The 87C51GA is programmed by a modified Quick-Pulse Programming algorithm. It differs from older methods in the value used for V_{PP} (Programming Supply Voltage) and in the width and number of the ALE, $\overline{PROG}$ pulses.

The 87C51GA contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C51GA manufactured by Intel.

Table 2 shows the logic levels for reading the signature byte, and for programming the Program Memory, the Encryption Table, and the Lock Bits. The circuit configuration and waveforms for Quick-Pulse Programming are shown in Figures 11 and 12. Figure 13 shows the circuit configuration for normal Program Memory verification.

Table 2. EPROM Programming Modes

Mode	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read Signature	1	0	1	1	0	0	0	0
Program Code Data	1	0	0*	V_{PP}	1	0	1	1
Verify Code Data	1	0	1	1	0	0	1	1
Pgm Encryption Table	1	0	0*	V_{PP}	1	0	1	0
Pgm Lock Bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm Lock Bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:
"1" = Valid high for that pin
"0" = Valid low for that pin
"V_{PP}" = +12.75V ±0.25V
*ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100 μs (±5 μs) and high for a minimum of 10 μs.

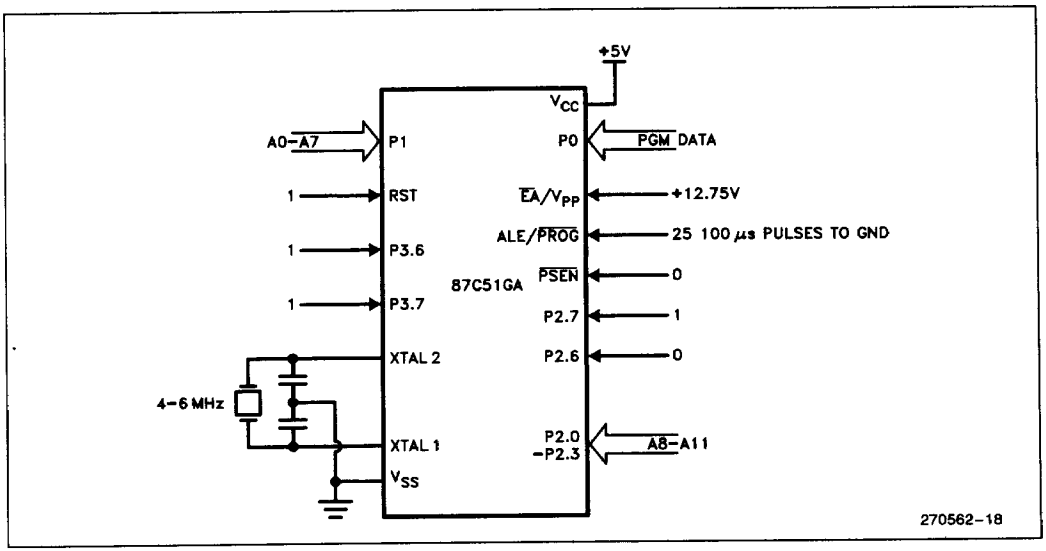


Figure 11. Programming Configuration

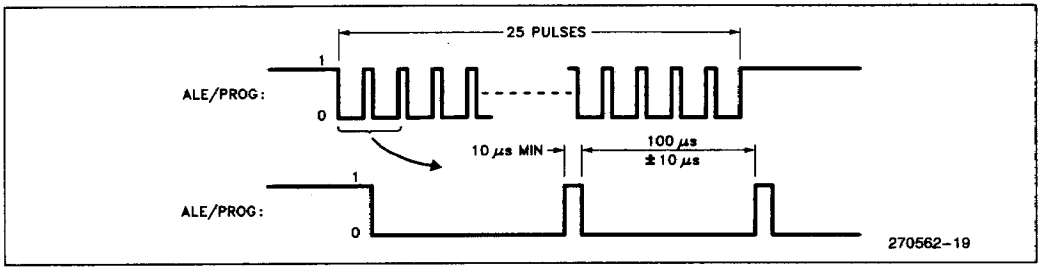


Figure 12. $\overline{\text{PROG}}$ Waveforms

Quick-Pulse Programming™

The setup for Microcontroller Quick-Pulse Programming is shown in Figure 11. Note that the 87C51GA is running with a 4 MHz to 6 MHz oscillator. The reason the oscillator must be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to Ports 1 and 2, as shown in Figure 11. The code byte to be programmed into that location is applied to Port 0. RST, $\overline{\text{PSEN}}$, and pins of Ports 2 and 3 specified in Table 2 are held at the "Program Code Data" levels indicated in Table 2. Then ALE/$\overline{\text{PROG}}$ is pulsed low 25 times as shown in Figure 12.

To program the Encryption Table, repeat the 25-pulse programming sequence for addresses 0 through 1FH, using the "Pgm Encryption Table" levels. Don't forget that after the Encryption Table is programmed, verify cycles will produce only encrypted data.

To program the Lock Bits, repeat the 25-pulse programming sequence using the "Pgm Lock Bit" levels. After one Lock Bit is programmed, further programming of the Code Memory and Encryption Table is disabled. However, the other Lock Bit can still be programmed.

Note that the $\overline{\text{EA}}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

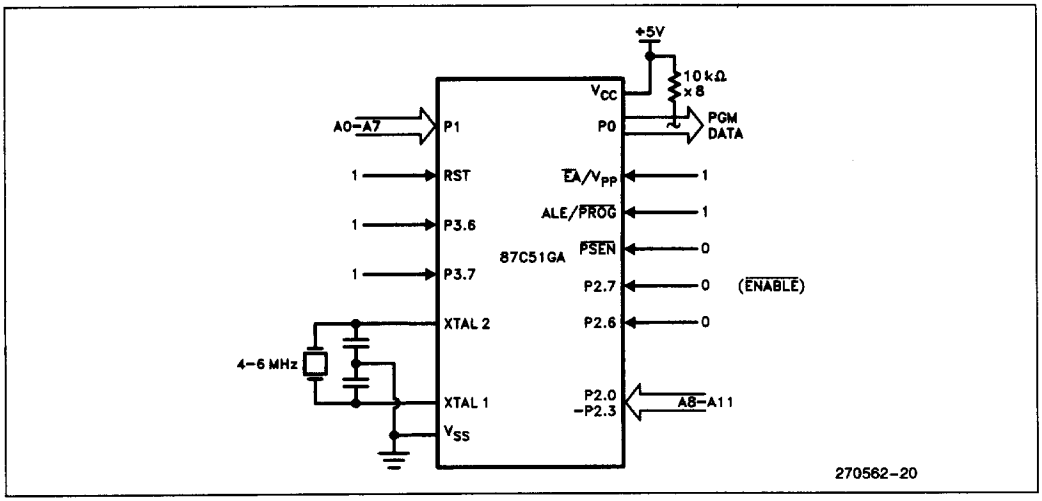


Figure 13. Program Verification

Program Verification

If Lock Bit 2 has not been programmed, the on-chip Program Memory can be read out for program verification. The address of the Program Memory location to be read is applied to Ports 1 and 2 as shown in Figure 13. The other pins are held at the "Verify Code Data" levels indicated in Table 2. The contents of the addressed location will be emitted on Port 0. External pullups are required on Port 0 for this operation. Detailed timing specifications are shown in later sections of this data sheet.

If the Encryption Table has been programmed, the data presented at Port 0 will be the Exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the Encryption Table contents in order to correctly decode the verification data. The Encryption Table itself cannot be read out.

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 2, and which satisfies the timing specifications, is suitable.

EPROM Program Lock

The two-level Program Lock system consists of two Program Lock bits and a 32 byte Encryption Array which are used to protect the program memory against software piracy.

Encryption Array

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encrypted Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in it's original, unmodified form.

Program Lock Bits

Also included in the EPROM Program Lock scheme are two Program Lock Bits which are programmed as shown in Table 2.

Table 3 outlines the features of programming the Lock Bits.

Erasing the EPROM also erases the Encryption Array and the Program Lock Bits, returning the part to full functionality.

Table 3. Program Lock Bits and their Features

Program Lock Bits LB1	LB2	Logic Enabled
U	U	No Program Lock features enabled. (Code Verify will still be encrypted by the Encryption Array.)
P	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled.
P	P	Same as above, but Verify is also disabled.
U	P	Reserved for Future Definition.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are:

(030H) = 89H indicates manufactured by Intel
(031H) = 60H indicates 87C51GA

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537Å) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

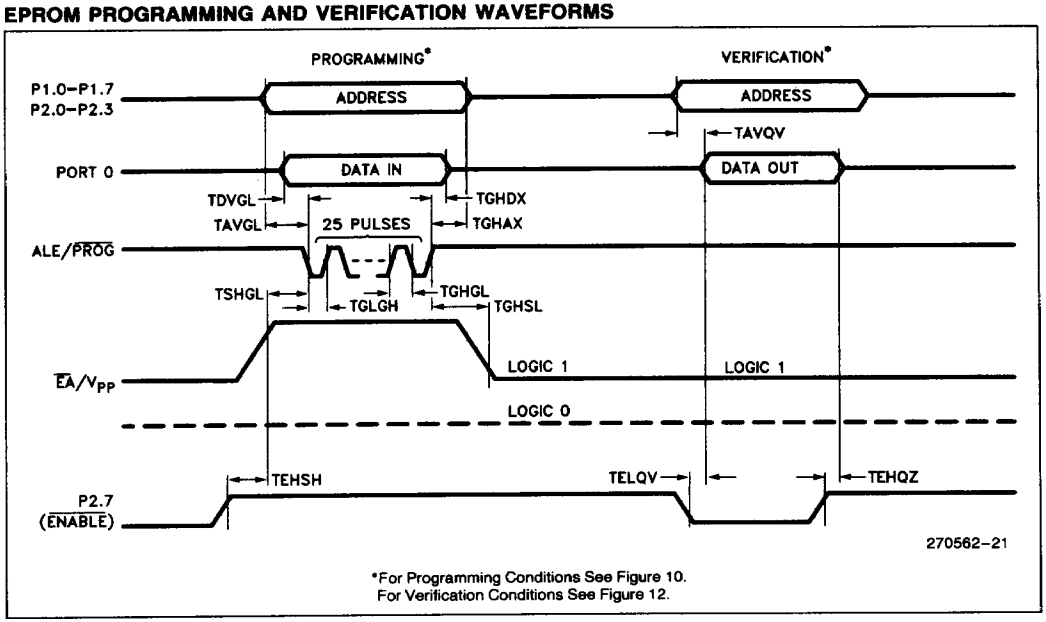
Erasure leaves the array in an all 1s state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_A = 21°C to 27°C, V_{CC} = 5V ±10% V_{SS} = 0V

Symbol	Parameter	Min	Max	Unit
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		50.0	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48 TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48 TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48 TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48 TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) HIGH to V_{PP}	48 TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	95	105	µs
TAVQV	Address to Data Valid		48 TCLCL	
TELQV	$\overline{ENABLE}$ Low to Data Valid		48 TCLCL	
TEHQZ	Data Float after $\overline{ENABLE}$	0	48 TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*For Programming Conditions See Figure 10.
For Verification Conditions See Figure 12.

A/D Glossary of Terms

Absolute Error—The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

Actual Characteristic—The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An actual characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversions under the same conditions.

Break-Before-Make—The property of a multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected (e.g. the converter will not short inputs together).

Channel-To-Channel Matching—The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

Characteristic—A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

Code—The digital value output by the converter.

Code Center—The voltage corresponding to the midpoint between two adjacent code transitions.

Code Transition—The point at which the converter changes from an output code of Q, to a code of Q + 1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

Code Width—The voltage corresponding to the difference between two adjacent code transitions.

Crosstalk—See "Off-Isolation."

D.C. Input Leakage—Leakage current to ground from an analog input pin.

Differential Non-Linearity—The difference between the ideal and actual code widths of the terminal based characteristic.

Feedthrough—Attenuation of a voltage applied on the selected channel of the A/D Converter after the sample window closes.

Full Scale Error—The difference between the expected and actual input voltage corresponding to the full scale code transition.

Ideal Characteristic—A characteristic with its first code transition at V_{IN} = 0.5 LSB, its last code transition at V_{IN} = (V_{REF} − 1.5 LSB) and all code widths equal to one LSB.

Input Resistance—The effective series resistance from the analog input pin to the sample capacitor.

LSB—Least Significant Bit: The voltage corresponding to the full scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For an 8-bit converter with a reference voltage of 5.12V, one LSB is 20 mV. Note that this is different than digital LSBs since an uncertainty of two LSBs, when referring to an A/D converter, equals 40 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 80 mV.)

Monotonic—The property of successive approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value.

No Missed Codes—For each and every output code, there exists a unique input voltage range which produces that code only.

Non-Linearity—The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristic.

Off-Isolation—Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

Repeatability—The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

Resolution—The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

Sample Delay—The delay from receiving the start conversion signal to when the sample window opens.

Sample Delay Uncertainty—The variation in the sample delay.

Sample Time—The time that the sample window is open.

Sample Time Uncertainty—The variation in the sample time.

Sample Window—Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

Successive Approximation—An A/D conversion method which uses a binary search to arrive at the best digital representation of an analog input.

Temperature Coefficients—Change in the stated variable per degree centigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effect of temperature drift.

Terminal Based Characteristic—An actual characteristic which has been rotated and translated to remove zero offset and full scale error.

V_{CC} Rejection—Attenuation of noise on the V_{CC} line to the A/D converter.

Zero Offset—The difference between the expected and actual input voltage corresponding to the first code transition.

DATA SHEET REVISION SUMMARY

The following are the key differences between this and the -001 version of the 87C51GA data sheet:

1. Reference to ROM and ROMless versions was reworded.
2. Packages Table was added.
3. Second paragraph to Power Down Mode description was added.
4. A/D nominal conversion speed changed from 27 μs to 22 μs at 12 MHz.
5. Figure 5 for Ports 1 and 3 hysteresis added.
6. Note 2 for DC Characteristics pertaining to the V_{OH1} specification on ALE and $\overline{PSEN}$ was changed.
7. Note 4 on maximum current specifications added to DC Characteristics.
8. The graph for I_{CC} specs was extended on Figure 6 from 12 MHz to 16 MHz and from 3.5 MHz to 0.5 MHz.
9. The following AC Timing specifications were changed:
   TLLAX changed from TCLCL−35 to TCLCL−30.
   TLLPL changed from TCLCL−40 to TCLCL−30.
   TRHDZ changed from 2TCLCL−70 to 2TCLCL−60.
   TQVWX changed from TCLCL−60 to TCLCL−50.
   TQVWH was added.
10. F_{OSC} specifications for Sample and Hold were deleted on A/D Characteristics.
11. Program Memory Lock scheme description was added.
12. Data Sheet Revision Summary added.