

4-TO-16 LINE DECODER/DEMULTIPLEXER

FEATURES

- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- 2-input enable gate for strobing or expansion
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT154 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually exclusive active LOW outputs.

The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for the expansion of the decoder.

The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The "154" can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable is LOW, the addressed output will follow the state of the applied data.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay A _n , E _n to Y _n	C _L = 15 pF V _{CC} = 5 V	11	13	ns
C _I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	60	60	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF
f_o = output frequency in MHz V_{CC} = supply voltage in V

Σ (C_L × V_{CC}² × f_o) = sum of outputs

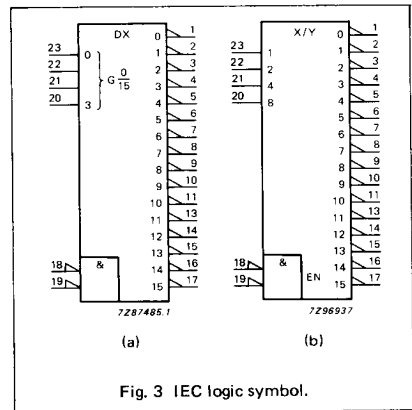
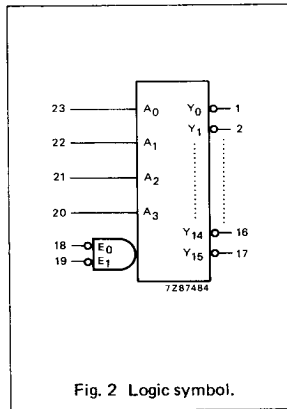
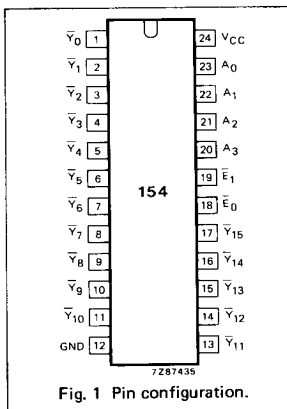
2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).
24-lead mini-pack; plastic (SO24; SOT137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	Y ₀ to Y ₁₅	outputs (active LOW)
18, 19	E ₀ , E ₁	enable inputs (active LOW)
12	GND	ground (0 V)
23, 22, 21, 20	A ₀ to A ₃	address inputs
24	V _{CC}	positive supply voltage



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay A _n to \bar{Y}_n		36 13 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t _{PHL} / t _{PLH}	propagation delay E _n to \bar{Y}_n		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	1.0
E _n	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay A _n to Y _n		16	35		44		53	ns	4.5	Fig. 6
t _{PHL} / t _{PLH}	propagation delay E _n to Y _n		15	32		40		48	ns	4.5	Fig. 7
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

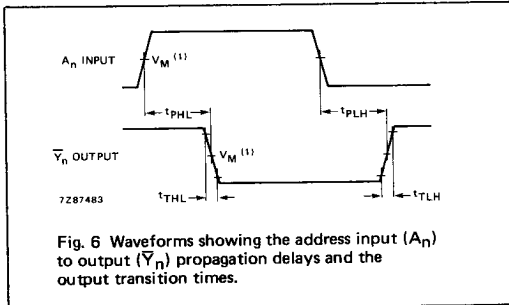


Fig. 6 Waveforms showing the address input (A_n) to output (\bar{Y}_n) propagation delays and the output transition times.

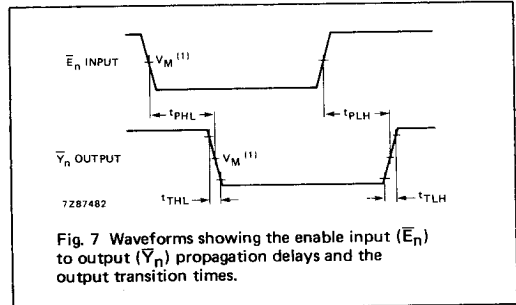


Fig. 7 Waveforms showing the enable input (\bar{E}_n) to output (\bar{Y}_n) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
- HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

APPLICATION INFORMATION

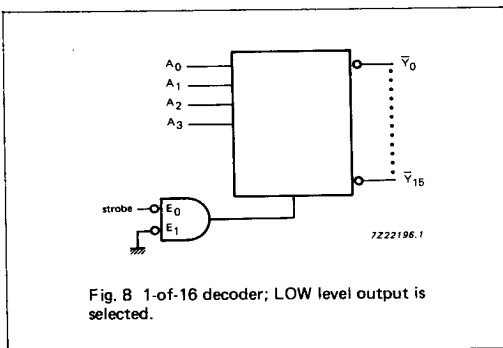


Fig. 8 1-of-16 decoder; LOW level output is selected.

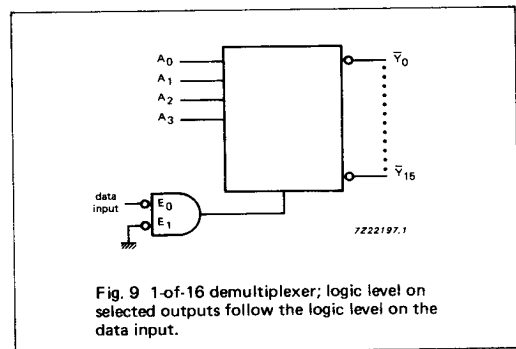


Fig. 9 1-of-16 demultiplexer; logic level on selected outputs follow the logic level on the data input.