FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12534-3E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89620R Series

MB89623R/625R/P625/W625/626R/627R/P627/W627/T627R
MB89PV620

■ DESCRIPTION

The MB89620R series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to the F²MC-8L CPU core which can operate at low voltage but at high speed, the microcontrollers contain a variety of peripheral functions such as timers, serial interfaces, an A/D converter, and an external interrupt.

The MB89620R series is applicable to a wide range of applications from consumer products to industrial equipment, including portable devices.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Various package options
  Three types of QFP packages (1 mm, 0.65 mm, or 0.5 mm lead pitch)
  SDIP packages
- High-speed processing at low voltage
  Minimum execution time: 0.4 µs/3.5 V, 0.8 µs/2.7 V
- F²MC-8L family CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.
- Four types of timers
  8-bit PWM timer (also usable as a reload timer)
  8-bit pulse width count timer (Continuous measurement capable, applicable to remote control, etc.)
  16-bit timer/counter
  20-bit timebase timer
- Two serial interfaces
  Switchable transfer direction allows communication with various equipment.
- 8-bit A/D converter
  Sense mode function enabling comparison at 5 µs
  Activation by an external input capable

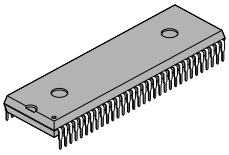
(Continued)

(Continued)

- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current cunsumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
- Bus interface functions
  Including hold and ready functions

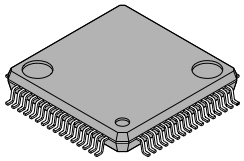
■ PACKAGE

64-pin Plastic SH-DIP



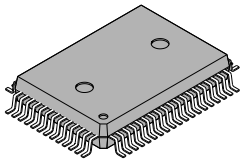
(DIP-64P-M01)

64-pin Plastic LQFP



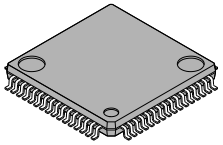
(FPT-64P-M03)

64-pin Plastic QFP



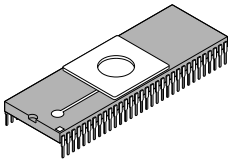
(FPT-64P-M06)

64-pin Plastic QFP



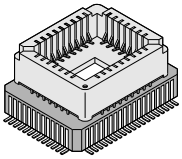
(FPT-64P-M09)

64-pin Ceramic SH-DIP



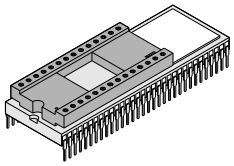
(DIP-64C-A06)

64-pin Ceramic MQFP



(MQP-64C-P01)

64-pin Ceramic MDIP



(MDP-64C-P02)

■ PRODUCT LINEUP

Part number / Parameter	MB89623R	MB89625R	MB89626R	MB89627R	MB89T627R	MB89P625 MB89W625	MB89P627 MB89W627	MB89PV620
Classification	Mass production products (mask ROM products)				External ROM products	One-time PROM products/EPROM products		Piggyback/ evaluation product for evaluation and development
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	External ROM	16 K × 8 bits (internal PROM, programmable with general-purpose EPROM programmer)	32 K × 8 bits (internal PROM, programmable with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	256 × 8 bits	512 × 8 bits	768 × 8 bits	1 K × 8 bits	1 K × 8 bits	512 × 8 bits	1 K × 8 bits	1 K × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 µs /10 MHz Interrupt processing time: 3.6 µs/10 MHz							
Ports	Input ports: 5 (4 ports also serve as peripherals.) Output ports (N-ch open-drain): 8 (All also serve as peripherals.) I/O ports (N-ch open-drain) 8 (4 ports also serve as peripherals.) Output ports (CMOS): 8 (All also serve as bus control pins.) I/O ports (CMOS): 24 (All also serve as bus pins or peripherals.) Total: 53							
8-bit PWM timer	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 µs to 3.3 ms) 8-bit resolution PWM operation (conversion cycle: 102 µs to 839 ms)							
8-bit pulse width count timer	8-bit timer operation (overflow output capable, operating clock cycle: 0.4 to 12.8 µs) 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 to 12.8 µs) 8-bit pulse width measurement operation (Continuous measurement “H” pulse width/“L” pulse width/from ↑ to ↑/from ↓ to ↓ capable)							
16-bit timer/ counter	16-bit timer operation (operating clock cycle: 0.4 µs) 16-bit event counter operation (Rising/falling/both edges selectable)							
8-bit serial I/O 1, 8-bit serial I/O 2	8 bits LSB first/MSB first selectable One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 µs, 3.2 µs, 12.8 µs)							
8-bit A/D converter	8-bit resolution × 8 channels A/D conversion mode (conversion time: 18 µs) Sense mode (conversion time: 5 µs) Continuous activation by an external activation or an internal timer capable Reference voltage input							

(Continued)

(Continued)

Parameter \ Part number	MB89623R	MB89625R	MB89626R	MB89627R	MB89T627R	MB89P625 MB89W625	MB89P627 MB89W627	MB89PV620
External interrupt	4 independent channels (edge selection, interrupt vector, source flag) Rising edge/falling edge selectable Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)							
Standby modes	Sleep mode, stop mode							
Process	CMOS							
Operating voltage*	2.2 V to 6.0 V				2.7 V to 6.0 V			
EPROM for use								MBM27C256A-20TV MBM27C256A-20CZ

*: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89623R MB89625R	MB89626R MB89627R MB89T627R MB89P625	MB89P627	MB89W625 MB89W627	MB89PV620
DIP-64P-M01	○	○	○	×	×
FPT-64P-M03	○	×*	×*	×*	×*
FPT-64P-M06	○	○	○	×	×
FPT-64P-M09	○	○	×*	×*	×*
DIP-64C-A06	×	×	×	○	×
MQP-64C-P01	×	×	×	×	○
MDP-64C-P02	×	×	×	×	○

○: Available ×: Not available

*: Lead pitch converter sockets (manufacturer: Sun Hayato Co., Ltd.) are available.
64SD-64QF2-8L: For conversion from DIP-64P-M01 or DIP-64C-A06 to FPT-64P-M03
64SD-64SQF-8L: For conversion from DIP-64P-M01 or DIP-64C-A06 to FPT-64P-M09
Inquiry: Sun Hayato Co., Ltd. : TEL (81)-3-3986-0403
FAX (81)-3-5396-9106

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89623R, the upper half of the register bank cannot be used.
- On the MB89P627, the program area starts from address 8007_H but on the MB89PV620 and MB89627R starts from 8000_H.

  (On the MB89P627, addresses 8000_H to 8006_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV620 and MB89627R, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P627.)
- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

2. Current Consumption

- In the case of the MB89PV620, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see section "■ Electrical Characteristics".)

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

Take particular care on the following points:

- A pull-up resistor cannot be set for P40 to P47 on the MB89P625, MB89W625, MB89P627, and MB89W627.
- A pull-up resistor is not selectable for P50 to P57 when the A/D converter is used.
- Options are fixed on the MB89PV620.

4. Differences between the MB89620 and MB89620R Series

- Memory access area

Memory access area of the following products is the same; both the MB89625 and MB89625R, and both the MB89627 and MB89627R.

The access area of the MB89623 and MB89626 is different from that of the MB89623R and MB89626R respectively when using in external bus mode. See below.

Address	Memory area	
	MB89623	MB89623R
0000_H to $007F_H$	I/O area	I/O area
0080_H to $017F_H$	RAM area	RAM area
0180_H to $027F_H$	External area	Access prohibited
0280_H to $BFFF_H$		External area
$C000_H$ to $DFFF_H$		Access prohibited
$E000_H$ to $FFFF_H$	ROM area	ROM area

Address	Memory area	
	MB89626	MB89626R
0000_H to $007F_H$	I/O area	I/O area
0080_H to $037F_H$	RAM area	RAM area
0380_H to $047F_H$	External area	Access prohibited
0480_H to $7FFF_H$		External area
8000_H to $9FFF_H$		Access prohibited
$A000_H$ to $FFFF_H$	ROM area	ROM area

- Other specifications
  Both the MB89620R and MB89620 series is the same.
- Electrical specifications/electrical characteristics
  Electrical specifications of the MB89620R series are the same with that of the MB89620 series.

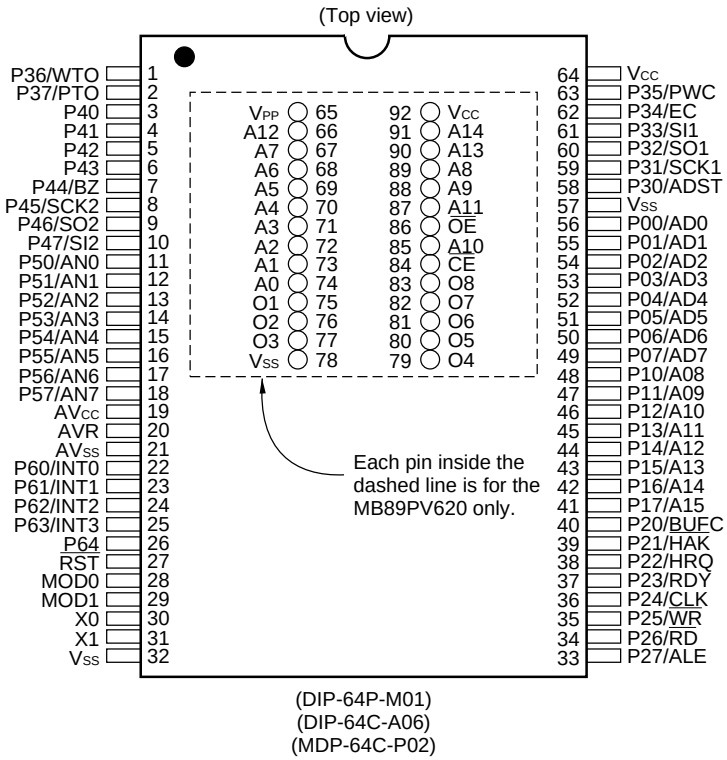
■ CORRESPONDENCE BETWEEN THE MB89620 AND MB89620R SERIES

- The MB89620R series is the reduction version of the MB89620 series.
- The MB89620 and MB89620R series consist of the following products:

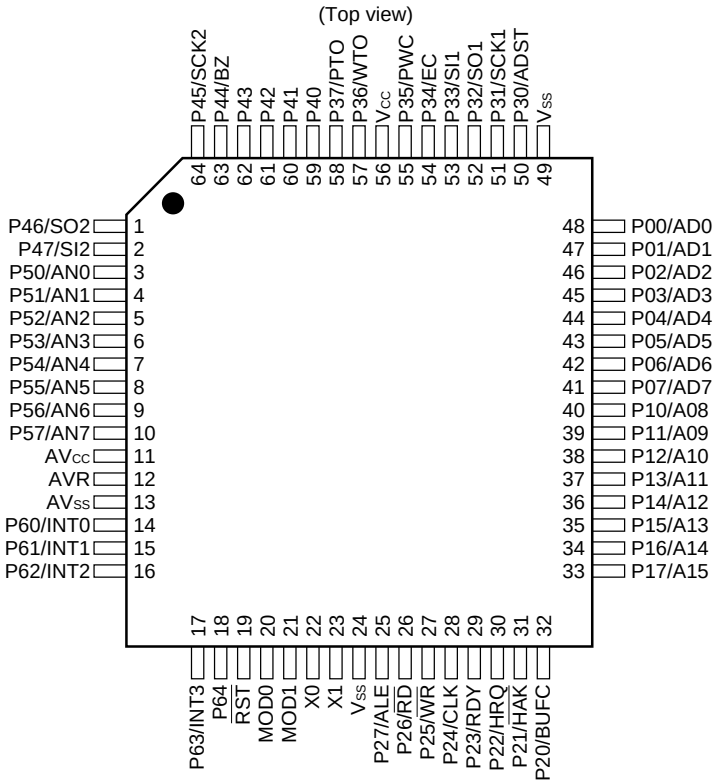
MB89620 series	MB89623	MB89625	MB89626	MB896267	MB89P625	MB89P627	MB89PV620
MB89620R series	MB89623R	MB89625R	MB89626R	MB896267R			

MB89620 series	MB89W625	MB89W627	MB89T627R
MB89620R series			

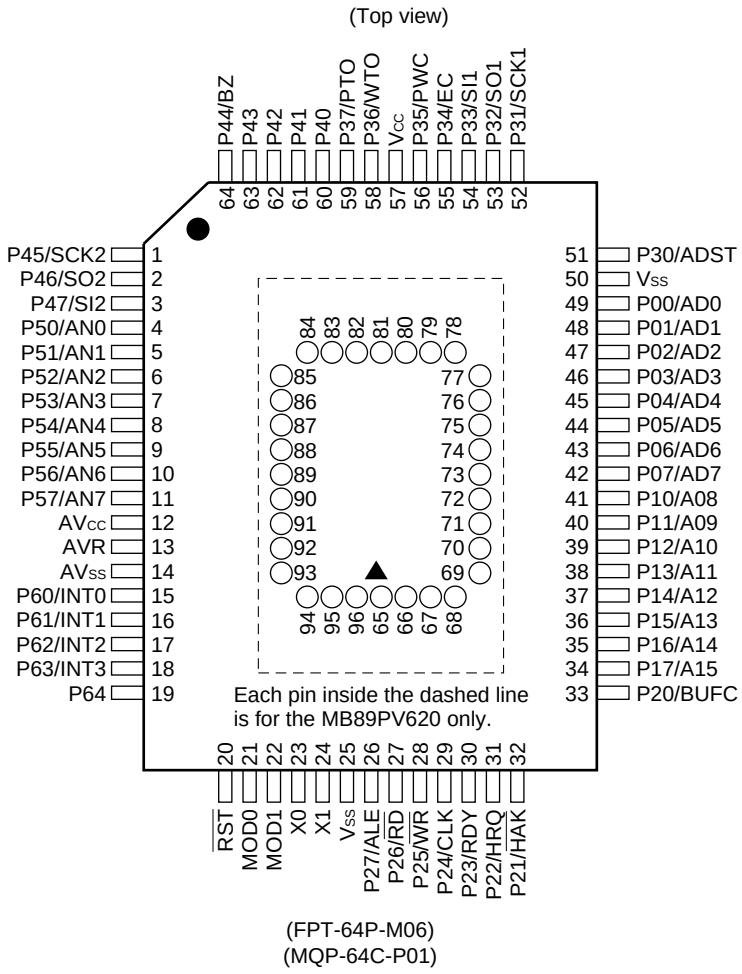
■ PIN ASSIGNMENT



(DIP-64P-M01)
(DIP-64C-A06)
(MDP-64C-P02)



(FPT-64P-M03)
(FPT-64P-M09)



(FPT-64P-M06)
(MQP-64C-P01)

- **Pin assignment on package top (MB89PV620 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	V_{PP}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP1*3 MQFP*4	LQFP*5 QFP2*6			
30	23	22	X0	A	Crystal oscillator pins
31	24	23	X1		
28	21	20	MOD0	B	Operating mode selection pins Connect directly to V_{CC} or V_{SS}.
29	22	21	MOD1		
27	20	19	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".
56 to 49	49 to 42	48 to 41	P00/AD0 to P07/AD7	D	General-purpose I/O ports When an external bus is used, these ports function as multiplex pins of lower address output and data I/O.
48 to 41	41 to 34	40 to 33	P10/A08 to P17/A15	D	General-purpose I/O ports When an external bus is used, these ports function as upper address output.
40	33	32	P20/BUFC	F	General-purpose output-only port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.
39	32	31	P21/$\overline{HAK}$	F	General-purpose output-only port When an external bus is used, this port can also be used as a hold acknowledge output by setting the BCTR.
38	31	30	P22/HRQ	D	General-purpose output-only port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.
37	30	29	P23/RDY	D	General-purpose output-only port When an external bus is used, this port functions as a ready input.
36	29	28	P24/CLK	F	General-purpose output-only port When an external bus is used, this port functions as a clock output.
35	28	27	P25/$\overline{WR}$	F	General-purpose output-only port When an external bus is used, this port functions as a write signal output.
34	27	26	P26/$\overline{RD}$	F	General-purpose output-only port When an external bus is used, this port functions as a read signal output.
33	26	25	P27/ALE	F	General-purpose output-only port When an external bus is used, this port functions as an address latch signal output.

(Continued)

*1: DIP-64P-M01, DIP-64C-A06 *2: MDP-64C-P02 *3: FPT-64P-M06
*4: MQP-64C-P01 *5: FPT-64P-M03 *6: FPT-64P-M09

(Continued)

Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP1*3 MQFP*4	LQFP*5 QFP2*6			
58	51	50	P30/ADST	E	General-purpose I/O port Also serves as an A/D converter external activation. This port is a hysteresis input type.
59	52	51	P31/SCK1	E	General-purpose I/O port Also serves as the clock I/O for the 8-bit serial I/O 1. This port is a hysteresis input type.
60	53	52	P32/SO1	E	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O 1. This port is a hysteresis input type.
61	54	53	P33/SI1	E	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O 1. This port is a hysteresis input type.
62	55	54	P34/EC	E	General-purpose I/O port Also serves as the external clock input for the 16-bit timer/counter. This port is a hysteresis input type.
63	56	55	P35/PWC	E	General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width count timer. This port is a hysteresis input type.
1	58	57	P36/WTO	E	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width count timer. This port is a hysteresis input type.
2	59	58	P37/PTO	E	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer. This port is a hysteresis input type.
3 to 6	60 to 63	59 to 62	P40 to P43	G	N-ch open-drain I/O ports These ports are a hysteresis input type.
7	64	63	P44/BZ	G	N-ch open-drain I/O port Also serves as a buzzer output. This port is a hysteresis input type.
8	1	64	P45/SCK2	G	N-ch open-drain I/O port Also serves as the clock I/O for the 8-bit serial I/O 2. This port is a hysteresis input type.
9	2	1	P46/SO2	G	N-ch open-drain I/O port Also serves as the data output for the 8-bit serial I/O 2. This port is a hysteresis input type.
10	3	2	P47/SI2	G	N-ch open-drain I/O port Also serves as the data input for the 8-bit serial I/O 2. This port is a hysteresis input type.

(Continued)

*1: DIP-64P-M01, DIP-64C-A06 *2: MDP-64C-P02 *3: FPT-64P-M06
*4: MQP-64C-P01 *5: FPT-64P-M03 *6: FPT-64P-M09

(Continued)

Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP1*3 MQFP*4	LQFP*5 QFP2*6			
11 to 18	4 to 11	3 to 10	P50/AN0 to P57/AN7	H	N-ch open-drain output-only ports Also serve as the analog input for the A/D converter.
22 to 25	15 to 18	14 to 17	P60/INT0 to P63/INT3	I	General-purpose input-only ports Also serve as an external interrupt input. These ports are a hysteresis input type.
26	19	18	P64	I	General-purpose input-only port This port is a hysteresis input type.
64	57	56	V_{CC}	—	Power supply pin
32, 57	25, 50	24, 49	V_{SS}	—	Power supply (GND) pins
19	12	11	AV_{CC}	—	A/D converter power supply pin
20	13	12	AVR	—	A/D converter reference voltage input pin
21	14	13	AV_{SS}	—	A/D converter power supply (GND) pin Use this pin at the same voltage as V_{SS}.

*1: DIP-64P-M01, DIP-64C-A06 *2: MDP-64C-P02 *3: FPT-64P-M06

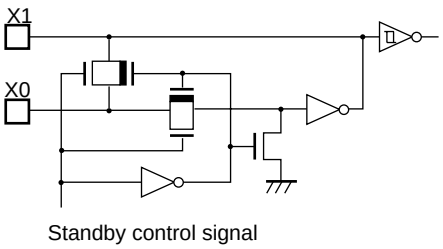
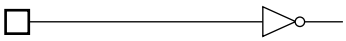
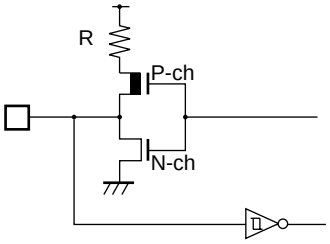
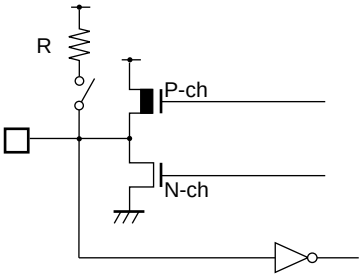
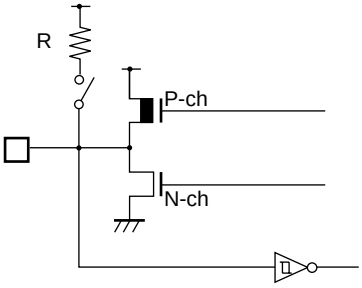
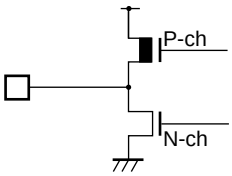
*4: MQP-64C-P01 *5: FPT-64P-M03 *6: FPT-64P-M09

- **External EPROM pins (MB89PV620 only)**

Pin no.		Pin name	I/O	Function
MDIP*1	MQFP*2			
65	66	V_{PP}	O	“H” level output pin
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
75 76 77	77 78 79	O1 O2 O3	I	Data input pins
78	80	V_{SS}	O	Power supply (GND) pin
79 80 81 82 83	82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins
84	87	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
85	88	A10	O	Address output pin
86	89	$\overline{OE}$	O	ROM output enable pin Outputs “L” at all times.
87 88 89	91 92 93	A11 A9 A8	O	Address output pins
90	94	A13	O	
91	95	A14	O	
92	96	V_{CC}	O	EPROM power supply pin
—	65 76 81 90	N.C.	—	Internally connected pins Be sure to leave them open.

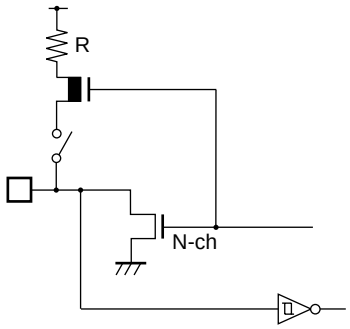
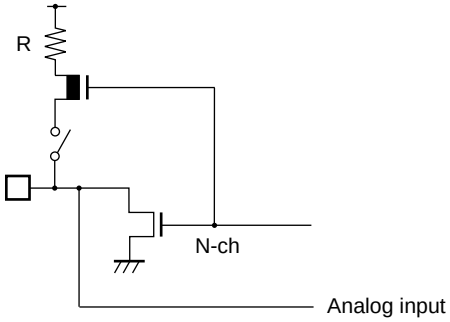
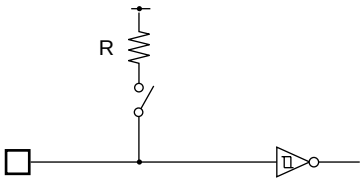
*1: MDP-64C-P02
*2: MQP-64C-P01

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D		• CMOS output • CMOS input • Pull-up resistor optional (except P22 and P23)
E		• CMOS output • Hysteresis input • Pull-up resistor optional
F		• CMOS output

(Continued)

(Continued)

Type	Circuit	Remarks
G		• N-ch open-drain output • Hysteresis input • Pull-up resistor optional (MB89623R, MB89625R, MB89626R, and MB89627R only)
H		• N-ch open-drain output • Analog input • Pull-up resistor optional
I		• Hysteresis input • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P625

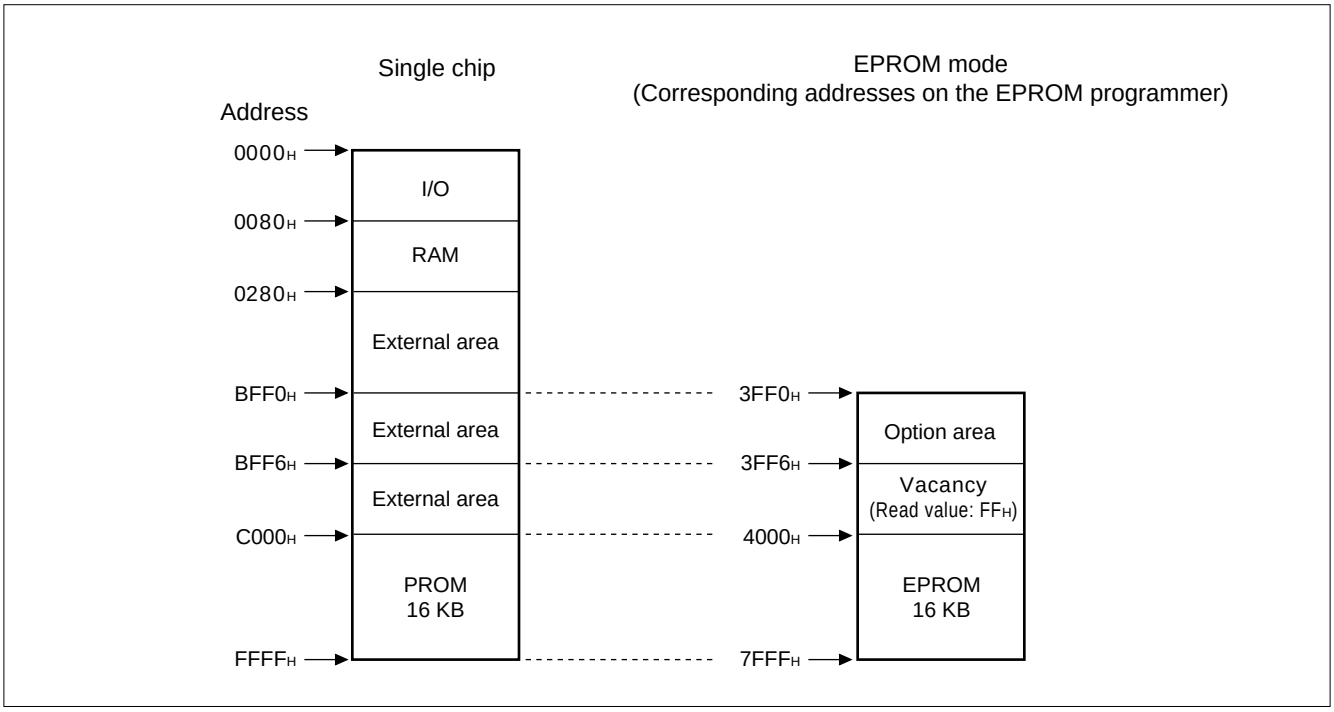
The MB89P625 is an OTPROM version of the MB89620R series.

1. Features

- 16-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 16-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P625 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

When the operating ROM area for a single chip is 16 Kbytes (C000H to FFFFH) the PROM can be programmed as follows:

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000H to 7FFFH (note that addresses C000H to FFFFH while operating as a single chip assign to 4000H to 7FFFH in EPROM mode).
Load option data into addresses 3FF0H to 3FF5H of the EPROM programmer. (For information about each corresponding option, see “4. Setting OTPROM Options.”)

(3) Program to 3FF0H to 7FFFH with the EPROM programmer.

4. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map.

The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map (MB89P625)**

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Reset pin output 1: Yes 0: No	Oscillation stabilization time 1: Crystal 0: Ceramic	Power-on reset 1: Yes 0: No
3FF1H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
3FF2H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
3FF3H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
3FF4H	P57 Pull-up 1: No 0: Yes	P56 Pull-up 1: No 0: Yes	P55 Pull-up 1: No 0: Yes	P54 Pull-up 1: No 0: Yes	P53 Pull-up 1: No 0: Yes	P52 Pull-up 1: No 0: Yes	P51 Pull-up 1: No 0: Yes	P50 Pull-up 1: No 0: Yes
3FF5H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes

Note: Each bit is set to ‘1’ as the initialized value, therefore the pull-up option is not selected.

■ PROGRAMMING TO THE EPROM ON THE MB89P627

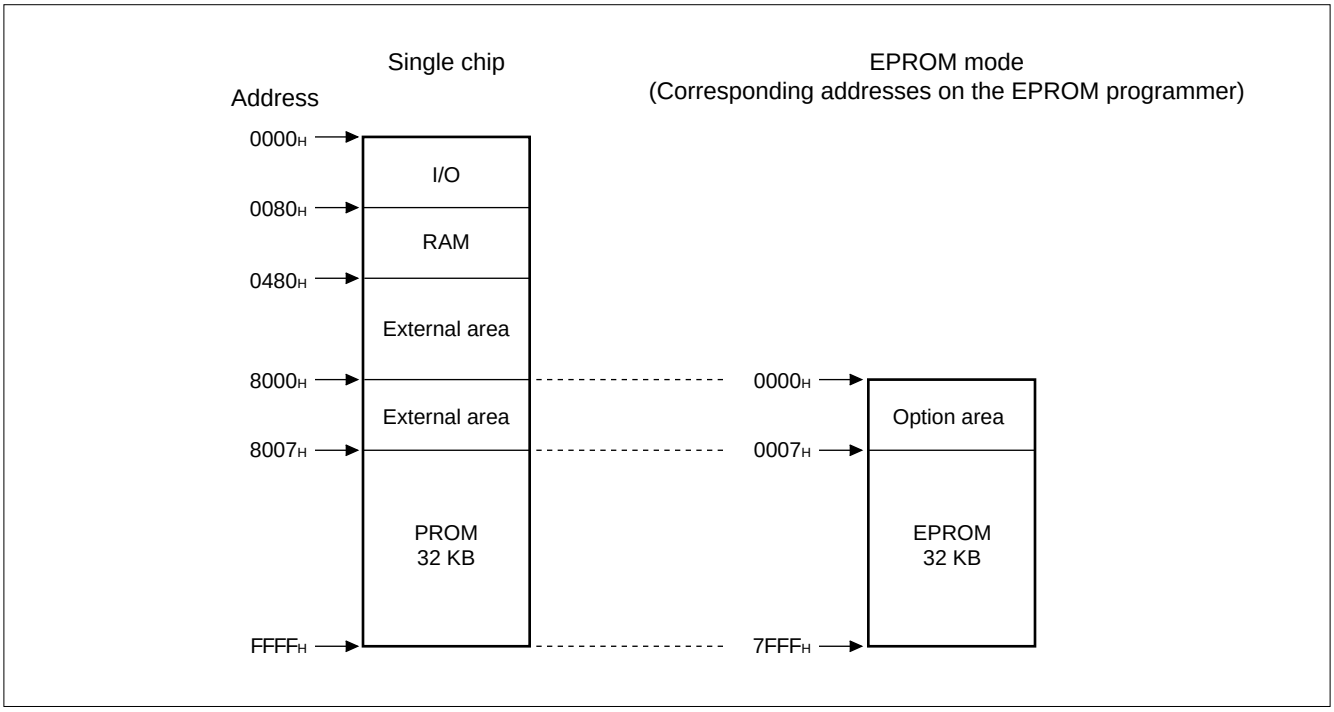
The MB89P627 is an OTPROM version of the MB89620R series.

1. Features

- 32-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 32-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P627 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

When the operating ROM area for a single chip is 32 Kbytes (8007_H to $FFFF_H$) the PROM can be programmed as follows:

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$ (note that addresses 8007_H to $FFFF_H$ while operating as a single chip assign to 0007_H to $7FFF_H$ in EPROM mode).
Load option data into addresses 0000_H to 0006_H of the EPROM programmer. (For information about each corresponding option, see “4. Setting OTPROM Options.”)

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

4. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map.

The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map (MB89P627)**

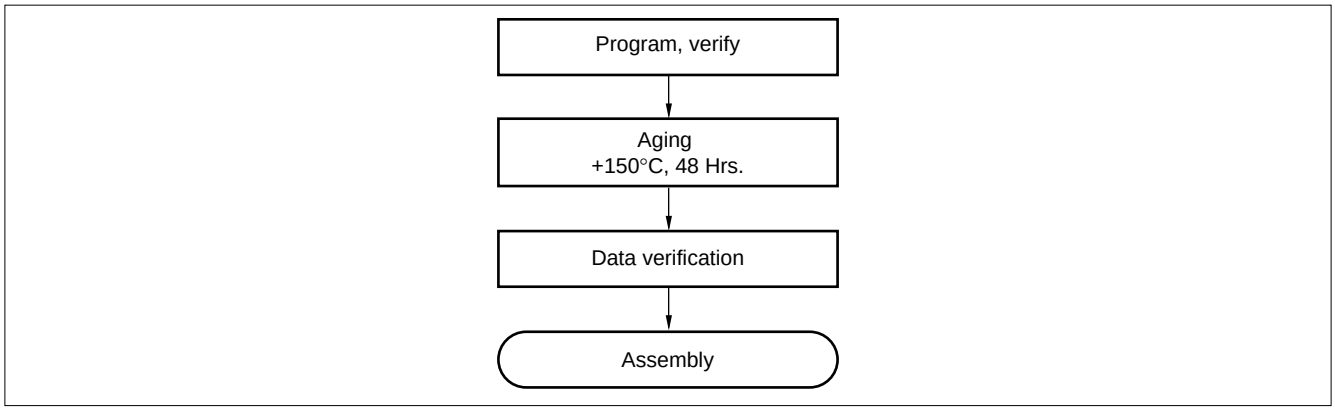
Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Reset pin output 1: Yes 0: No	Oscillation stabilizatio ntime 1: Crystal 0: Ceramic	Power-on reset 1: Yes 0: No
0001_H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
0002_H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0003_H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0004_H	P57 Pull-up 1: No 0: Yes	P56 Pull-up 1: No 0: Yes	P55 Pull-up 1: No 0: Yes	P54 Pull-up 1: No 0: Yes	P53 Pull-up 1: No 0: Yes	P52 Pull-up 1: No 0: Yes	P51 Pull-up 1: No 0: Yes	P50 Pull-up 1: No 0: Yes
0005_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
0006_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable

Note: Each bit is set to ‘1’ as the initialized value, therefore the pull-up option is not selected.

■ HANDLING THE MB89P625/P627

1. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



2. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

3. Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the internal EPROM to an ultraviolet light source. A dosage of 10 W-seconds/cm^2 is required to completely erase an internal EPROM. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000 μW/cm^2 for 15 to 21 minutes. The internal EPROM should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the internal EPROM and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the internal EPROM, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

4. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

Part number	Package	Compatible socket adapter Sun Hayato Co., Ltd.	Recommended programmer manufacturer and programmer name					
			Minato Electronics Inc.		Data I/O Co., Ltd.			Advantest Corp.
			1890A	1891	UNISITE	3900	2900	R4945A
MB89P625P-SH	SH-DIP-64	ROM-64SD-28DP-8L	Recommended		Recommended		—	Recommended
MB89P625PF	QFP-64	ROM-64QF-28DP-8L	Recommended*		Recommended			Recommended
MB89P625PFM	QFP-64	ROM-64QF2-28DP-8L	Recommended*		Recommended	—		Recommended

*: It is required to connect a capacitor of approximately 0.1 µF between V_{PP} and GND, and V_{CC} and GND.

Inquiry: Sun Hayato Co., Ltd. : TEL (81)-3-3986-0403
FAX (81)-3-5396-9106
Minato Electronics Inc.: TEL: USA (1)-916-348-6066
JAPAN (81)-45-591-5611
Data I/O Co., Ltd: TEL: USA/ASIA (1)-206-881-6444
EUROPE (49)-8-985-8580
Advantest Corp. :TEL: Except JAPAN (81)-3-3930-4111

■ PROGRAMMING TO THE EPROM PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV, MBM27C256A-20CZ

2. Programming Socket Adapter

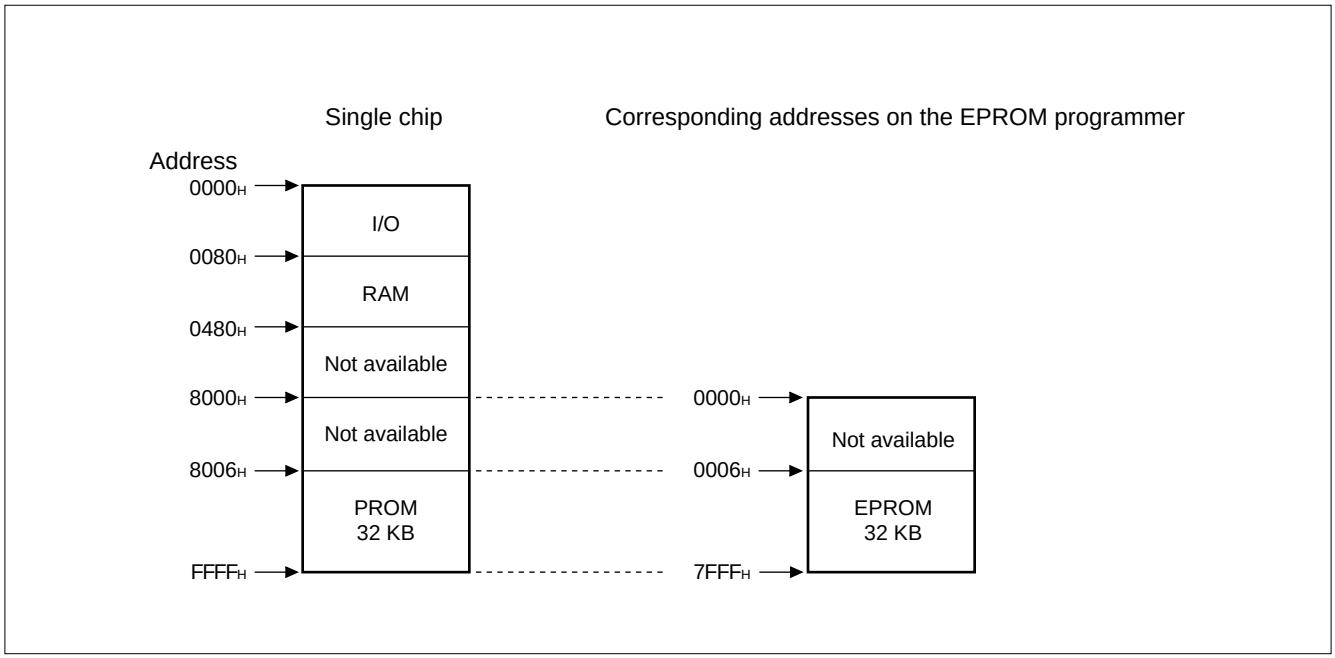
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL (81)-3-3986-0403
FAX (81)-3-5396-9106

3. Memory Space

Memory space in 32-Kbyte PROM is diagrammed below.



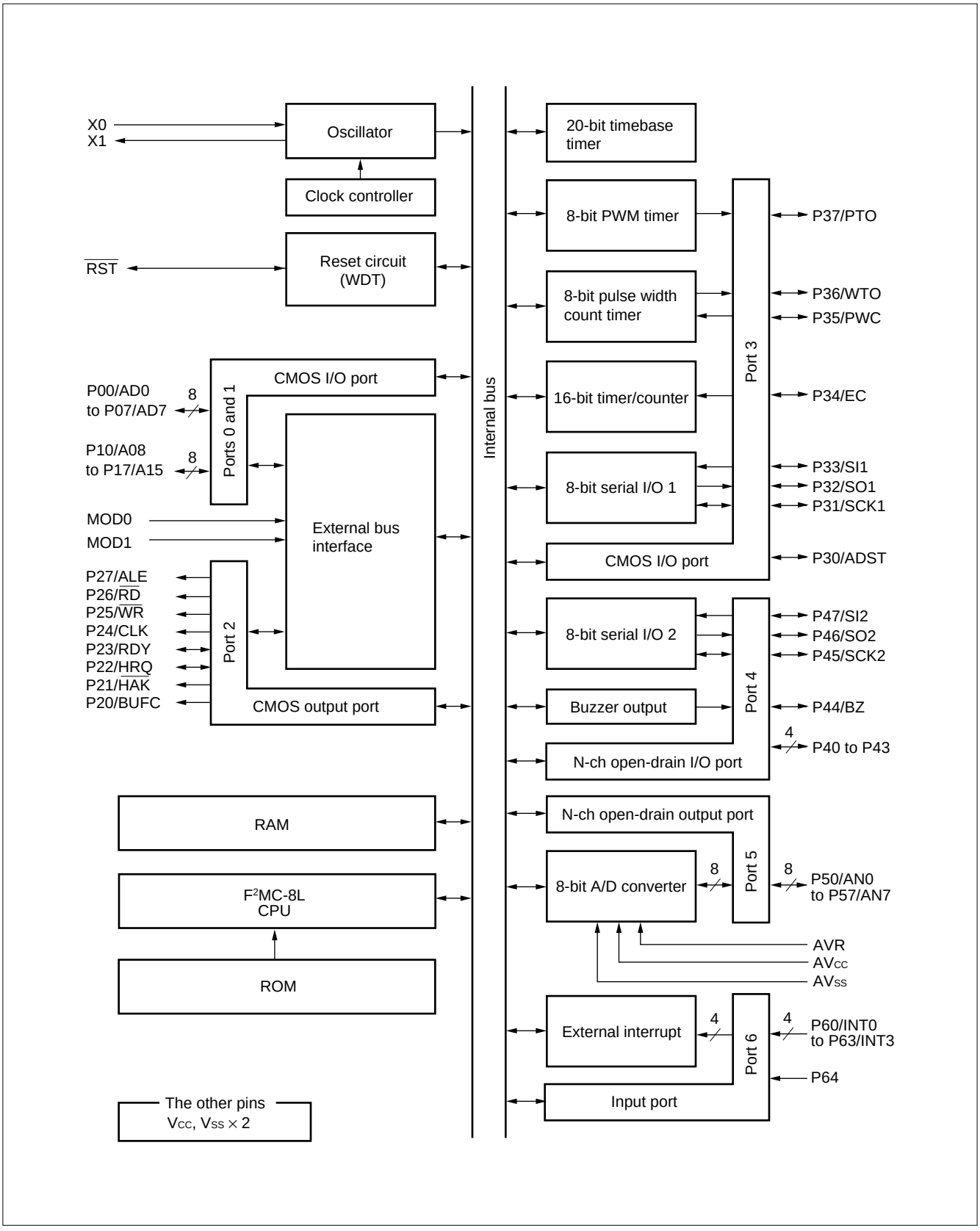
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0006_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

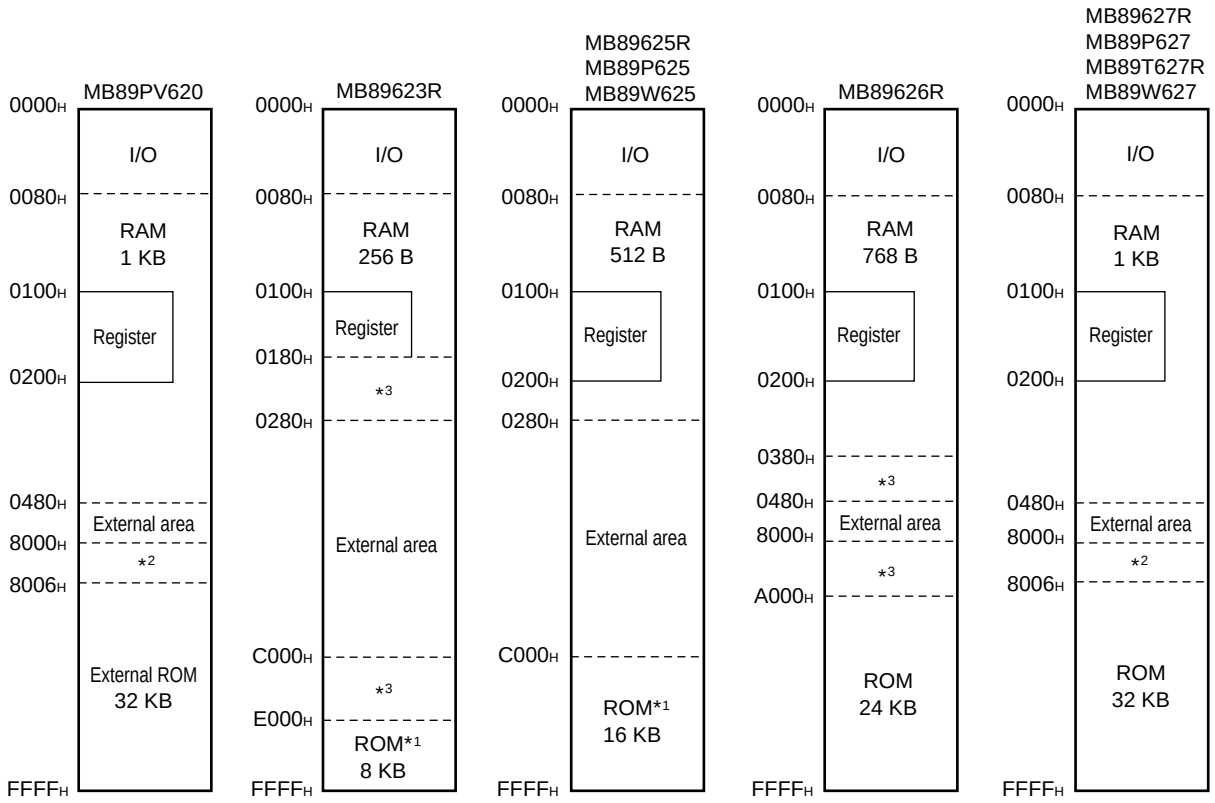


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89620R series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89620R series is structured as illustrated below.

- **Memory Space**



*1: The ROM area is an external area depending on the mode.

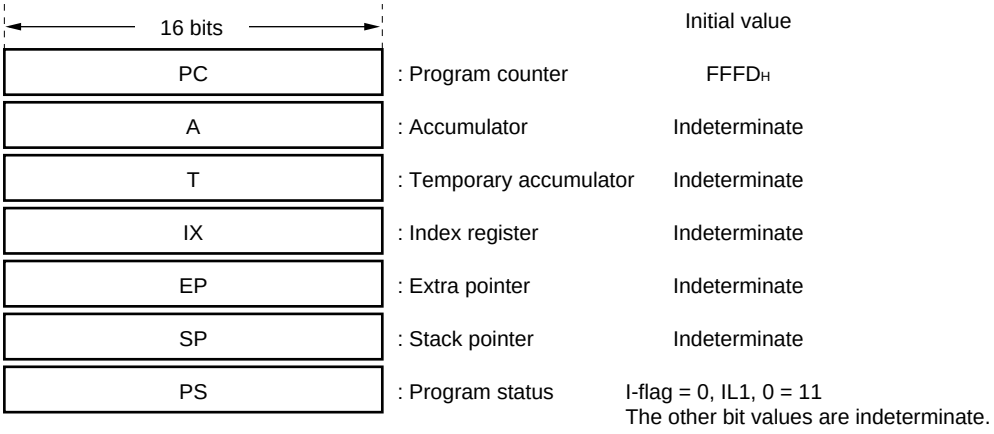
*2: Since addresses 8000H to 8005H for the MB89P627 and MB89W627 comprise an option area, do not use this area for the MB89PV620 and MB89627R.

*3: Access to this area is prohibited when using external bus mode.

2. Registers

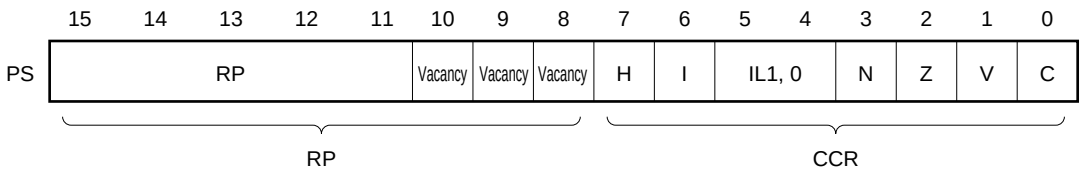
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



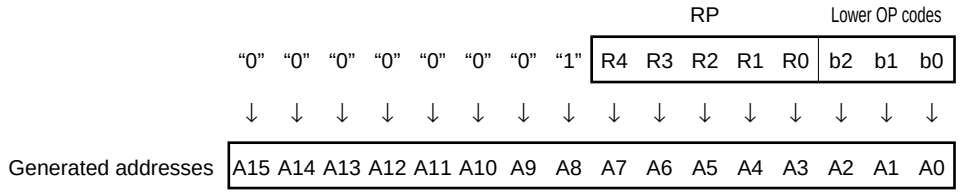
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

- **Structure of the Program Status Register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.
Set to the shift-out value in the case of a shift instruction.

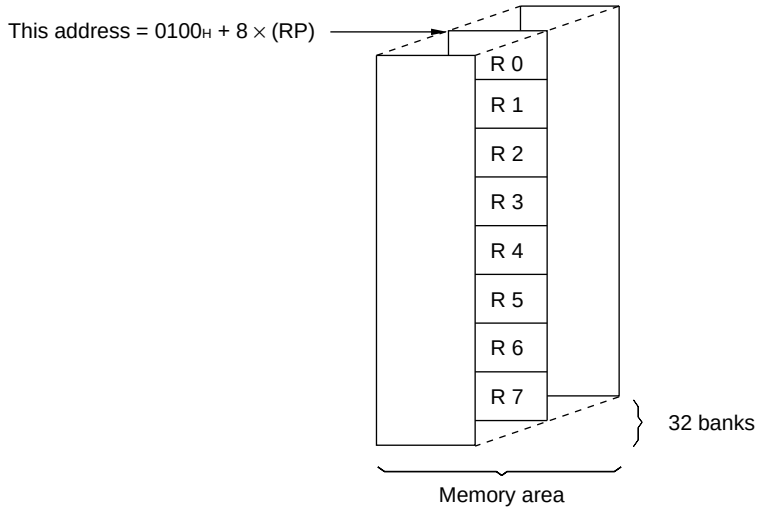
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89620R. In the MB89623R, there are 16 banks in internal RAM. The remaining 16 banks can be extended externally by allocating an external RAM to addresses 0180_H to $01FF_H$ using an external circuit. The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

- **Register Bank Configuration**



■ I/O MAP

Address	Read/write	Register name	Register description
00_H	(R/W)	PDR0	Port 0 data register
01_H	(W)	DDR0	Port 0 data direction register
02_H	(R/W)	PDR1	Port 1 data register
03_H	(W)	DDR1	Port 1 data direction register
04_H	(R/W)	PDR2	Port 2 data register
05_H	(R/W)	BCTR	External bus pin control register
06_H			Vacancy
07_H			Vacancy
08_H	(R/W)	STBC	Standby control register
09_H	(R/W)	WDTC	Watchdog timer control register
$0A_H$	(R/W)	TBTC	Timebase timer control register
$0B_H$			Vacancy
$0C_H$	(R/W)	PDR3	Port 3 data register
$0D_H$	(W)	DDR3	Port 3 data direction register
$0E_H$	(R/W)	PDR4	Port 4 data register
$0F_H$	(R/W)	BZCR	Buzzer register
10_H	(R/W)	PDR5	Port 5 data register
11_H	(R)	PDR6	Port 6 data register
12_H	(R/W)	CNTR	PWM control register
13_H	(W)	COMR	PWM compare register
14_H	(R/W)	PCR1	PWC pulse width control register 1
15_H	(R/W)	PCR2	PWC pulse width control register 2
16_H	(R/W)	RLBR	PWC reload buffer register
17_H			Vacancy
18_H	(R/W)	TMCR	16-bit timer control register
19_H	(R/W)	TCHR	16-bit timer count register (H)
$1A_H$	(R/W)	TCLR	16-bit timer count register (L)
$1B_H$			Vacancy
$1C_H$	(R/W)	SMR1	Serial I/O 1 mode register
$1D_H$	(R/W)	SDR1	Serial I/O 1 data register
$1E_H$	(R/W)	SMR2	Serial I/O 2 mode register
$1F_H$	(R/W)	SDR2	Serial I/O 2 data register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20_H	(R/W)	ADC1	A/D converter control register 1
21_H	(R/W)	ADC2	A/D converter control register 2
22_H	(R/W)	ADCD	A/D converter data register
23_H			Vacancy
24_H	(R/W)	EIC1	External interrupt 1 control register 1
25_H	(R/W)	EIC2	External interrupt 1 control register 2
26_H to $7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	*1
A/D converter reference input voltage	AVR	V_{SS} – 0.3	V_{SS} + 7.0	V	AVR must not exceed AV_{CC} + 0.3 V.
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P40 to P47*2
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P40 to P47
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P40 to P47*2
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P40 to P47
“L” level maximum output current	I_{OL}	—	20	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–20	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: Use AV_{CC} and V_{CC} set to the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

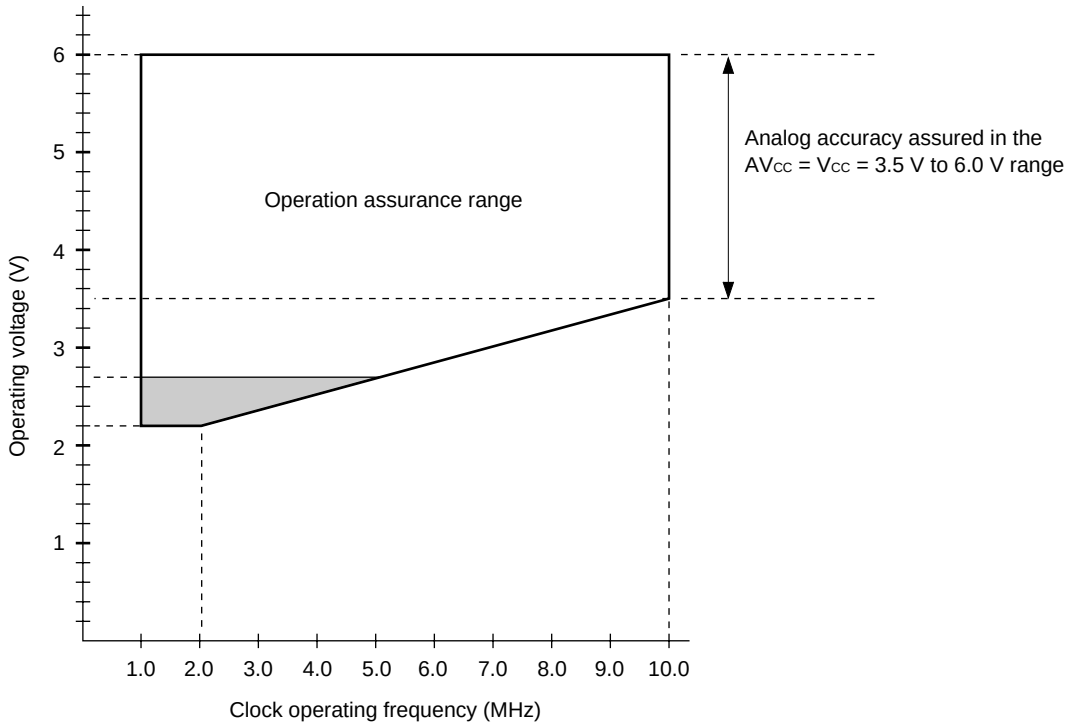
2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	2.2*	6.0*	V	Normal operation assurance range* (MB89623R/625R/626R/627R)
		2.7*	6.0*	V	Normal operation assurance range* (MB89P625/W625/P627/T627R/ W627/PV620)
		1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	0.0	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

*: These values vary with the operating frequency and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."

Figure 1 Operating Voltage vs. Clock Operating Frequency



Note: The shaded area is assured only for the MB89623R/625R/626R/627R.

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_C.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P22, P23	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, P30 to P37, P60 to P64	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS2}	P40 to P47	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P22, P23	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, P30 to P37, P40 to P47, P60 to P64	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P50 to P57	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
	V_{D2}	P40 to P47	—	V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57	I_{OL} = +4.0 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$		—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P64, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P64, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_{CC}	V_{CC}	F_C = 10 MHz Normal operating mode t_{inst}*2 = 0.4 µs	—	9	15	mA	MB89623R/ 625R/626R/ 627R/T627R/ PV620
				—	10	18	mA	MB89P625/ W625 MB89P627/ W627
	I_{CCS}		F_C = 10 MHz Sleep mode t_{inst}*2 = 0.4 µs	—	3	4	mA	
	I_{CCH}		Stop mode T_A = +25°C	—	—	1	µA	
	I_A	AV_{CC}	F_C = 10 MHz, when starting A/D conversion	—	1	3	mA	
	I_{AH}		F_C = 10 MHz, T_A = +25°C, when stopping A/D conversion	—	—	1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: In the case of the MB89PV620, the current consumed by the connected EPROM and ICE is not included. The power supply current is measured at the external clock.

*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

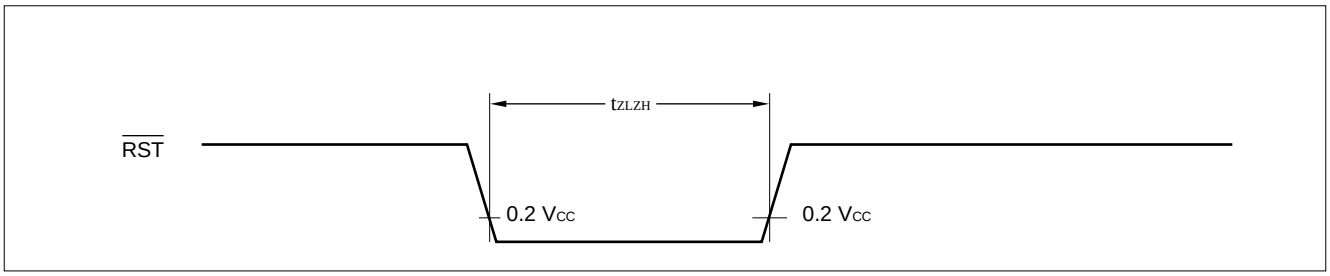
4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	16 t_{XCYL}	—	ns	

Note: t_{XCYL} is the oscillation cycle (1/F_C) to input to the X0 pin.

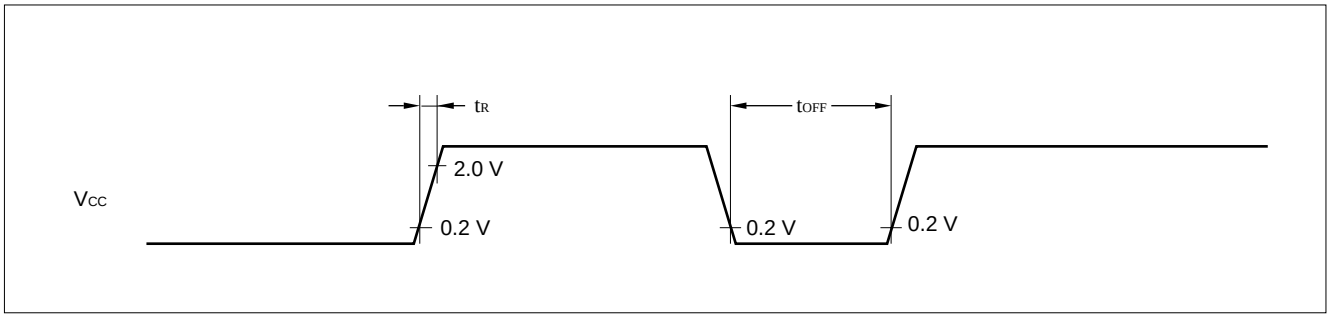


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

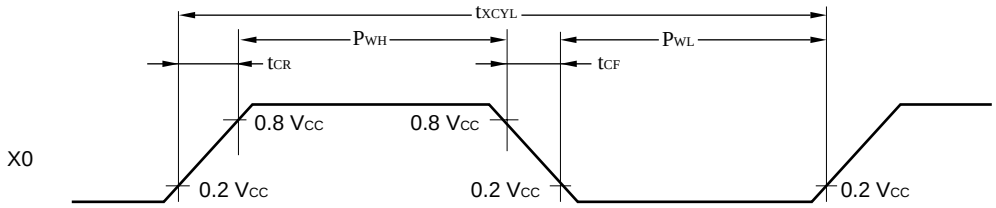


(3) Clock Timing

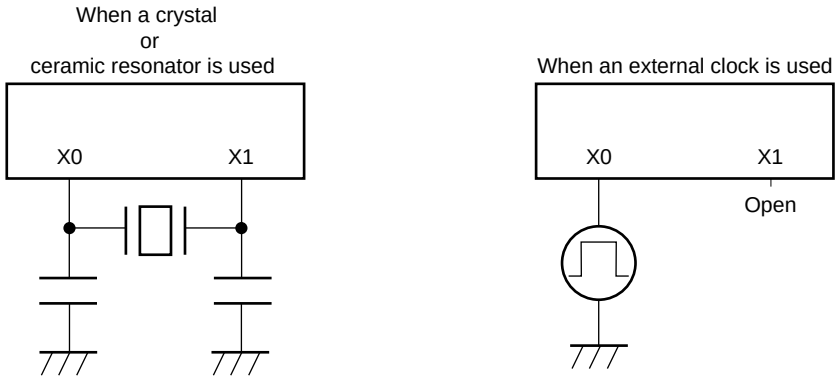
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	—	1	10	MHz	
Clock cycle time	t_{XYCL}	X0, X1		100	1000	ns	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0		—	10	ns	External clock

- **X0 and X1 Timing and Conditions**



- **Clock Conditions**



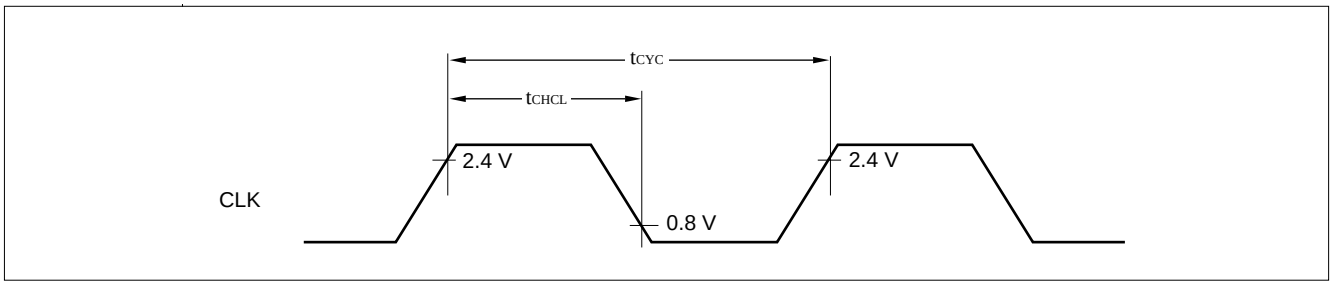
(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_C$	µs	t_{inst} = 0.4 µs when operating at F_C = 10 MHz

(5) Clock Output Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	200	—	ns	$t_{XCYL} \times 2$ at 10 MHz oscillation
CLK ↑ → CLK ↓	t_{CHCL}			30	100	ns	Approx. $t_{CYC}/2$ at 10 MHz oscillation

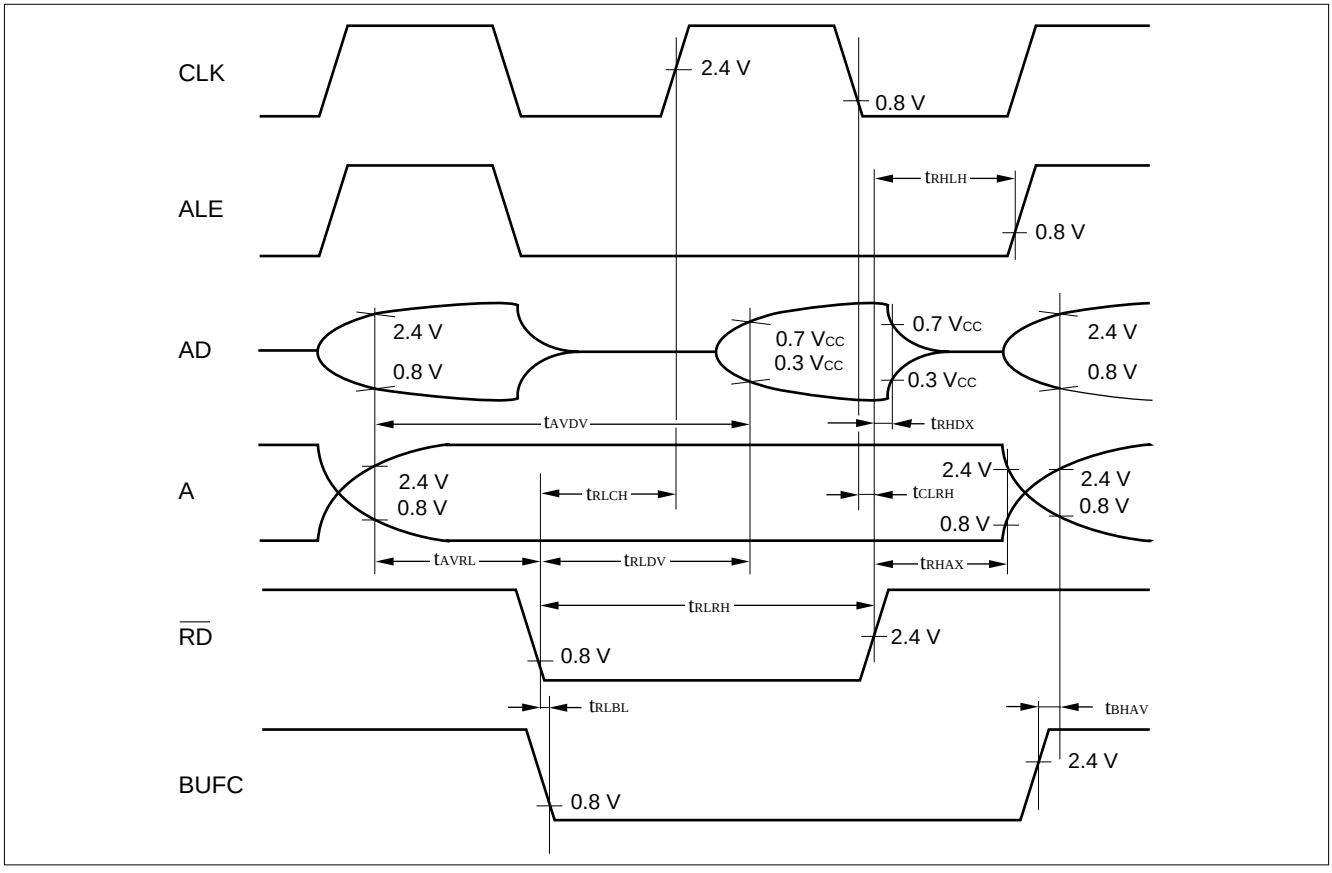


(6) Bus Read Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, A15 to A08, AD7 to AD0	—	1/4 t_{inst}* – 64 ns	—	µs	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		1/4 t_{inst}* – 20 ns	—	µs	
Valid address → data read time	t_{AVDV}	AD7 to AD0, A15 to A08		—	1/2 t_{inst}*	µs	In the case of no wait
$\overline{RD}$ ↓ → data read time	t_{RLDV}	$\overline{RD}$, AD7 to AD0		—	1/2 t_{inst}* – 80 ns	µs	In the case of no wait
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	AD7 to AD0, $\overline{RD}$		0	—	µs	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1/4 t_{inst}* – 40 ns	—	µs	
$\overline{RD}$ ↑ → address invalid time	t_{RHAX}	$\overline{RD}$, A15 to A08		1/4 t_{inst}* – 40 ns	—	µs	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1/4 t_{inst}* – 40 ns	—	µs	
CLK ↓ → $\overline{RD}$ ↑ time	t_{CLRH}			0	—	ns	
$\overline{RD}$ ↓ → BUFC ↓ time	t_{RLBL}	$\overline{RD}$, BUFC		–5	—	µs	
BUFC ↑ → valid address time	t_{BHAV}	A15 to A08, AD7 to AD0, BUFC		5	—	µs	

*: For information on t_{inst}, see “(4) Instruction Cycle.”



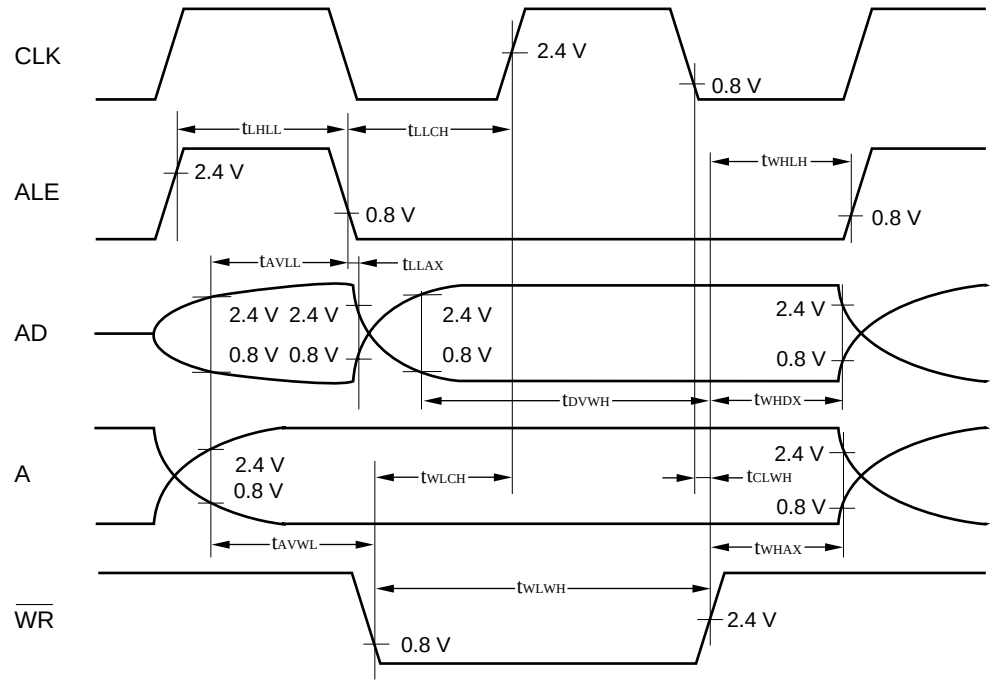
(7) Bus Write Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → ALE ↓ time	t_{AVLL}	AD7 to AD0, ALE, A15 to A08	—	1/4 t_{inst}*1 – 64 ns	—	µs	
ALE ↓ time → address invalid time	t_{LLAX}	AD7 to AD0, ALE, A15 to A08		5	—	ns	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 60 ns	—	µs	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		1/2 t_{inst}*1 – 20 ns	—	µs	
Write data → $\overline{WR}$ ↑ time	t_{DVWH}	AD7 to AD0, $\overline{WR}$		1/2 t_{inst}*1 – 60 ns	—	µs	
$\overline{WR}$ ↑ → address invalid time	t_{WHAX}	$\overline{WR}$, A15 to A08		1/4 t_{inst}*1 – 40 ns	—	ns	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	AD7 to AD0, $\overline{WR}$		1/4 t_{inst}*1 – 40 ns	—	µs	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 40 ns	—	µs	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		1/4 t_{inst}*1 – 40 ns	—	µs	
CLK ↓ → $\overline{WR}$ ↑ time	t_{CLWH}			0	—	ns	
ALE pulse width	t_{LHLL}	ALE		1/4 t_{inst}*1 – 35 ns*2	—	µs	
ALE ↓ → CLK ↑ time	t_{LLCH}	ALE,CLK		1/4 t_{inst}*1 – 30 ns*2	—	µs	

*1: For information on t_{inst}, see “(4) Instruction Cycle.”

*2: These characteristics are also applicable to the bus read timing.

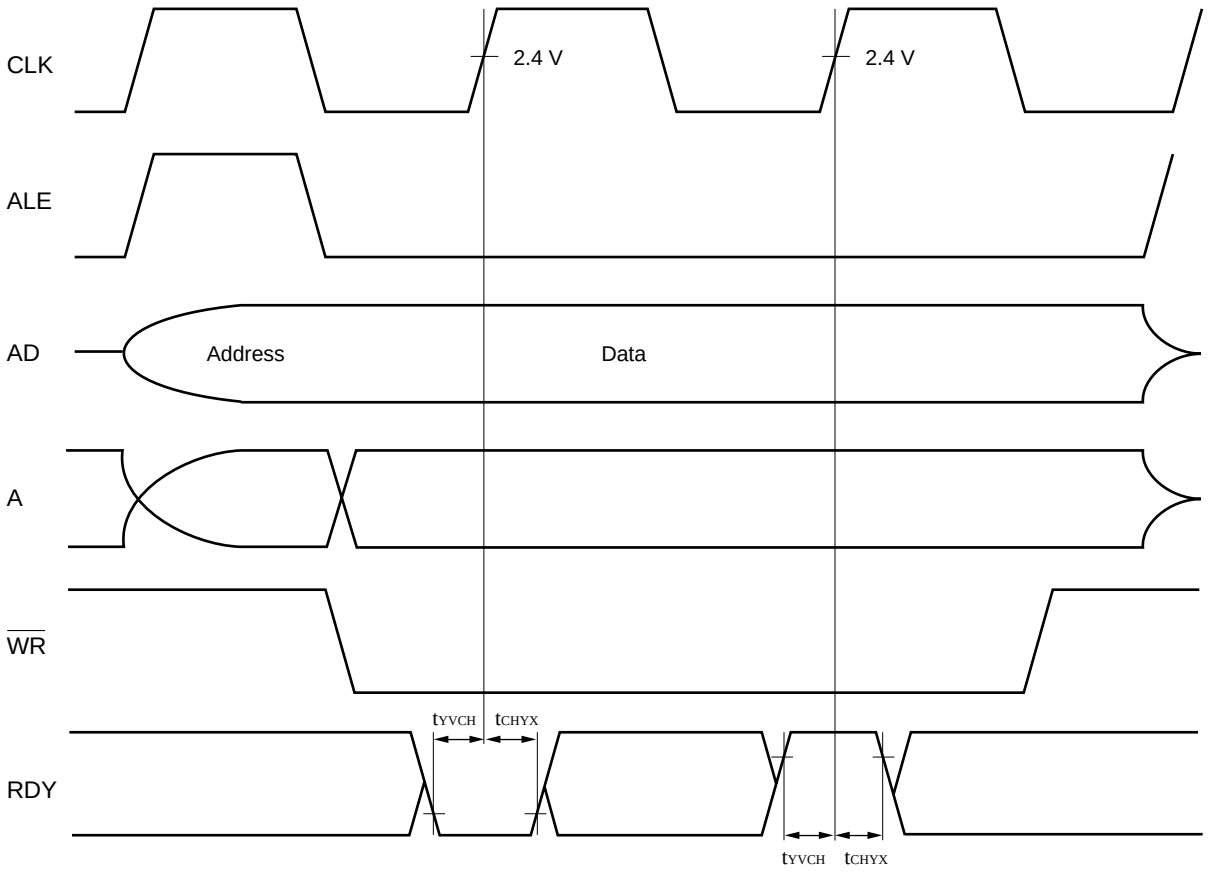


(8) Ready Input Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY valid → CLK ↑ time	t_{YVCH}	RDY, CLK	—	60	—	ns	*
CLK ↑ → RDY invalid time	t_{CHYX}			0	—	ns	*

*: These characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

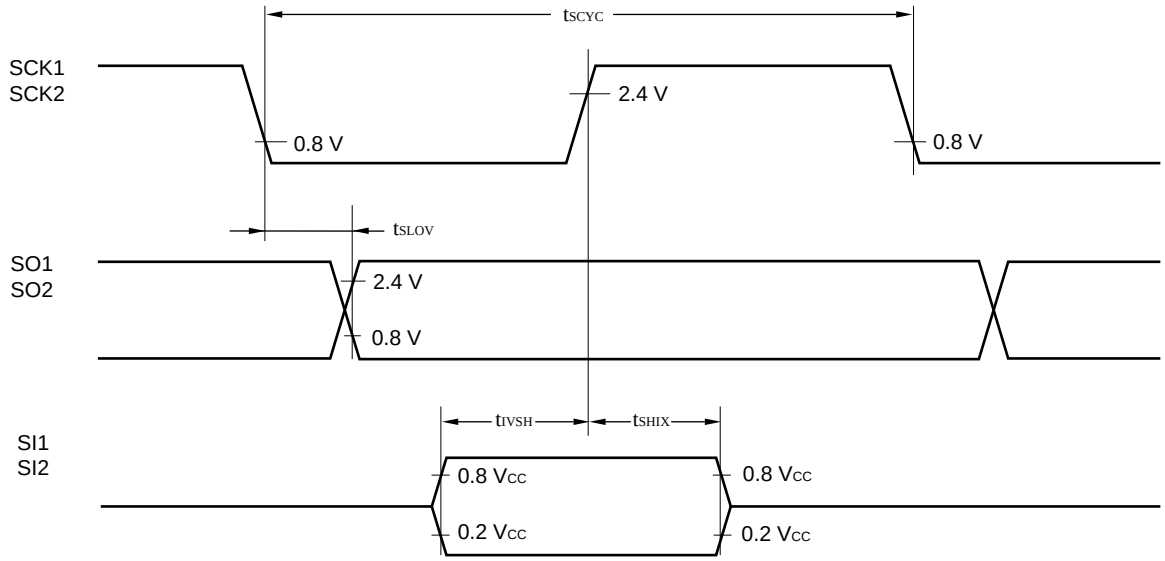
(9) Serial I/O Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

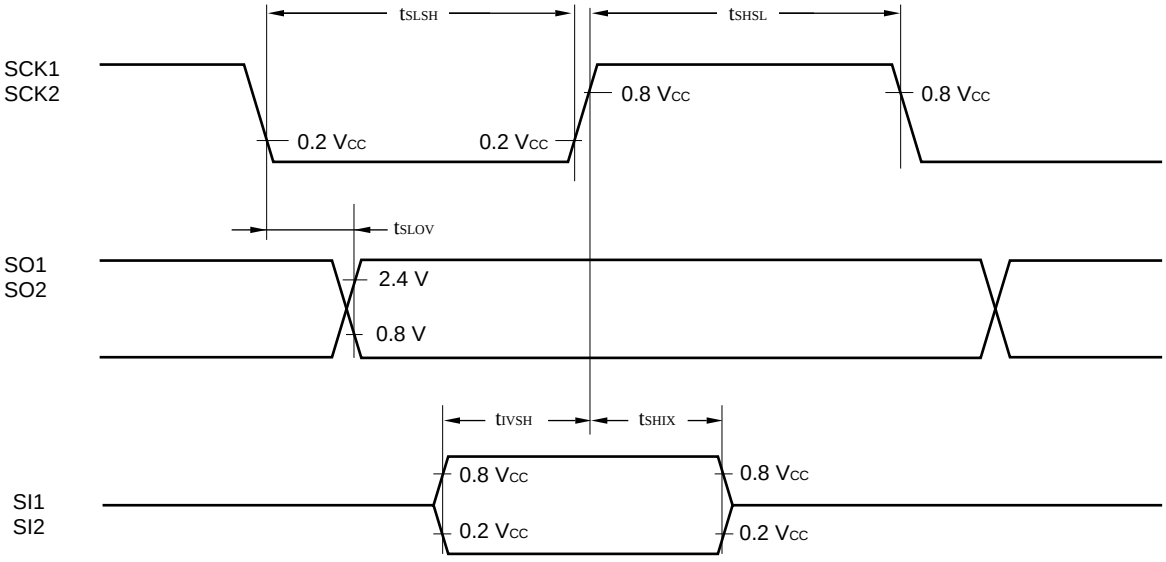
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, SCK2	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		–200	200	ns	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, SCK2	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK1, SCK2		1 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	

*: For information on t_{inst}, see “(4) Instruction Cycle.”

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**

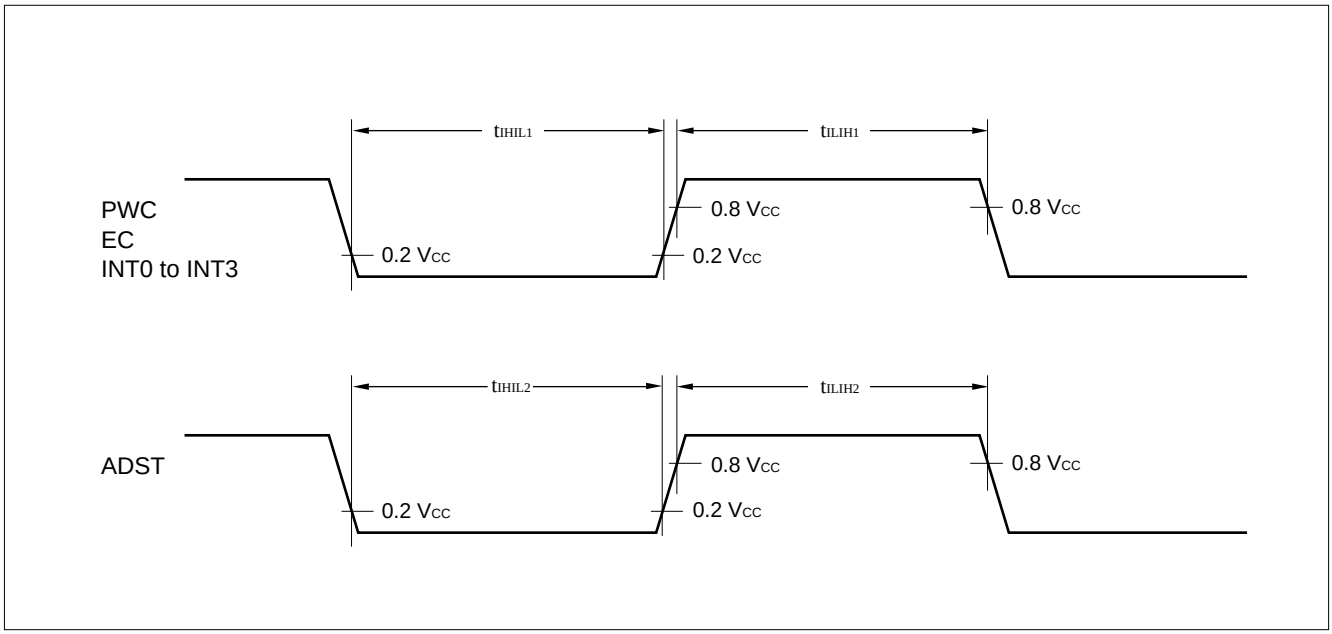


(10) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	PWC, EC, INT0 to INT3	—	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}			2 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	ADST	A/D mode	32 t_{inst}*	—	µs	
Peripheral input “L” pulse width 2	t_{IHIL2}			32 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}		Sense mode	8 t_{inst}*	—	µs	
Peripheral input “L” pulse width 2	t_{IHIL2}			8 t_{inst}*	—	µs	

*: For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

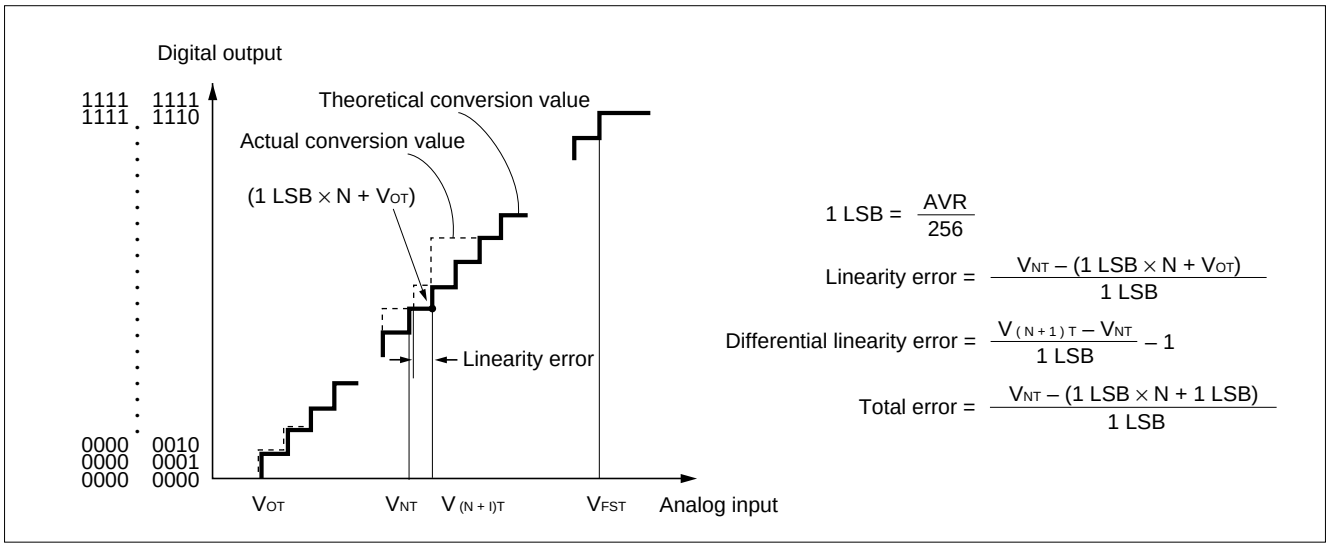
(AV_{CC} = V_{CC} = +3.5 V to +6.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error			AVR = AV_{CC}	—	—	±1.5	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V_{OT}			AV_{SS} – 1.0 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.0 LSB	mV	
Full-scale transition voltage	V_{FST}			AVR – 3.0 LSB	AVR – 1.5 LSB	AVR	mV	
Interchannel disparity	—			—	—	0.5	LSB	
A/D mode conversion time			—	—	44 t_{inst}*	—	µs	
Sense mode conversion time				—	12 t_{inst}*	—	µs	
Analog port input current	I_{AIN}	AN0 to AN7		—	—	10	µA	
Analog input voltage	—			0.0	—	AVR	V	
Reference voltage	—	AVR		0.0	—	AV_{CC}	V	
Reference voltage supply current	I_R		AVR = 5.0 V, when starting A/D conversion	—	100	—	µA	
	I_{RH}		AVR = 5.0 V, when stopping A/D conversion	—	—	1	µA	

*: For information on t_{inst}, see “(4) Instruction Cycle” in “4 AC Characteristics.”

6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
  When the number of bits is 8, analog voltage can be divided into 2^8 = 256.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



7. Notes on Using A/D Converter

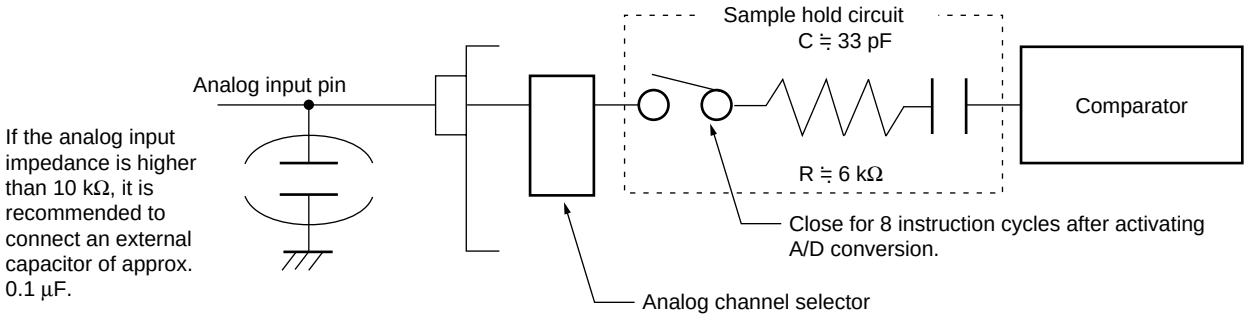
- **Input impedance of the analog input pins**

  The A/D converter contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 µF for the analog input pin.

- **Analog Input Equivalent Circiut**

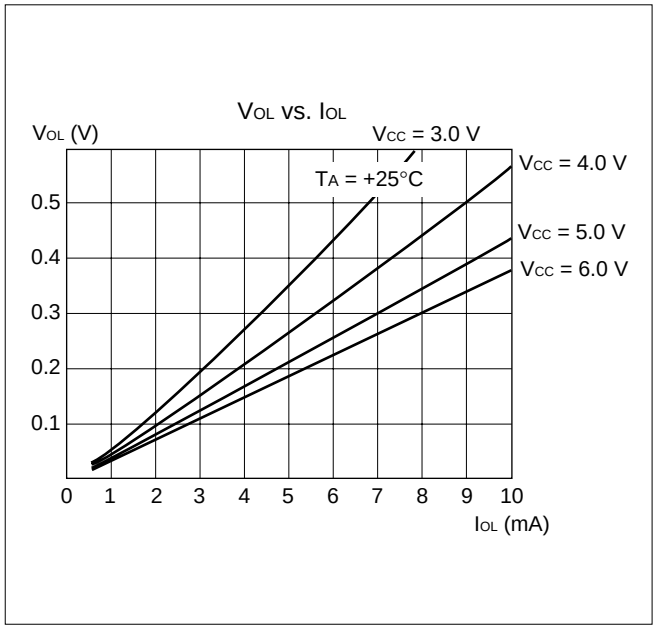


- **Error**

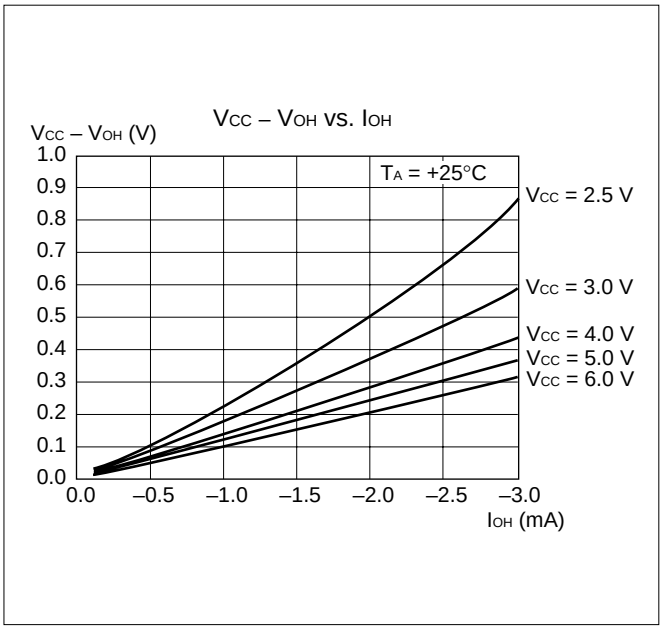
  The smaller the | AVR – AVSS |, the greater the error would become relatively.

■ EXAMPLE CHARACTERISTICS

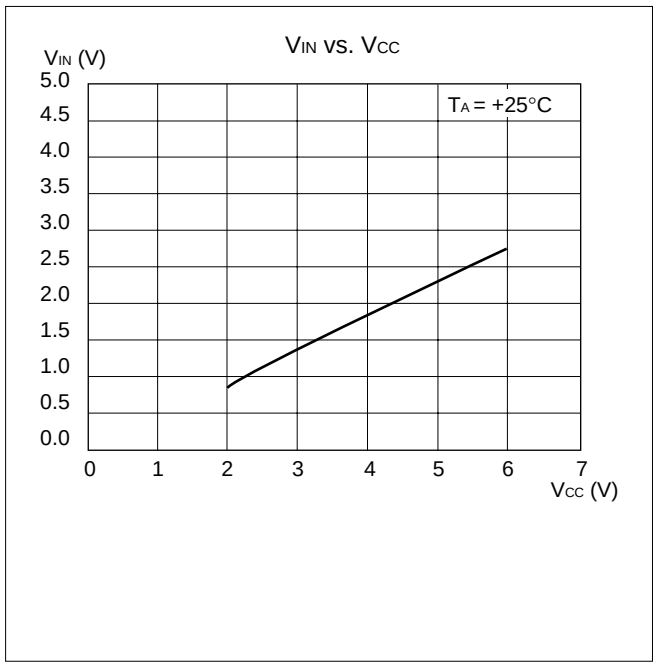
(1) "L" Level Output Voltage



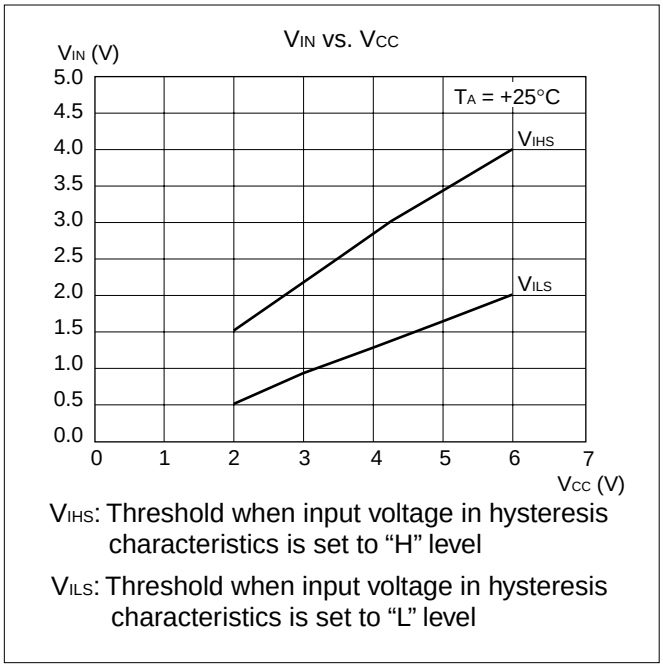
(2) "H" Level Output Voltage



(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



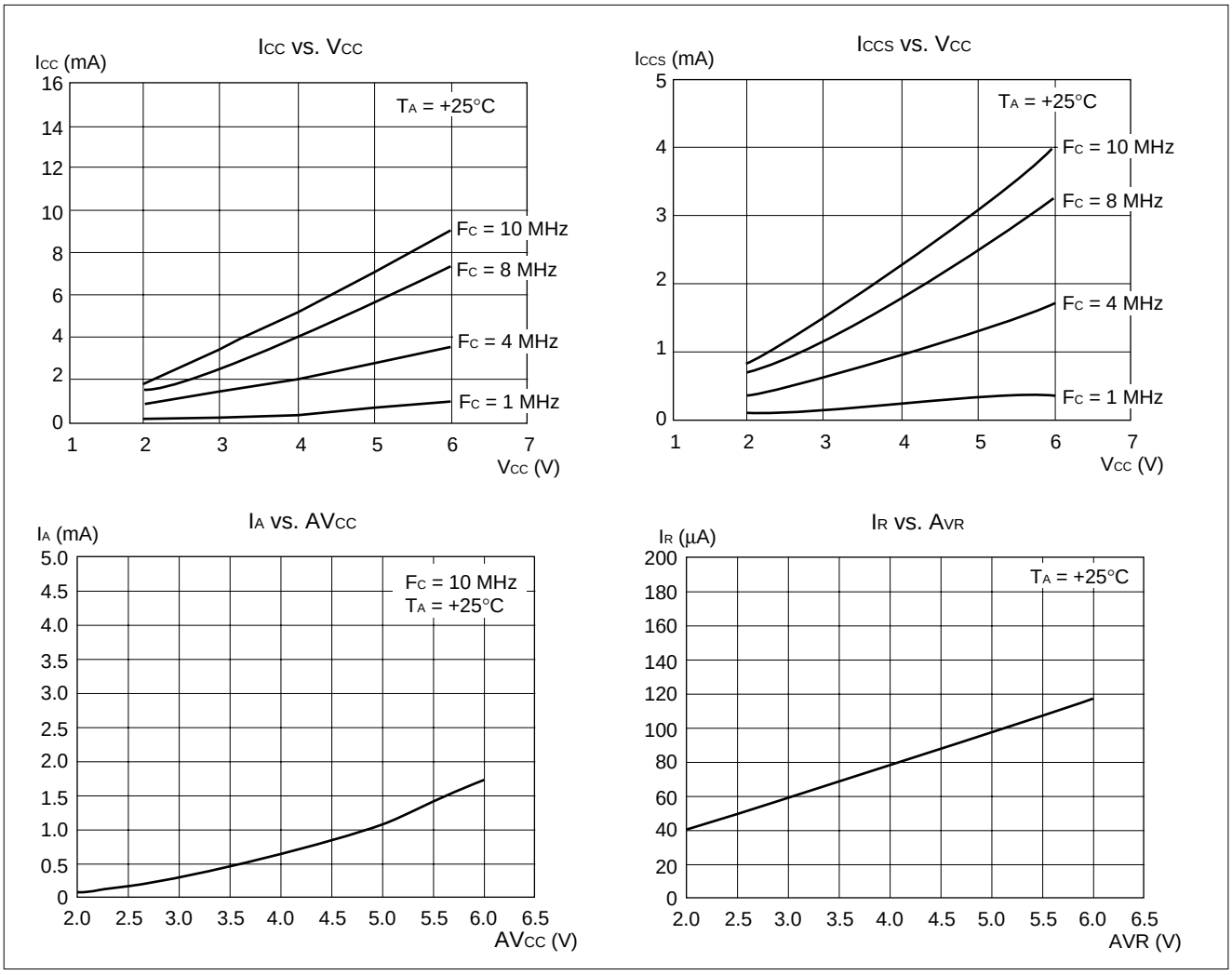
(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)



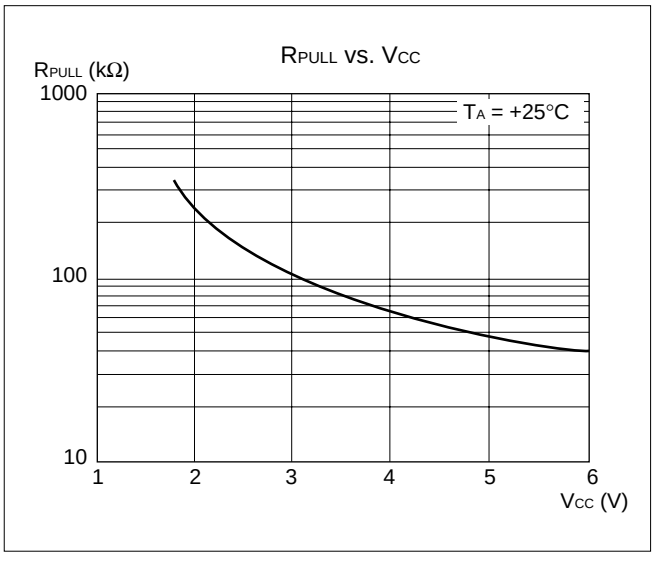
V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to "H" level

V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to "L" level

(5) Power Supply Current (External Clock)



(6) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No.	Part number	MB89623R MB89625R MB89626R MB89627R	MB89P625 MB89W625 MB89P627 MB89W627	MB89PV620 MB89T627R
	Specifying procedure	**Specify when ordering masking**	**Set with EPROM programmer**	**Setting not possible**
1	Pull-up resistors P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P64	Selectable per pin. (P50 to P57 must be set to without a pull-up resistor when an A/D converter is used.)	Can be set per pin. (P40 to P47 are available only for without a pull-up resistor.)	Fixed to without pull-up resistor
2	Power-on reset selection With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to with power-on reset
3	Oscillation stabilization time selection Crystal oscillator: $2^{18}/F_C$(s)) Ceramic oscillator: $2^{14}/F_C$(s))	Selectable	Setting possible	Crystal oscillator ($2^{18}/F_C$(s))
4	Reset pin output With reset output Without reset output	Selectable	Setting possible	With reset output

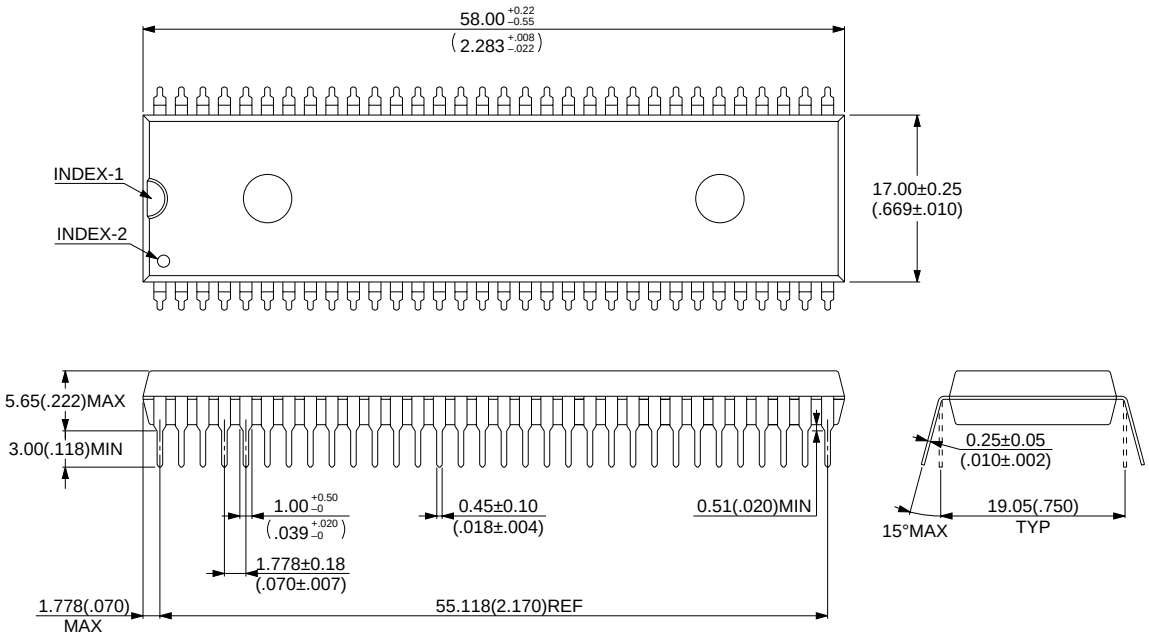
Note: Reset is input asynchronized with the internal clock whether with or without power-on reset.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89623RP-SH MB89625RP-SH MB89626RP-SH MB89627RP-SH MB89P625P-SH MB89P627-SH MB89T627RP-SH	64-pin Plastic SH-DIP (DIP-64P-M01)	
MB89623RPFV MB89625RPFV	64-pin Plastic LQFP (FPT-64P-M03)	Lead pitch: 0.5 mm
MB89623RPF MB89625RPF MB89626RPF MB89627RPF MB89P625PF MB89P627PF MB89T623RPF MB89T625RPF MB89T627RPF	64-pin Plastic QFP (FPT-64P-M06)	Lead pitch: 1.0 mm
MB89623RPFM MB89625RPFM MB89626RPFM MB89627RPFM MB89P625PFM MB89T627RPFM	64-pin Plastic QFP (FPT-64P-M09)	Lead pitch: 0.65 mm
MB89W625C-SH MB89W627C-SH	64-pin Ceramic SH-DIP (DIP-64C-A06)	
MB89PV620CF	64-pin Ceramic MQFP (MQP-64C-P01)	
MB89PV620C-SH	64-pin Ceramic MDIP (MDP-64C-P02)	

■ PACKAGE DIMENSIONS

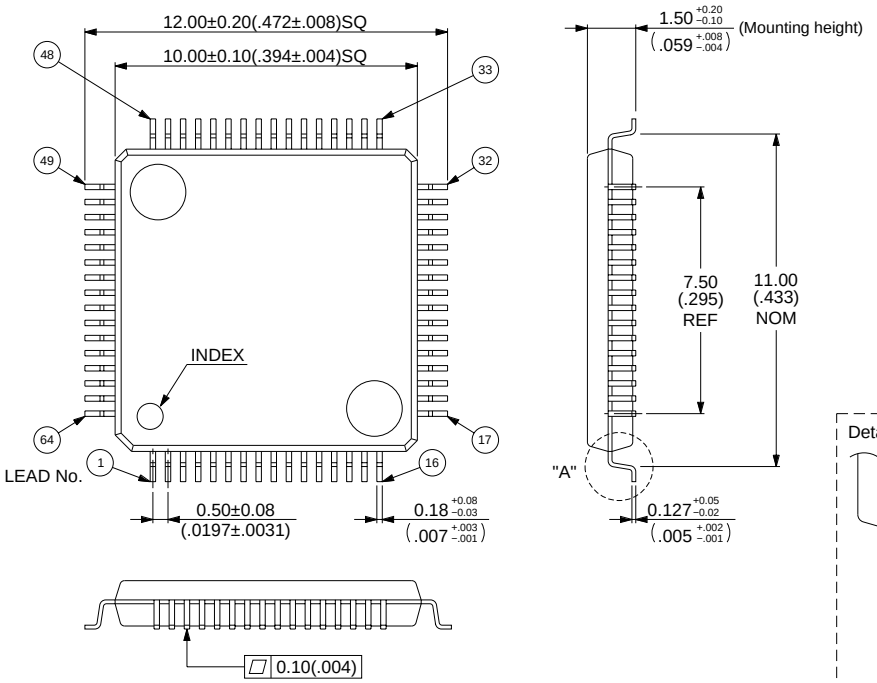
64-pin Plastic SH-DIP
(DIP-64P-M01)



© 1994 FUJITSU LIMITED D64001S-3C-4

Dimensions in mm (inches)

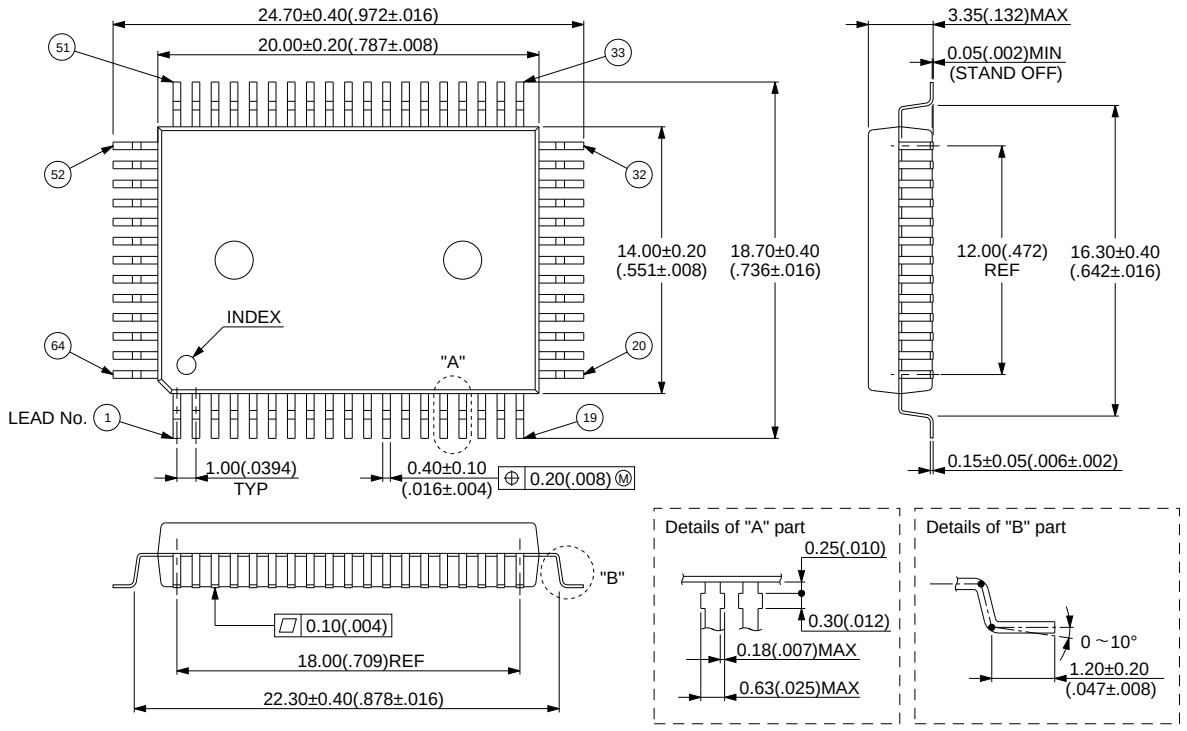
64-pin Plastic LQFP
(FPT-64P-M03)



© 1995 FUJITSU LIMITED F64009S-2C-5

Dimensions in mm (inches)

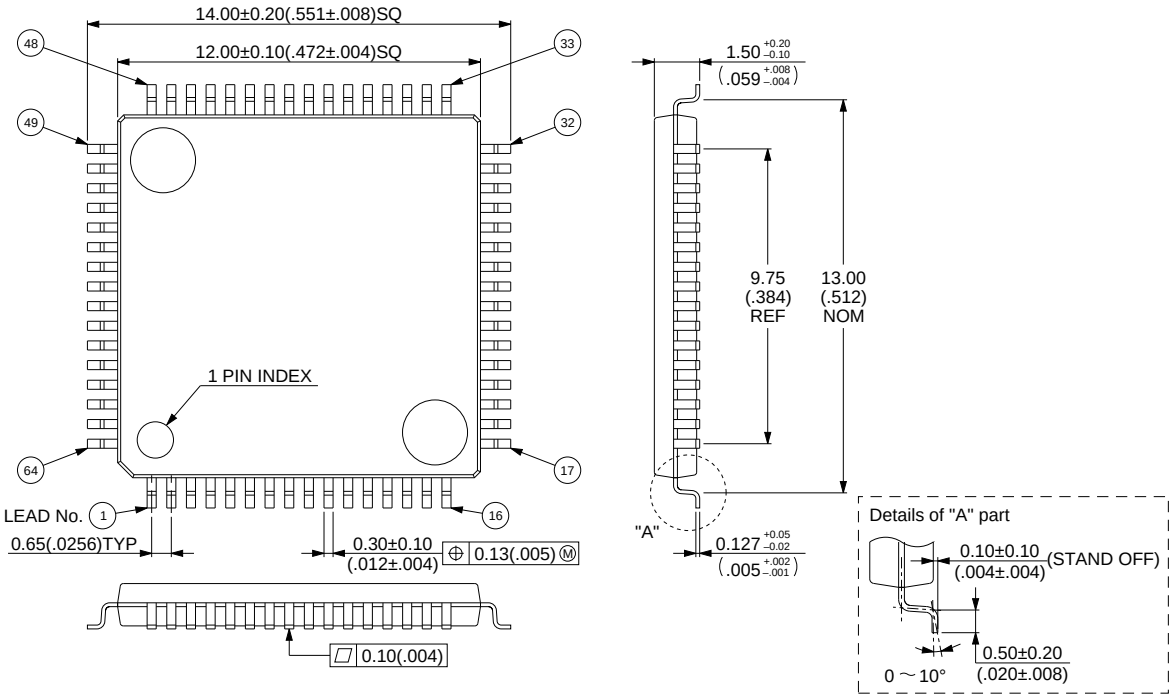
64-pin Plastic QFP
(FPT-64P-M06)



© 1994 FUJITSU LIMITED F64013S-3C-2

Dimensions in mm (inches)

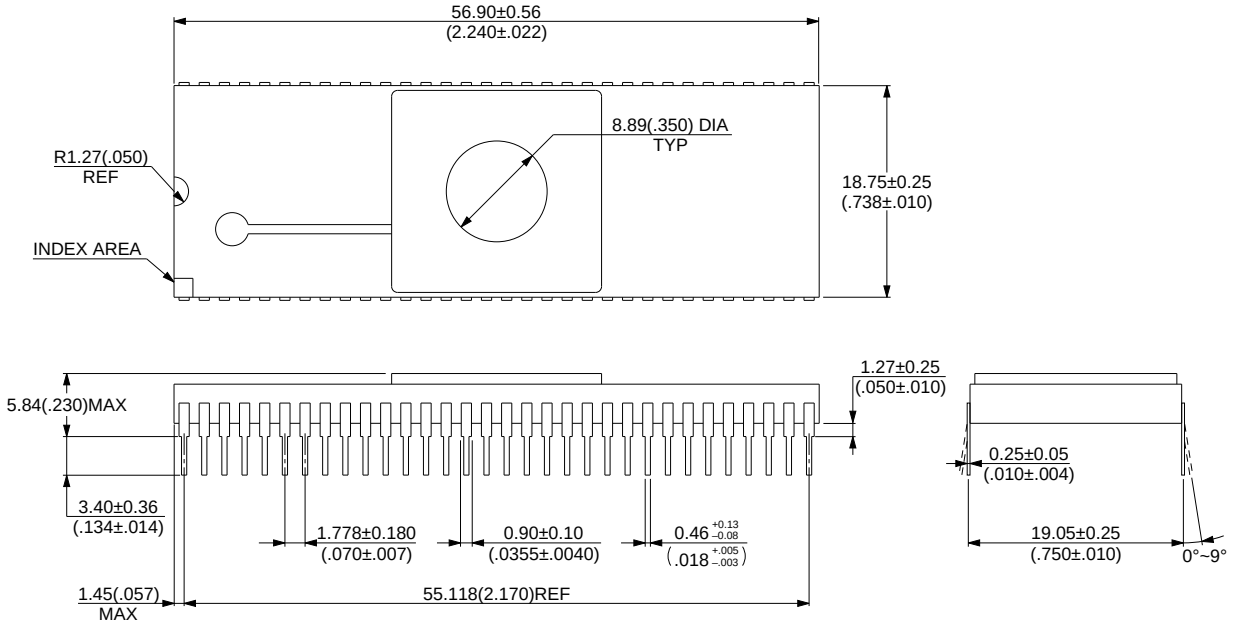
64-pin Plastic QFP
(FPT-64P-M09)



© 1994 FUJITSU LIMITED F64018S-1C-2

Dimensions in mm (inches)

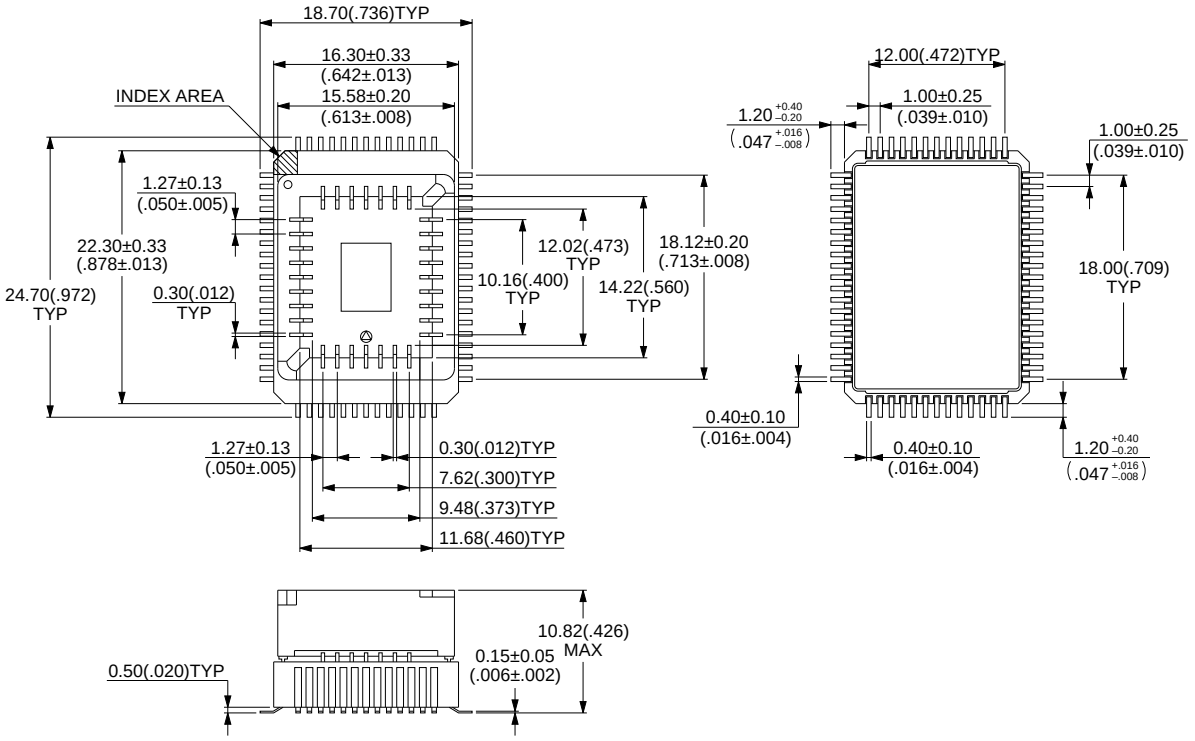
64-pin Ceramic SH-DIP
(DIP-64C-A06)



© 1994 FUJITSU LIMITED D64006SC-1-2

Dimensions in mm (inches)

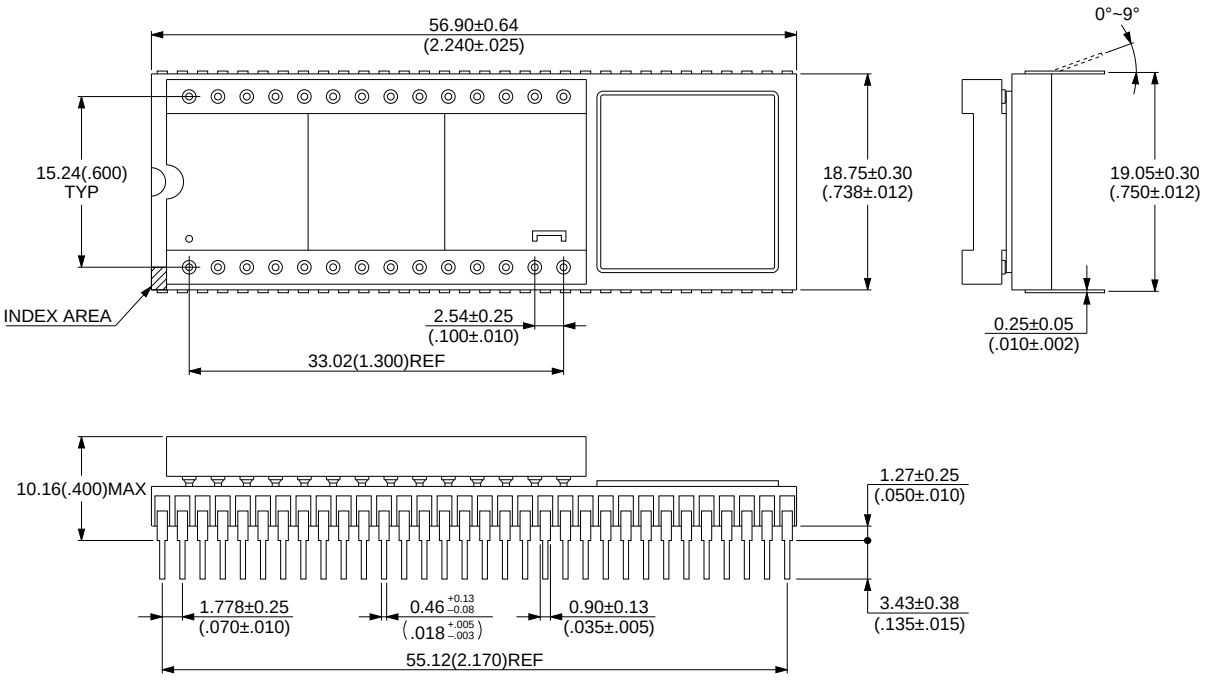
64-pin Ceramic MQFP
(MQP-64C-P01)



© 1994 FUJITSU LIMITED M64004SC-1-3

Dimensions in mm (inches)

64-pin Ceramic MDIP
(MDP-64C-P02)



© 1994 FUJITSU LIMITED M64002SC-1-4

Dimensions in mm (inches)

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

North and South America
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

Europe
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

F9703
© FUJITSU LIMITED Printed in Japan

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).
CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.