DGT305RE

Reverse Blocking Gate Turn-off Thyristor

Replaces February 2002 version, issue DS5520-2.0

DS5520-3.0 July 2004

FEATURES

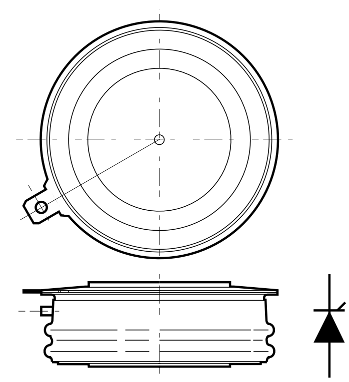
- Double Side Cooling
- Reverse Blocking Capability
- High Reliability In Service
- High Voltage Capability
- Fault Protection Without Fuses
- High Surge Current Capability
- Turn-off Capability Allows Reduction In Equipment Size And Weight. Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements

APPLICATIONS

- Variable speed A.C. motor drive inverters (VSD-AC)
- Uninterruptable Power Supplies
- High Voltage Converters
- Choppers
- Welding
- Induction Heating
- DC/DC Converters

KEY PARAMETERS

I_{TCM}	700A
V_{DRM}	1800V
$I_{T(AV)}$	240A
dV_D/dt	500V/µs
di_T/dt	500A/µs



Outline type code: E

(See Package Details for further information)

Fig. 1 Package outline

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V	Conditions
DGT305SE18	1800	1800	T_{vj} = 125°C, I_{DM} = 50mA, I_{RRM} = 50mA, V_{RG} = 2V

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TCM}	Repetitive peak controllable on-state current	V_D = 67%V_{DRM}, T_j = 125°C, di_{GQ}/dt = 15A/µs, Cs = 1.5µF	700	A
$I_{T(AV)}$	Mean on-state current	T_{HS} = 80°C. Double side cooled. Half sine 50Hz.	240	A
$I_{T(RMS)}$	RMS on-state current	T_{HS} = 80°C. Double side cooled. Half sine 50Hz.	373	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine. T_j = 125°C	4.0	kA
I^2t	I^2t for fusing	10ms half sine. T_j =125°C	80000	A^2s
di_T/dt	Critical rate of rise of on-state current	V_D = 67% V_{DRM}, I_T = 700A, T_j = 125°C, I_{FG} > 20A, Rise time < 1.0µs	500	A/µs
dV_D/dt	Rate of rise of off-state voltage	To 80% V_{DRM}; R_{GK} ≤ 1.5Ω, T_j = 125°C	500	V/µs
V_{DP}	Peak forward transient voltage during current fall time	V_D = 67% V_{DRM}, I_T = 700A, T_j = 125°C, di_{GQ}/dt =15A/µs, Cs = 1.5µF	400	V

GATE RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{RGM}	Peak reverse gate voltage	This value maybe exceeded during turn-off	-	16	V
I_{FGM}	Peak forward gate current		-	50	A
$P_{FG(AV)}$	Average forward gate power		-	10	W
P_{RGM}	Peak reverse gate power		-	6	kW
di_{GQ}/dt	Rate of rise of reverse gate current		10	50	A/µs
$t_{ON(min)}$	Minimum permissable on time		20	-	µs
$t_{OFF(min)}$	Minimum permissable off time		40	-	µs

THERMAL RATINGS

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-hs)}$	DC thermal resistance - junction to heatsink surface	Double side cooled		-	0.075	°C/W
		Anode side cooled		-	0.12	°C/W
		Cathode side cooled		-	0.20	°C/W
$R_{th(c-hs)}$	Contact thermal resistance	Clamping force 5.5kN With mounting compound	per contact	-	0.018	°C/W
T_{vj}	Virtual junction temperature			-	125	°C
T_{OP}/T_{stg}	Operating junction/storage temperature range			–40	125	°C
-	Clamping force			5.0	6.0	kN

CHARACTERISTICS

T_j = 125°C unless stated otherwise

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{TM}	On-state voltage	At 600A peak, $I_{G(ON)}$ = 2A d.c.	-	2.5	V
I_{DM}	Peak off-state current	At = V_{DRM}, V_{RG} = 2V	-	50	mA
I_{RRM}	Peak reverse current	At V_{RRM}	-	50	mA
V_{GT}	Gate trigger voltage	V_D = 24V, I_T = 100A, T_j = 25°C	-	0.75	V
I_{GT}	Gate trigger current	V_D = 24V, I_T = 100A, T_j = 25°C	-	1.2	A
I_{RGM}	Reverse gate cathode current	V_{RGM} = 16V, No gate/cathode resistor	-	50	mA
E_{ON}	Turn-on energy	V_D = 1200V, I_T = 600A,	-	160	mJ
t_d	Delay time	I_{FG} = 20A, rise time < 1.0µs	-	1.1	µs
t_r	Rise time	R_L = (Residual inductance 2.75µH)	-	2.5	µs
E_{OFF}	Turn-off energy		-	550	mJ
t_{tail}	Tail time		-	30	µs
t_{gs}	Storage time	I_T =600A, V_D = 1200V,	-	12	µs
t_{gf}	Fall time	Snubber Cap Cs = 1.5µF,	-	1.5	µs
t_{gq}	Gate controlled turn-off time	di_{GQ}/dt = 15A/µs	-	13.5	µs
Q_{GQ}	Turn-off gate charge	R_L = (Residual inductance 2.75µH)	-	900	µC
Q_{GQT}	Total turn-off gate charge		-	1800	µC

CURVES

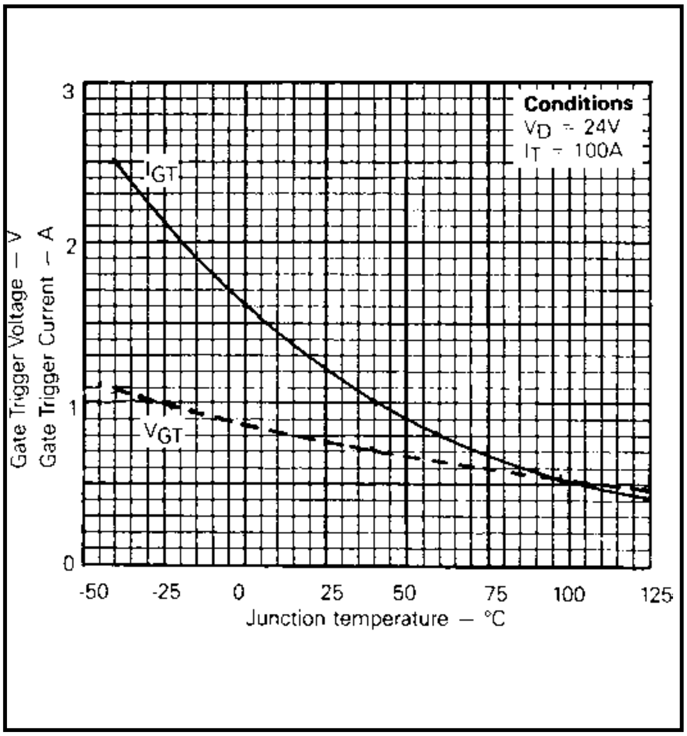


Fig.2 Gate characteristics

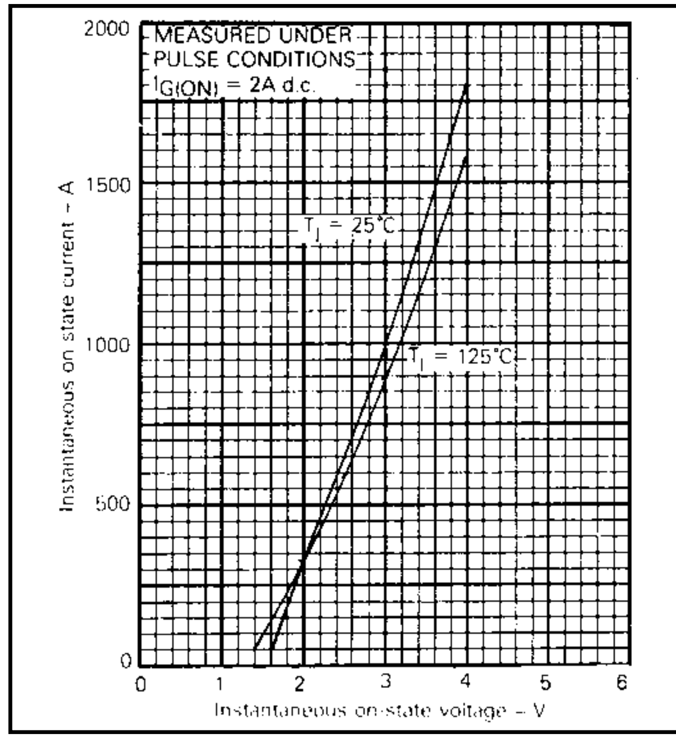


Fig.3 Maximum (limit) on-state characteristics

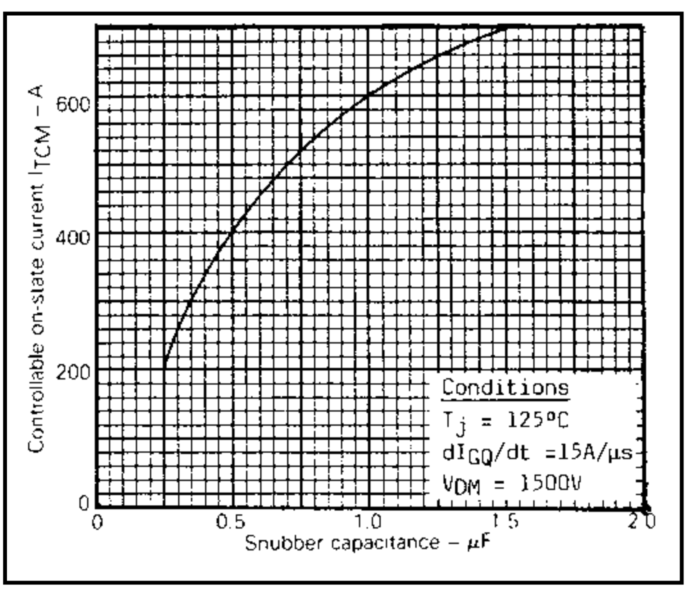


Fig.4 Dependence of I_{TCM} on C_S

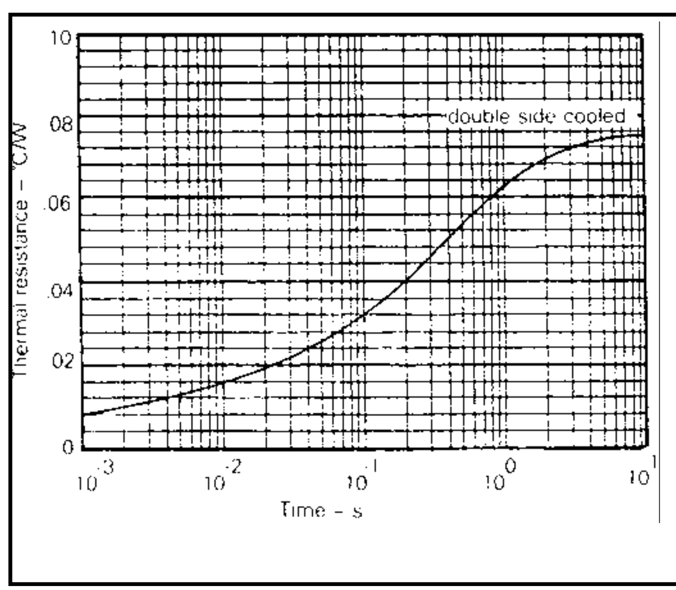


Fig.5 Maximum (limit) transient thermal resistance

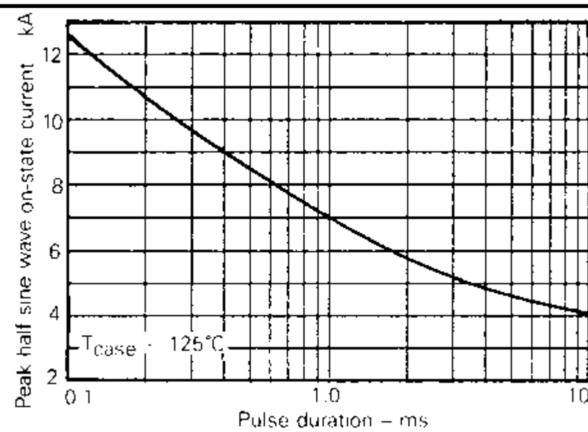


Fig.6 Surge (non-repetitive) on-state current vs time

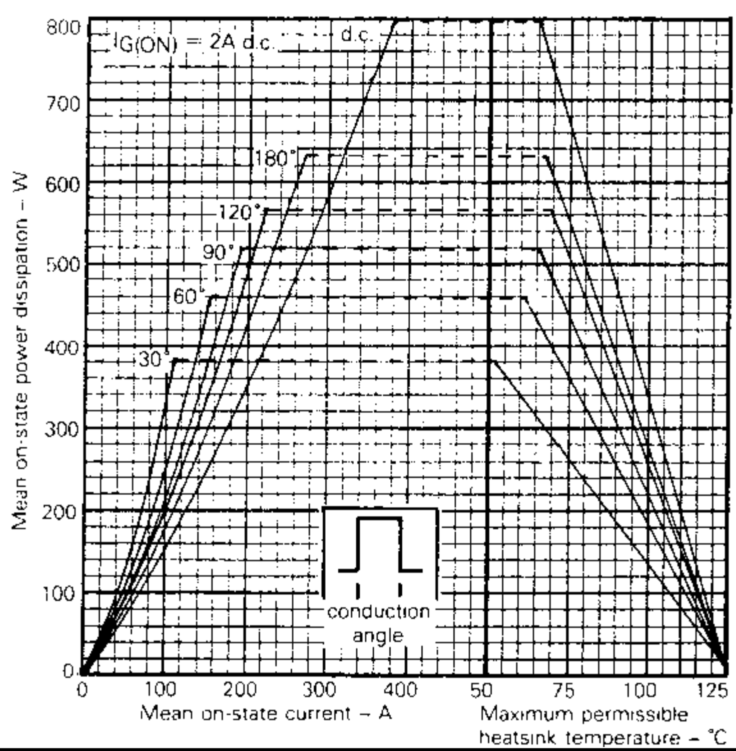


Fig.7 Steady state rectangulerwave conduction loss - double side cooled

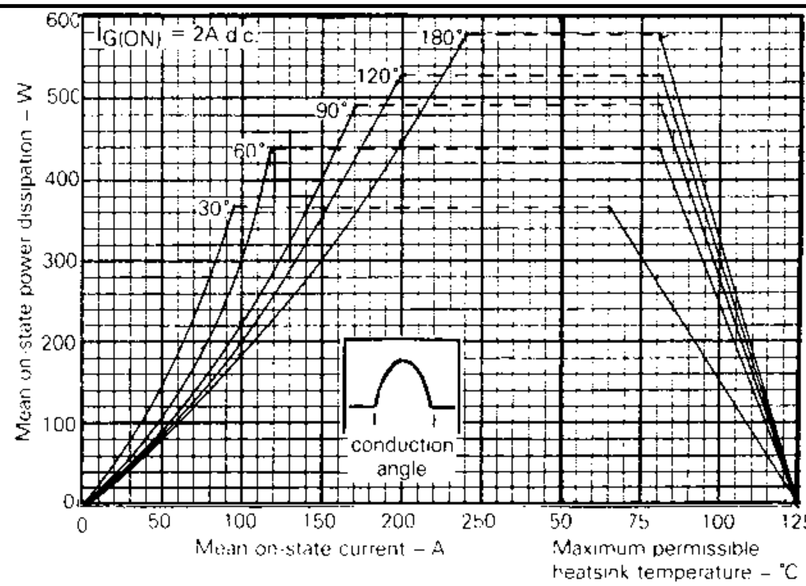


Fig.8 Steady state sinusoidal wave conduction loss - double side cooled

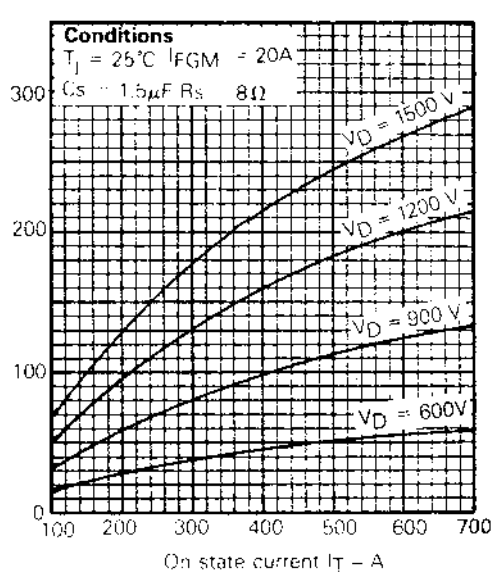


Fig.9 Turn-on energy vs on-state current

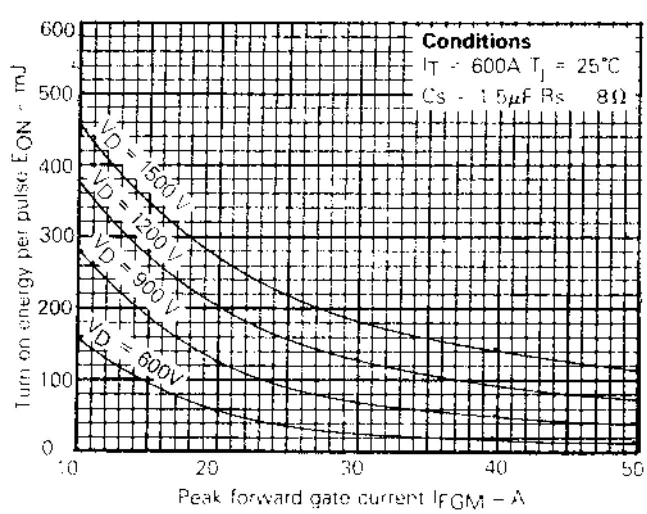


Fig.10 Turn-on energy vs peak forward gate current

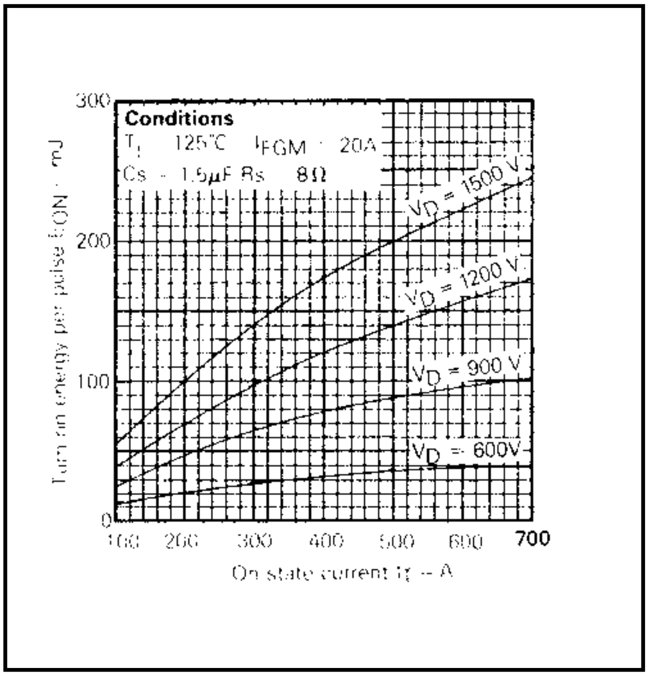


Fig.11 Turn-on energy vs on-state current

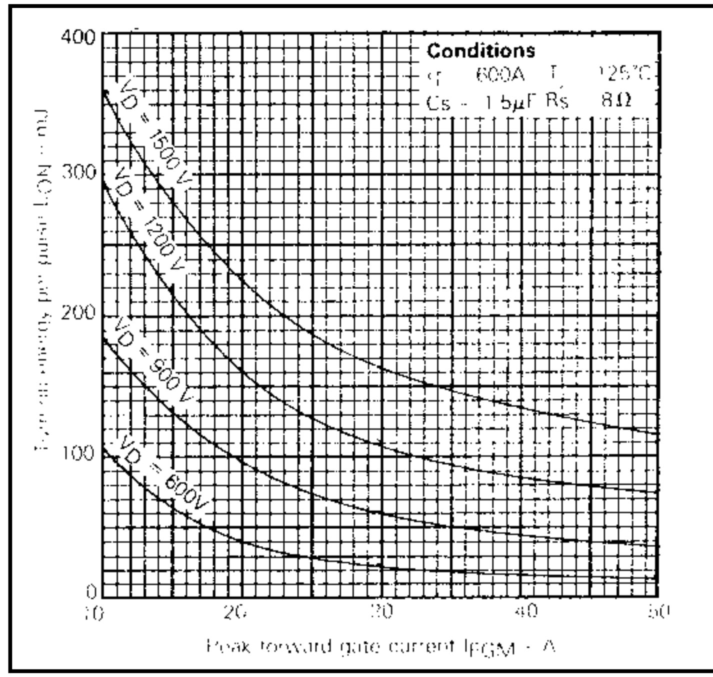


Fig.12 Turn-on energy vs peak forward gate current

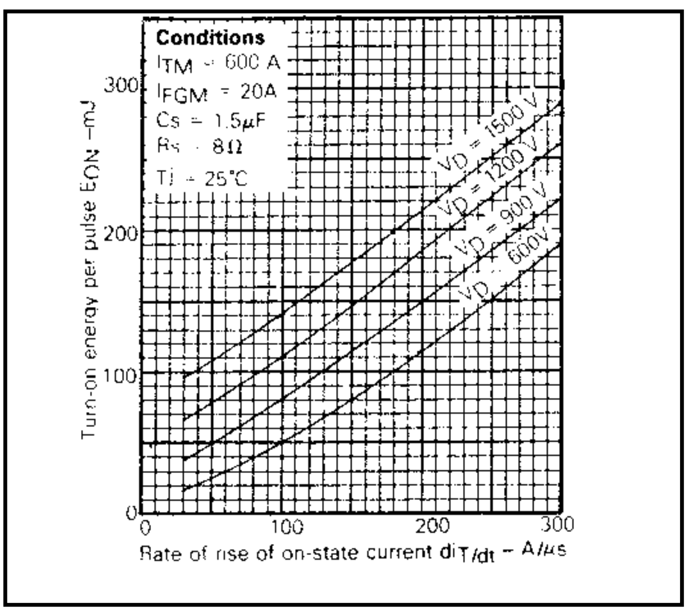


Fig.13 Turn-on energy vs rate of rise of on-state current

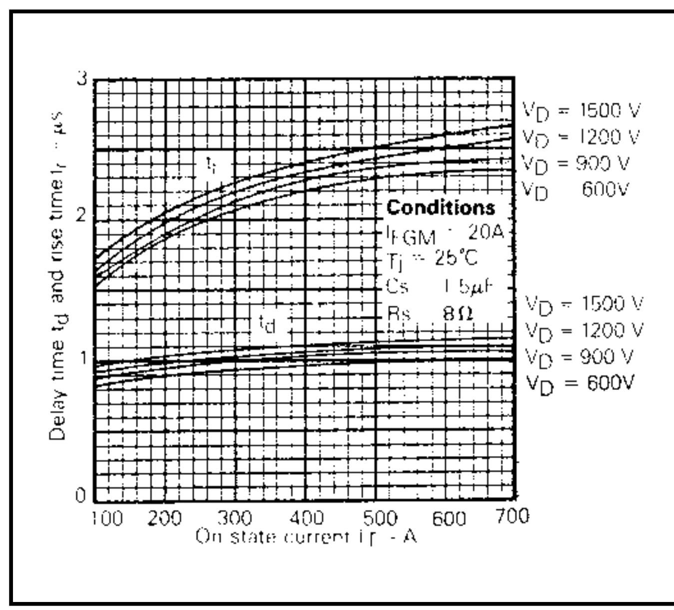


Fig.14 Delay time and rise time vs on-state current

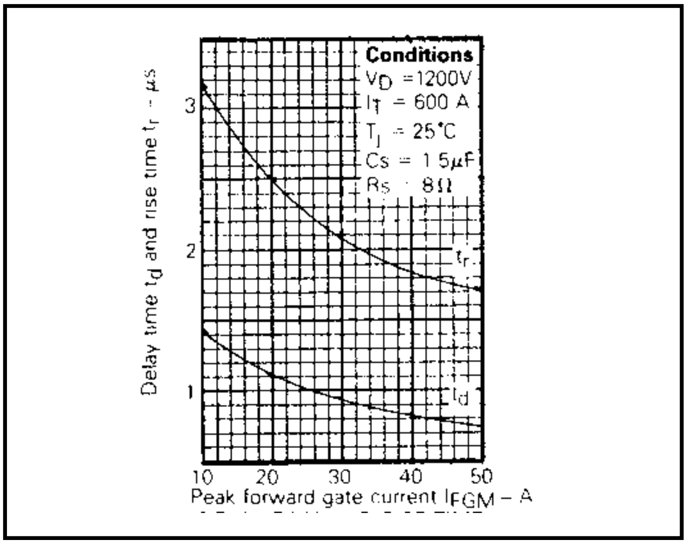


Fig.15 Delay time and rise time vs peak forward gate current

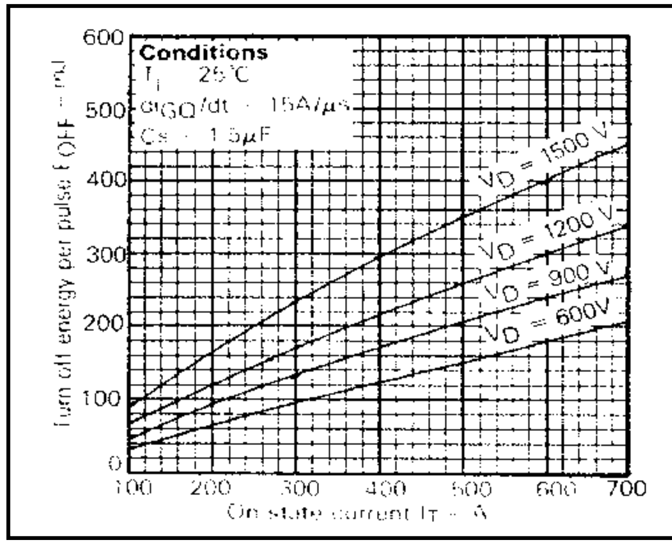


Fig.16 Turn-off energy vs on-state current

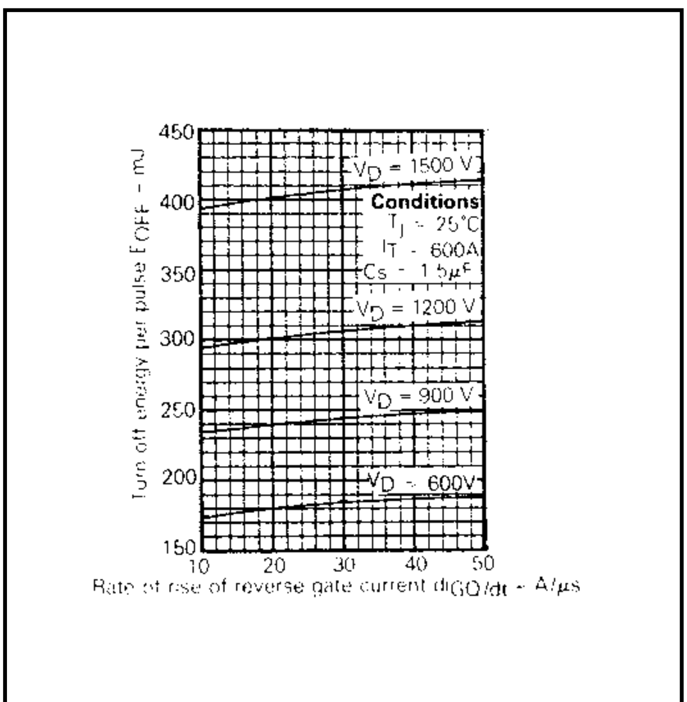


Fig.17 Turn-off energy vs rate of rise of reverse gate current

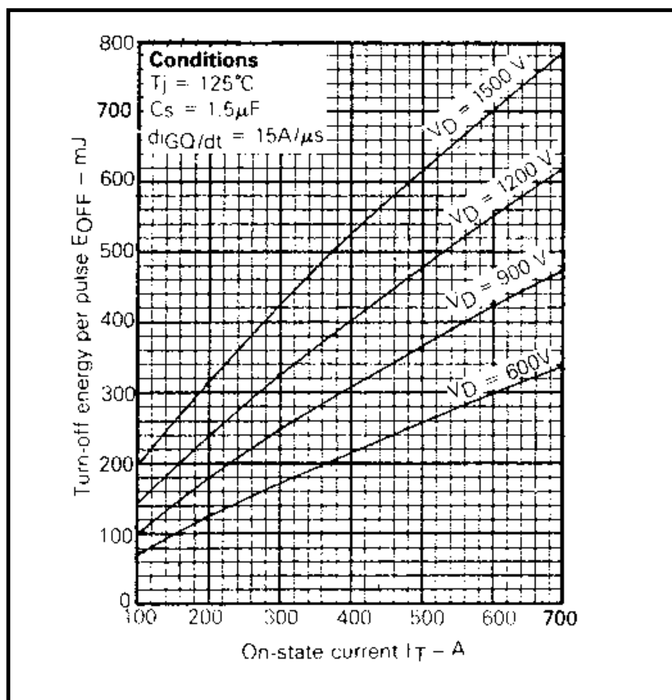


Fig.18 Turn-off energy vs on-state current

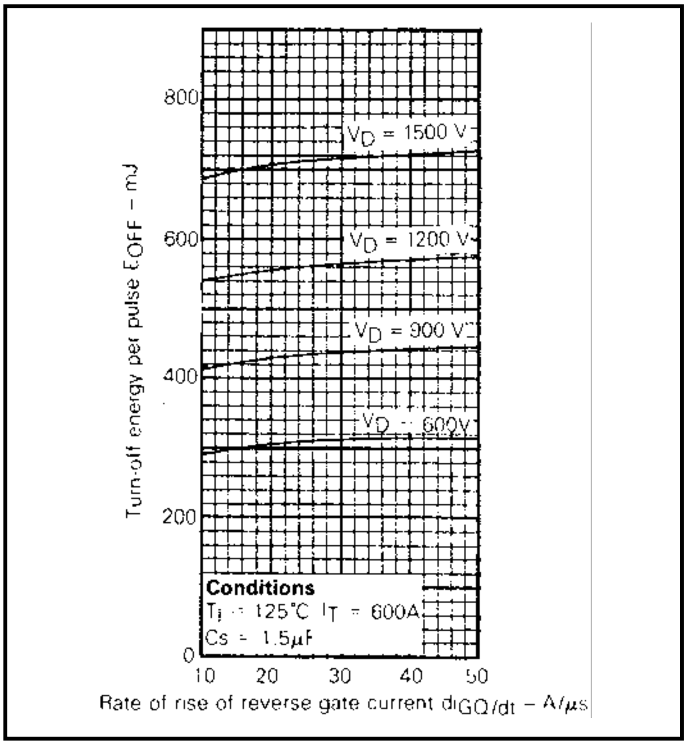


Fig.19 Turn-off energy vs rate of rise of reverse gate current

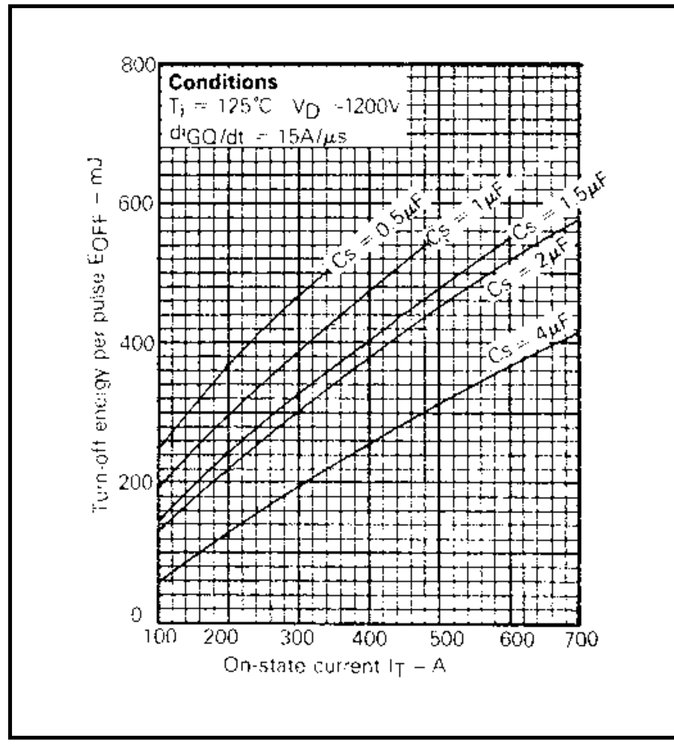


Fig.20 Turn-off energy vs on-state current with C_S as parameter

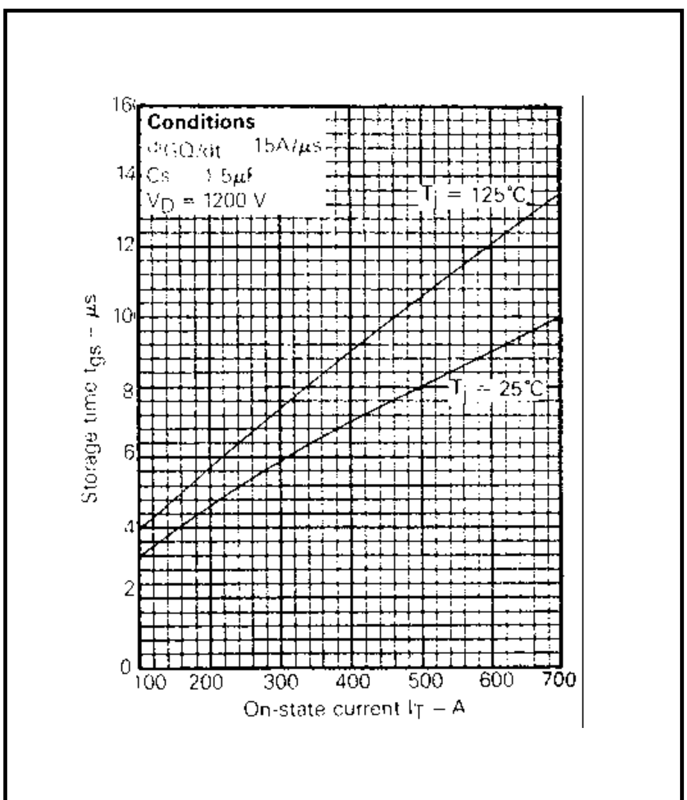


Fig.21 Storage time vs on-state current

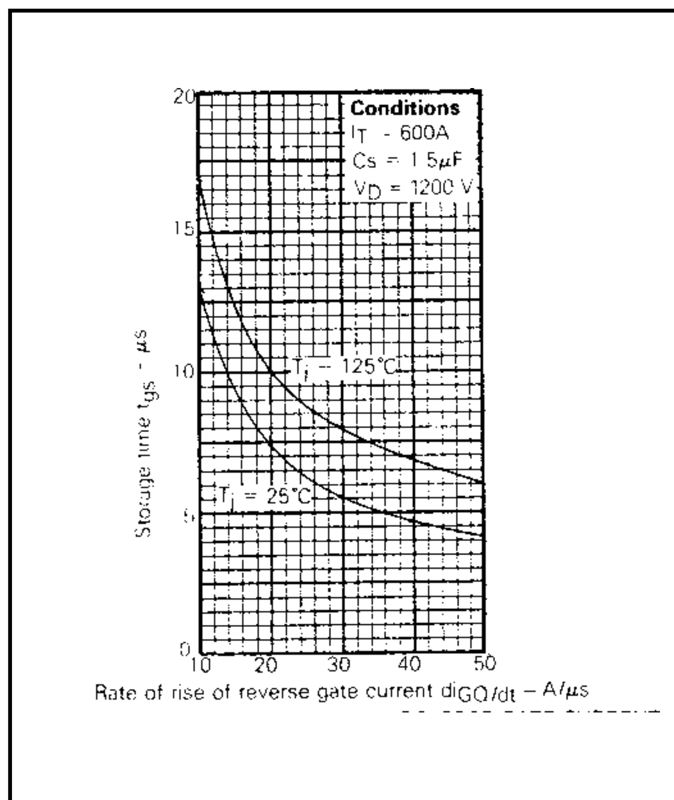


Fig.22 Storage time vs rate of rise of reverse gate current

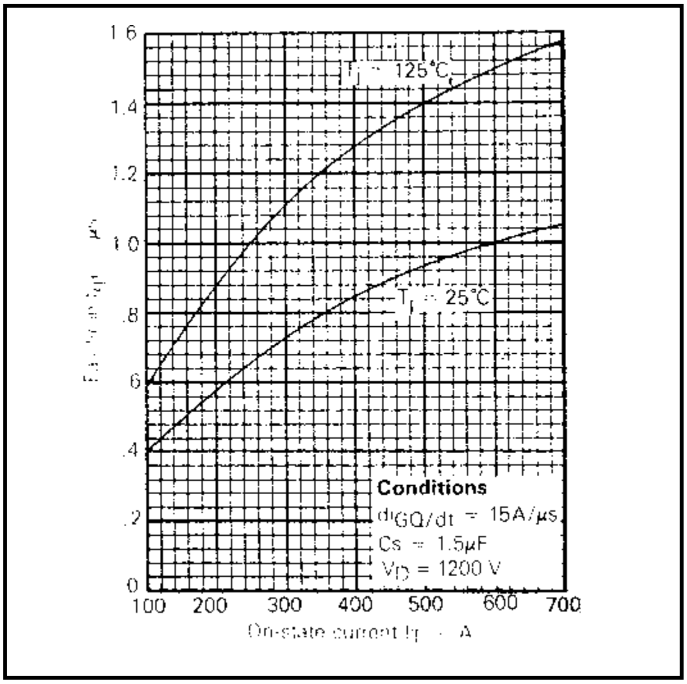


Fig.23 Fall time vs on-state current

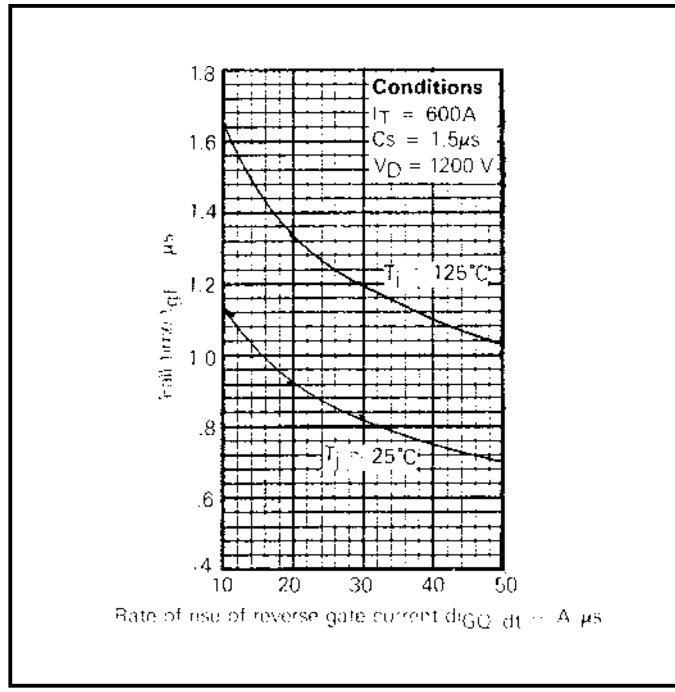


Fig.24 Fall time vs rate of rise of reverse gate current

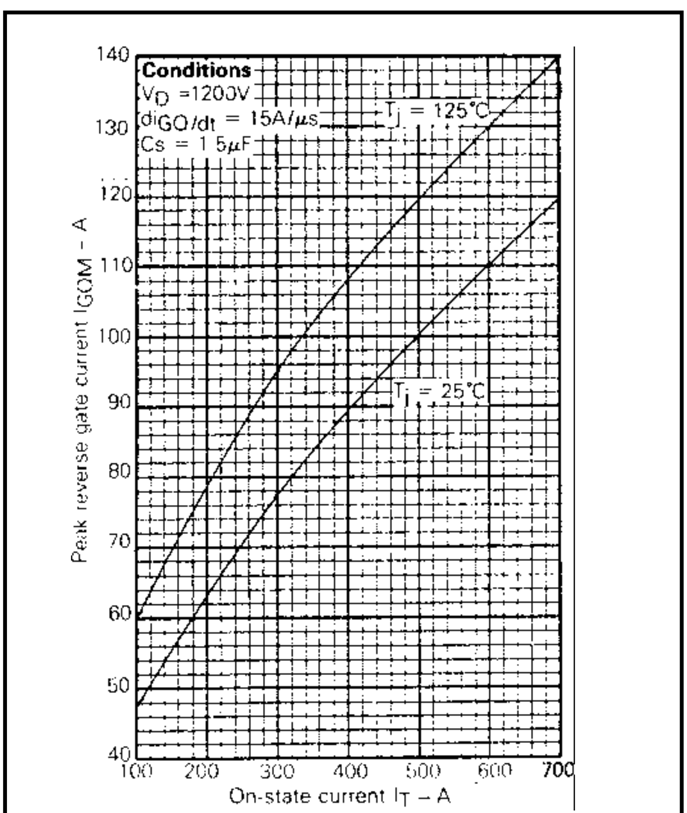


Fig.25 Peak reverse gate current vs on-state current

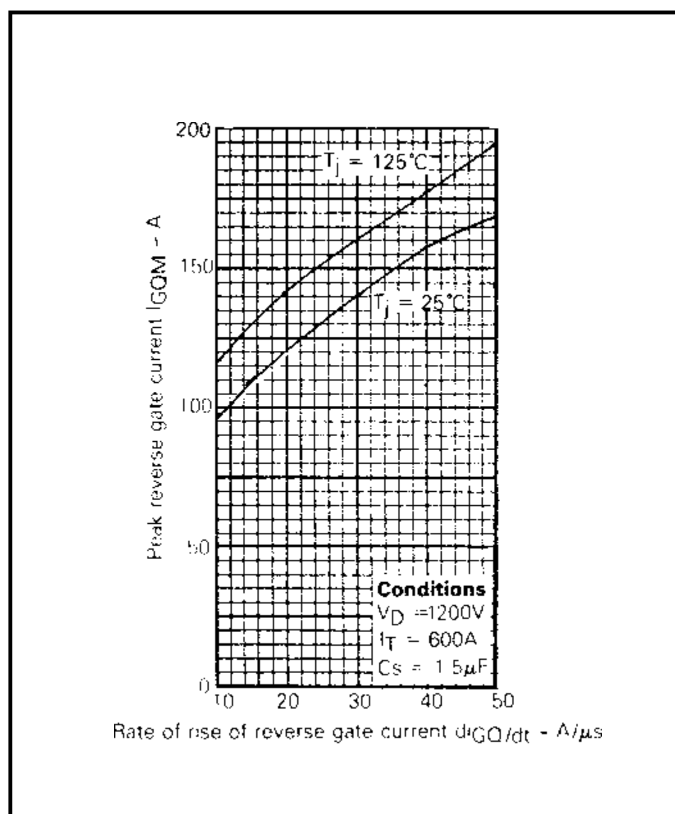


Fig.26 Peak reverse gate current vs rate of rise of reverse gate current

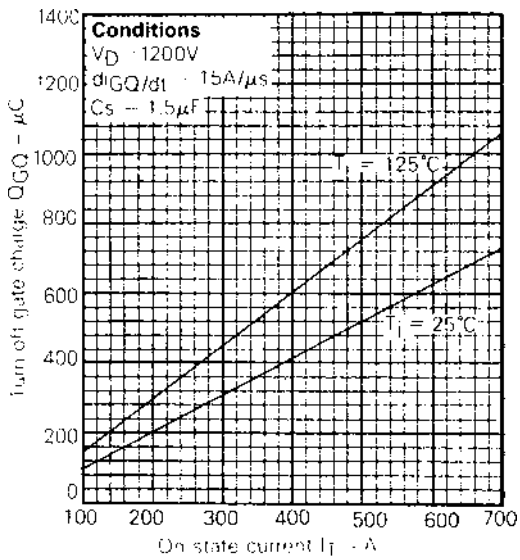


Fig.27 Turn-off gate charge vs on-state current

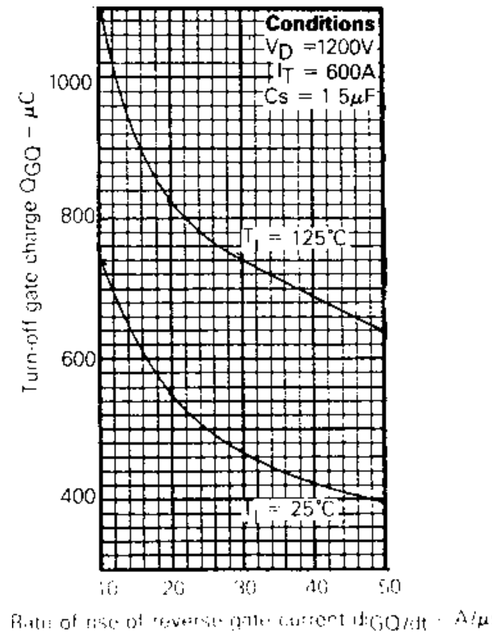


Fig.28 Turn-off gate charge vs rat of rise of reverse gate current

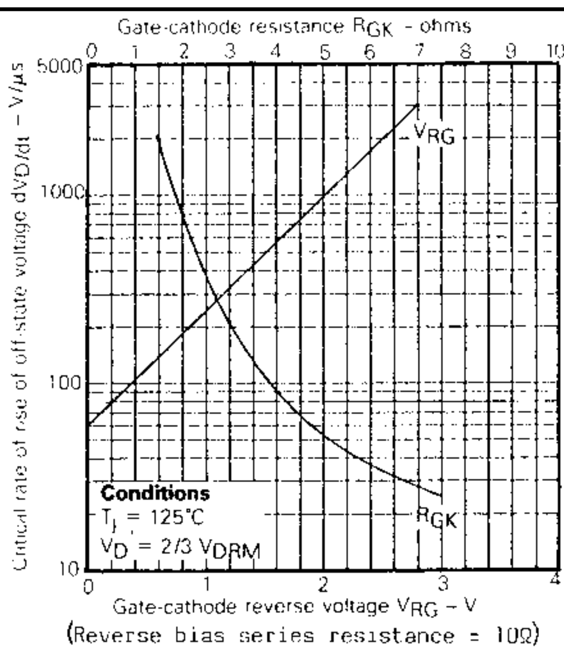
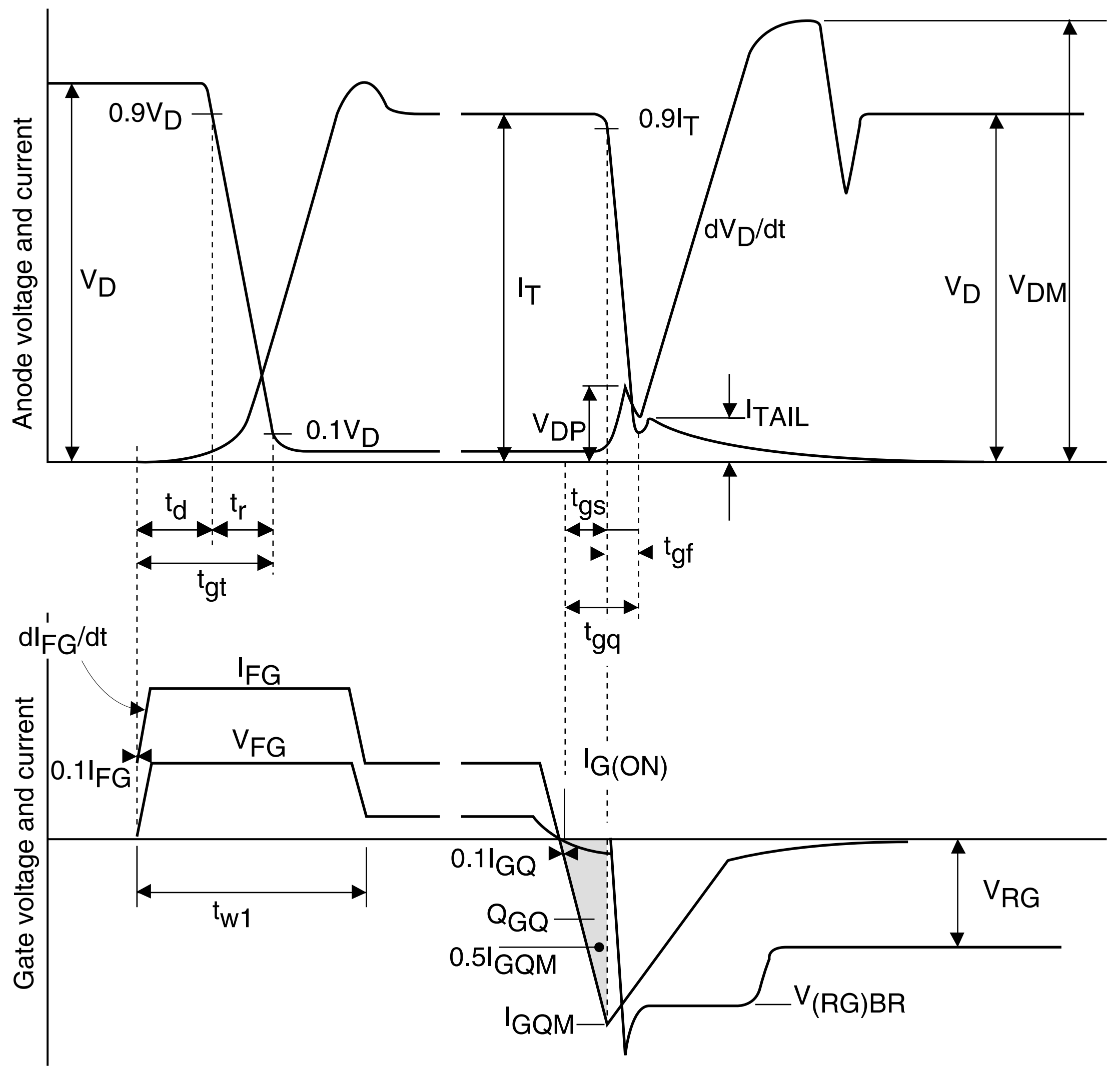


Fig.29 Dependence of critical dV_D/dt on gate-cathode resistance and gate-cathode reverse voltage

Snubber Capacitor Cs (µF)	Snubber Resistor Rs (Ω)	Minimum Reset Time (µs)
2	7	35
	5	30
1.5	7	26
	5	22
1	7	17
	5	15

Table of snubber discharge time variation with snubber capacitor value.



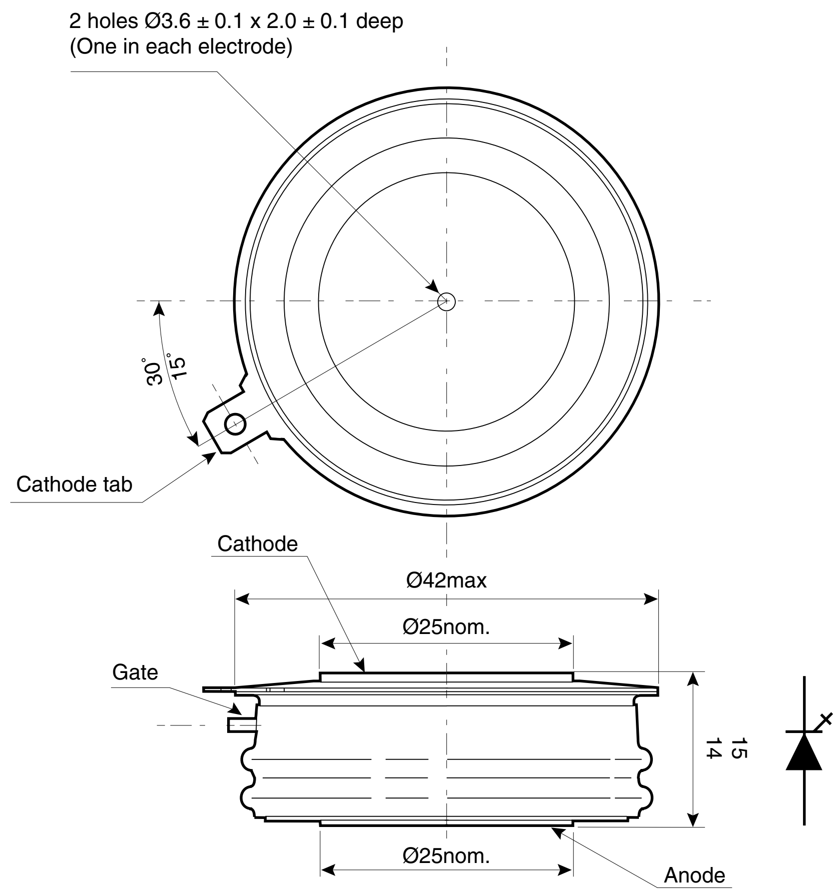
Recommended gate conditions:
I_{TCM} = 600A
I_{FG} = 20A
$I_{G(ON)}$ = 2A d.c.
$t_{w1(min)}$ = 4.5μs
I_{GQM} = 130A
di_{GQ}/dt = 15A/μs
Q_{GQ} = 900μC
$V_{RG(min)}$ = 2V
$V_{RG(max)}$ = 16V

These are recommended Dynex Semiconductor conditions. Other conditions are permitted according to users gate drive specifications.

Fig.30 General switching waveforms

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise.
DO NOT SCALE.



Nominal weight: 82g
Clamping force: 6kN ±10%

Package outline type code: E

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

http://www.dynexsemi.com

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