HARRIS SEMICONDUCTOR

HS-54C138RH

Radiation Hardened 3-Line to 8-Line Decoder/Demultiplexer

December 1992

Features

- Radiation Hardened EPI-CMOS
  - Total Dose 1 x 10^5 RAD(SI)
  - Latch-Up Immune > 1 x 10^{12} RAD(SI)/s
- Multiple Input Enable for Easy Expansion
- Single Power Supply +5V
- Outputs Active Low
- Low Standby Power (0.5mW Max at +5V)
- High Noise Immunity
- Equivalent to Sandia SA2995
- Bus Compatible with Harris Rad-Hard 80C85RH
- Full Military Temperature Range -55°C to +125°C

Description

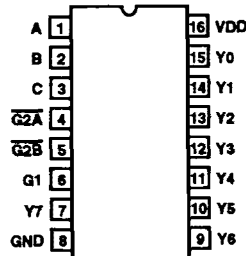
The Harris HS-54C138RH is a radiation hardened 3 to 8 decoder fabricated using a radiation hardened EPI-CMOS process. It features low power consumption, high noise immunity, and high speed. Also featured are pin and function compatibility with the 54LS138 industry standard part. The HS-54C138RH is ideally suited for high speed memory chip select address decoding. It is intended for use with the Harris HS-80C85RH radiation hardened microprocessor, but it can also be utilized as a demultiplexer in any low power rad-hard application.

The HS-54C138RH contains a one of eight binary decoder. A three bit binary input is used to select and activate each of the eight outputs, provided the three chip enable inputs are also present (see truth table).

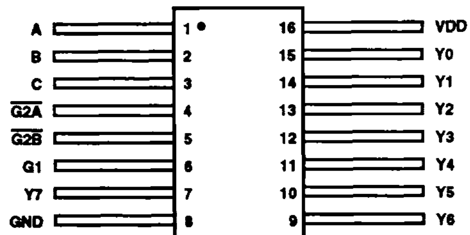
The HS-54C138RH has an on-chip enable gate. The active high (G1) and both active low ($\overline{G2A}$, $\overline{G2B}$) inputs are Anded together to provide a single enable input to the device. The use of both active high and active low inputs minimizes the need for external gates when expanding a system.

Pinouts

16 PIN DIP
CASE OUTLINE D2, CONFIGURATION 3
TOP VIEW



16 PIN FLATPACK
INTERNAL PACKAGE CODE HUV
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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Absolute Maximum Ratings

Supply Voltage ....+7.0V
I/O Voltage Applied.................... GND -.3V to VDD +.3V
Storage Temperature Range .... -65°C to +150°C
Junction Temperature.............................. +175°C
Lead Temperature (Soldering 10s).................... +300°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	74.5°C/W	12°C/W
Flatpack Package	63.3°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 670mW
Flatpack Package 700mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range.................... +4.75V to +5.25V
Operating Temperature Range................ -55°C to +125°C
Input Low Voltage .... 0V to 1.0V
Input High Voltage......................... VDD-1.0V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Leakage Current High	IIH	VDD = 5.25V, VIN = 0V, Pin Under Test = VDD	1, 2, 3	-55°C, +25°C, +125°C	-	1	µA
Input Leakage Current Low	IIL	VDD = 5.25V, VIN = 5.25V, Pin Under Test = 0V	1, 2, 3	-55°C, +25°C	-1	-	µA
High Level Output Voltage	VOH	VDD = 4.75V, IIN = -2mA	1, 2, 3	-55°C, +25°C, +125°C	4.25	-	V
Low Level Output Voltage	VOL	VDD = 5.25V, IIN = 2mA	1, 2, 3	-55°C, +25°C, +125°C	0.5	-	V
Static Current	SIDD	VDD = 5.25V, VIN = GND	1, 2, 3	-55°C, +25°C, +125°C	-	100	µA
Functional Tests	FT	VDD = 5.25V and 4.75V, VIH = VDD - 1.0V, VIL = 1.0V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTE: All devices are guaranteed at worst case limits and conditions.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
SELECT TO OUTPUT PROPAGATION DELAY TIME						
Low to high level input, High to low level output	TPHL11	9, 10, 11	-55°C, +25°C, +125°C	-	110	ns
Low to high level input, Low to high level output	TPLH11	9, 10, 11	-55°C, +25°C, +125°C	-	65	ns
High to low level input, Low to high level output	TPLH12	9, 10, 11	-55°C, +25°C, +125°C	-	75	ns
High to low level input, high to low level output	TPHL12	9, 10, 11	-55°C, +25°C, +125°C	-	90	ns
ENABLE TO OUTPUT PROPAGATION DELAY TIME						
Low to high level input, Low to high level output	TPLH21	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
Low to high level input, High to low level output	TPHL21	9, 10, 11	-55°C, +25°C, +125°C	-	105	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
High to low level input, Low to high level output	TPLH22	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
High to low level input, High to low level output	TPHL22	9, 10, 11	-55°C, +25°C, +125°C	-	105	ns

NOTE: Output timings are measured with a capacitive load, CL = 100pF, VIH = 3.75V, and VIL = 1.0V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	10	pF
Output Capcitance	COUT	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	10	pF

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

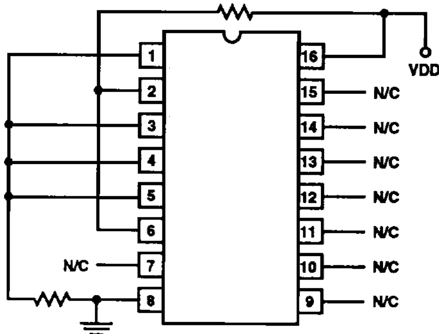
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current	SIDD	±30μA
Low Input Leakage Current	IIL	±100nA
High Input Leakage Current	IIH	±100nA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±400mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test	100%/5004	1, 7, 9
PDA	100%/5004	1, 7
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D Others	Samples/5004	1, 7
Group E Subgroup 2	Samples/5004	1, 7, 9

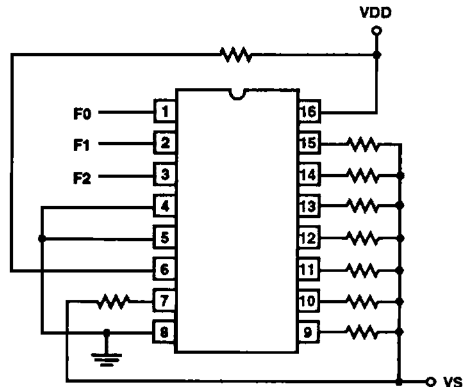
Burn-In Circuits



STATIC CONFIGURATIONS

NOTES:

Minimum Temperature = +125°C, VDD = 10V ± 5%
All Resistors 10KΩ, 1/4W

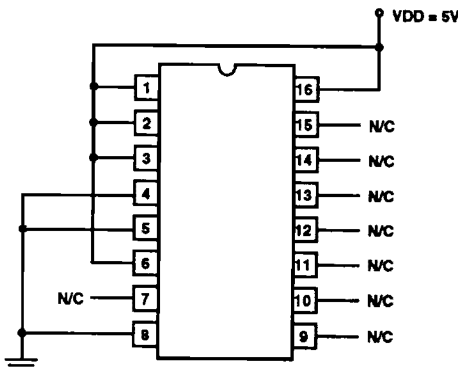


DYNAMIC CONFIGURATION

NOTES:

VDD = 10.0V ± 5%
VS = 5V ± 10%
T_A Min = +125°C
All resistors are 10KΩ ± 10%, 1/4W
F0 = 1MHz, 50% Duty Cycle
F1 = F0/2, F2 = F1/2

Irradiation Circuit



NOTES:

VDD = 5.0V ± 0.5V
Group E Testing Performed in Ceramic DIP
Group E Sample Size is 2 die/wafer

Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality, in a ceramic dip.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 105 Ras(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Bias circuit is shown to the left.
5. The sample devices shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-54C138RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latching up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained when special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad(Si). Transient radiation tests have shown the following results:

- Latch-up free to doses ≥ 1 x 10^{12} rads/sec.
- Upset (loss of stored data) ≥ 1 x 10^8 rads/sec.

Harris - Space Level Product Flow (Note 1)

SEM - Traceable to Diffusion - Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection - Method 2010, Condition A

Gamma Radiation Assurance Tests - Method 1019

Nondestructive Bond Pull - Method 2023

Customer Pre-Cap Visual Inspection (Notes 2)

Temperature Cycling - Method 1010, Condition C

Constant Acceleration - Method 2001, Condition E Min., Y1

Particle Impact Noise Detection - Method 2020, Condition A

Electrical Tests - Harris' Option

Serialization

X-Ray Inspection - Method 2012

Electrical Tests - Subgroup 1; Read and Record (T0)

Static Burn-In - Method 1015, Condition B, 72 Hours, +125°C Minimum

Electrical Tests - Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Dynamic Burn-In, Method 1015, Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests - Subgroup 1; Read and Record (T2)

Alternate Group A - Subgroups 1, 7, 9; Method 5005; Paragraph 3.5.1.1

Burn-In Delta Calculation (T0-T2)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Electrical Tests - Subgroup 3; Read and Record

Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Paragraph 3.5.1.1

Marking

Electrical Tests - Subgroup 2; Read and Record

Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Paragraph 3.5.1.1

Fine and Gross Leak Tests - Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection - Method 5005 (Notes 2)
End-Point Electrical Parameters: B5; Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11

Group D Inspection - Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: B5; Subgroups 1, 7, 9

External Visual Inspection - Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table I shall apply; unless otherwise specified.
2. These steps are optional, and should be listed on the purchase order if required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table O of Method 1015.
4. For Group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data

Metallization Topology

DIE DIMENSIONS:
76 x 63 x 14 ± 1mils

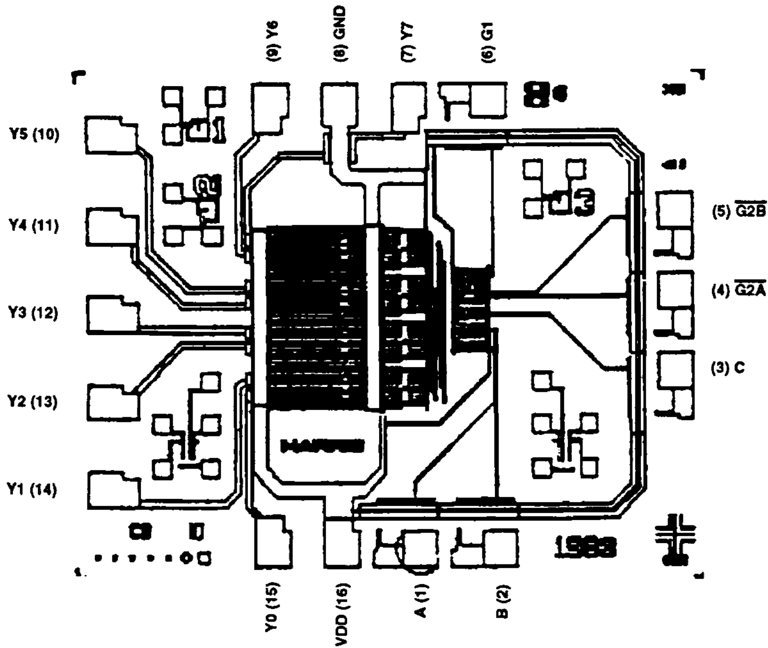
METALLIZATION:
Type: AlSi
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP- 460°C (Max)

Metallization Mask Layout

HS-54C138RH



Typical applications include systems which require multiple input/output ports and memories. When the HS-54C138RH is enabled one of the eight outputs will go low. This output can be used to select a particular device or a group of devices. The HS-54C138RH can also be cascaded to provide an enabling scheme for larger systems and allow one decoder to control eight other decoders as in Figure 1.

Figure 2 shows a configuration that can be used to enable multiple I/O ports or memory devices. Up to 24 memory devices or I/O ports can be controlled using this circuit.

For demultiplexer operation, one of the three enable inputs is used as the data input while the other two inputs are enable. The transmitted data is distributed to the proper output as determined by the 3-line select inputs. See Figure 3.

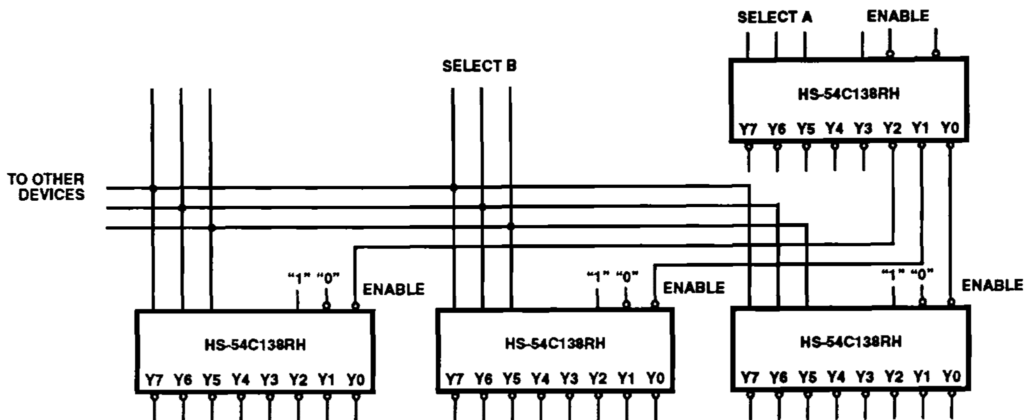


FIGURE 1

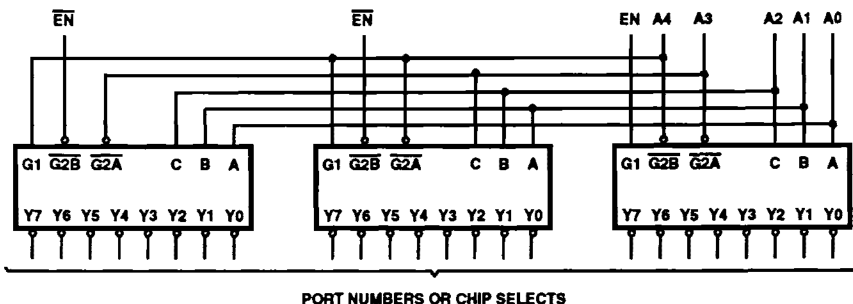


FIGURE 2

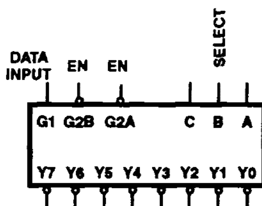


FIGURE 3

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μPROCESSOR PERIPHERALS