



Dual/Quad Gated Flip-Flops

General Description

The DM7511/8511 or the low-power versions DM75L11/85L11, are dual, gated, D-type flip-flops. Each flip-flop has its own clock, clear line, and two gated inputs. Both gate inputs must be low to enable data transfer to the output.

The DM7512/8512, and DM75L12/85L12 are dual, gated flip-flops which can operate in either a J-K mode, or as D-type flip-flops. They have a common clock and common, asynchronous clear, but have separate mode inputs such that one side can operate as J-K while the other side operates as a D-type flip-flop.

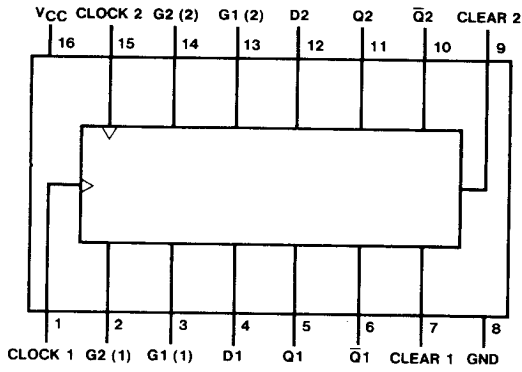
The DM7613/8613, and DM76L13/86L13 are quad, gated, D-type flip-flops with common clock, common clear, and gated input. When a high logic level is applied to the gated input, data entry to the flip-flop is inhibited.

Features

- Positive-edge triggered
- Do-nothing state
- Buffered inputs

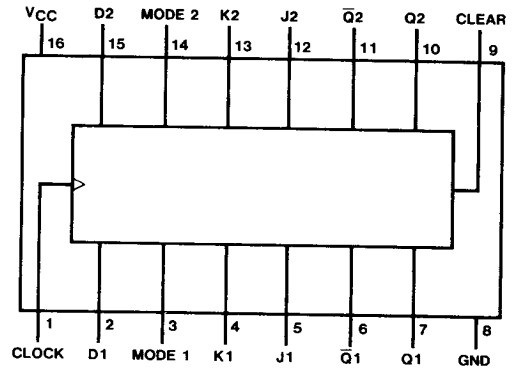
Type	Typical Toggle Rate	Typical Power Dissipation
DM7511/8511	45 MHz	210 mW
DM75L11/85L11	9 MHz	17.5 mW
DM7512/8512	28 MHz	220 mW
DM75L12/85L12	10 MHz	16.0 mW
DM7613/8613	30 MHz	290 mW
DM76L13/86L13	7 MHz	28.5 mW

Connection Diagrams



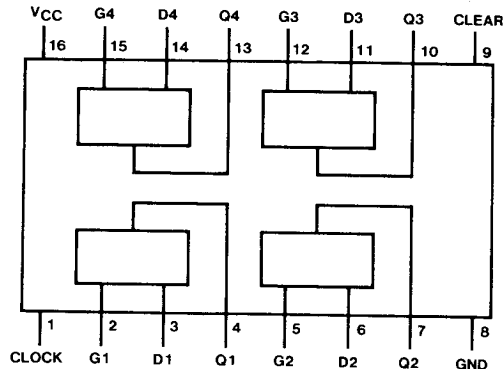
7511 (J,W)
75L11 (J,W)

8511 (N)
85L11 (N)



7512 (J,W)
75L12 (J,W)

8512 (N)
85L12 (N)



7613 (J,W)
76L13 (J,W)

8613 (N)
86L13 (N)



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter	Conditions	DM75-85			DM76-86			DM75L-85L11, 12			DM76L-86L13			Units
		11, 12			13			DM75L-85L11, 12			DM76L-86L13			
		Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	
V _{IH}	High Level Input Voltage	2			2			2					V	
V _{IL}	Low Level Input Voltage												V	
V _I	Input Clamp Voltage			0.8						0.8			V	
I _{OH}	High Level Output Current			-1.5						-1.5			N/A	
V _{OH}	High Level Output Voltage			-800						-800			μA	
I _{OL}	Low Level Output Current	2.4			2.4			2.4					V	
V _{OL}	Low Level Output Voltage			16				16		16			mA	
I _I	Input Current at Maximum Input Voltage			16				16		16			mA	
I _{IH}	High Level Input Current			0.4				0.4		0.4			V	
I _{IL}	Low Level Input Current			0.4				0.4		0.4			V	
I _{OS}	Short Circuit Output Current			-18				-18		-18			mA	
I _{CC}	Supply Current			42				42		42			mA	

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
 Note 2: Not more than one output should be shorted at a time.
 Note 3: Supply current is measured with clear clock at 3 V, all other inputs at 0 V.

Switching Characteristics $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

Parameter	From	To	Conditions	DM75/85			DM75/85			DM76/86			Units	
				11, L11	12, L12	13, L13	Min	Typ	Max	Min	Typ	Max		Min
t_{MAX}														
Maximum Clock Frequency														
t_{PLH}														
Propagation Delay Time, Low-to-High Level Output	Clock	Q	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$ (Standard)											
t_{PHL}														
Propagation Delay Time, High-to-Low Level Output	Clock	Q	$C_L = 50\text{ pF}$, $R_L = 4\text{ k}\Omega$ (Low Power)											
t_{PLH}														
Propagation Delay Time, Low-to-High Level Output	Clear	\bar{Q}												
t_{PHL}														
Propagation Delay Time, High-to-Low Output	Clear	Q												
$t_{W(CLOCK)}$														
Width of Clock Pulse														
$t_{W(CLEAR)}$														
Width of Clear Pulse														
t_{SETUP}	Setup Time	J, D Inputs												
		Mode Inputs												
		K Inputs												
		G1 or G2 Inputs												
t_{HOLD}	Hold Time	All												



Truth Tables

11, L11

D	G1	G2	CLR	Q _{n+1}	Q̄ _{n+1}
L	L	L	L	L	H
H	L	L	L	H	L
X	H	X	L	Q _n	Q̄ _n
X	X	H	L	Q _n	Q̄ _n
X	X	X	H	L	H*

12, L12

J	K	M	Clear	Q _{n+1}
L	L	H	L	Q _n
H	L	H	L	H
L	H	H	L	L
H	H	H	L	Q̄ _n
X	X	L	L	D
X	X	X	H	L*

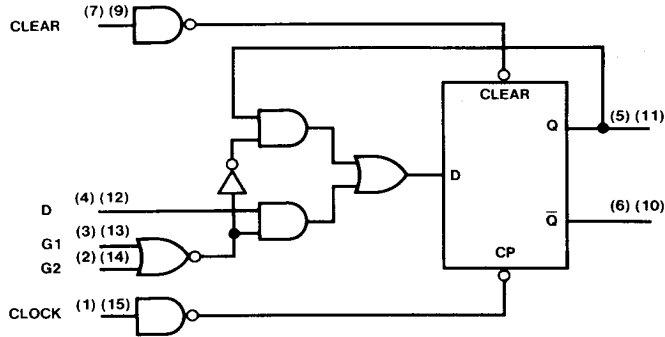
13, L13

D	G	CLR	Q _{n+1}
H	L	L	H
L	L	L	L
X	H	L	Q _n
X	X	H	L*

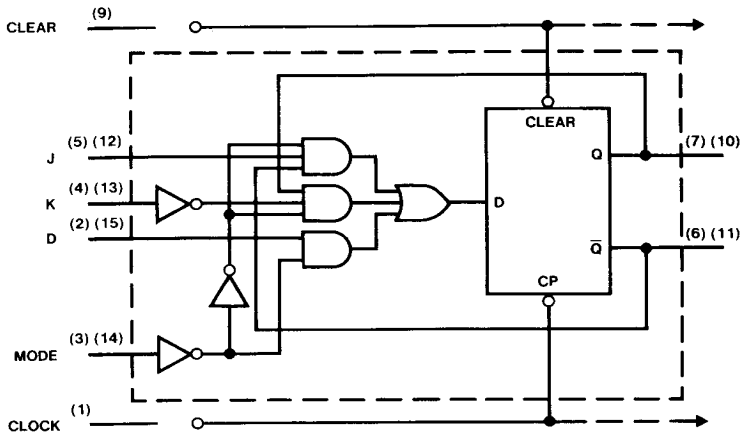
* Asynchronous Transition
X = Don't Care

Logic Diagrams

11, L11



12, L12





Logic Diagrams (Continued)

13, L13

