REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18															

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-01-26

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, ECL, 4-STAGE COUNTER/SHIFT REGISTER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-92306
A	67268	

SHEET 1 OF 18

1

DESC FORM 193
JUL 91

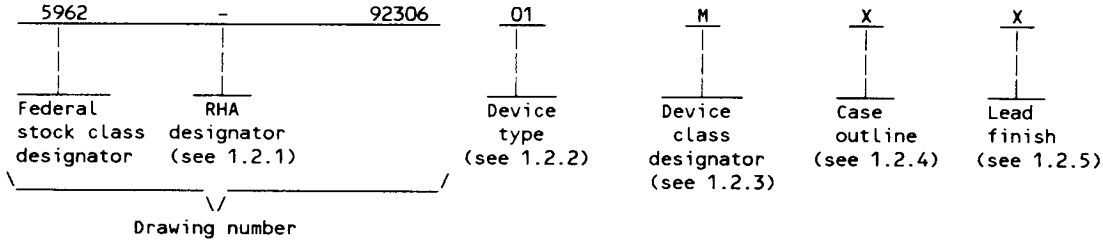
5962-E102-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	100336	4-stage counter/shift register

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP5-T24 or CDIP6-T24	24	dual-in-line
Y	See figure 1	24	quad flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Negative supply voltage range (V_{EE})	-7.0 V dc to +0.5 V dc
DC input voltage range (V_{IN})	V_{EE} to +0.5 V
Maximum dc output current (I_{OUT})	-50 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D)	1280 mW
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	28°C/W

1.4 Recommended operating conditions.

Negative supply voltage range (V_{EE})	-5.7 V dc minimum to -4.2 V dc maximum
High level input voltage range (V_{IH})	-1.165 V dc minimum to -0.870 V dc maximum
Low level input voltage range (V_{IL})	-1.830 V dc minimum to -1.475 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C
Minimum setup time, D_3 to CP (t_s)	1.4 ns
Minimum hold time, D_3 to CP (t_h)	0.9 ns
Minimum setup time, P_n to CP (t_s)	1.7 ns
Minimum hold time, P_n to CP (t_h)	1.0 ns
Minimum setup time, $D_{Q/\overline{CET}}$ to CP (t_s)	1.8 ns
Minimum hold time, $D_{Q/\overline{CET}}$ to CP (t_h)	0.7 ns
Minimum setup time, $\overline{CEP}$ to CP (t_s)	1.8 ns
Minimum hold time, $\overline{CEP}$ to CP (t_h)	0.6 ns
Minimum setup time, S_n to CP (t_s)	3.3 ns
Minimum hold time, S_n to CP (t_h)	0.0 ns
Minimum setup time, $\overline{MR}$ to CP (t_s)	2.6 ns
Minimum pulse width, CP (t_w)	1.6 ns
Minimum pulse width, $\overline{MR}$ (t_w)	2.0 ns
Maximum clock frequency, CP (f_{MAX})	325 MHz

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Function select and truth tables. The function select and truth tables shall be as specified on figure 3.

3.2.4 Test circuits and switching waveforms. The test circuits and switching waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 33 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $-5.7\ V \le V_{EE} \le -4.2\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
High level output voltage	V_{OH}	$V_{IH} = -0.870\ V$, $V_{EE} = -4.2\ V$, $V_{IL} = -1.830\ V$	1, 2	-1.025	-0.870	V
			3	-1.085	-0.870	
Low level output voltage	V_{OL}		1, 2	-1.830	-1.620	
			3	-1.830	-1.555	
High level threshold output voltage	V_{OHC}	$V_{IH} = -1.165\ V$, $V_{EE} = -4.2\ V$, $V_{IL} = -1.475\ V$	1, 2	-1.035		
			3	-1.085		
Low level threshold output voltage	V_{OLC}		1, 2		-1.610	
			3		-1.555	
High level input current	I_{IH}	$V_{EE} = -5.7\ V$, $V_{IN} = -0.870\ V$	1, 2		240	µA
			3		340	
Low level input current	I_{IL}	$V_{EE} = -4.2\ V$, $V_{IN} = -1.830\ V$	1, 2, 3	0.5		
Power supply drain current	I_{EE}	$V_{EE} = -5.7\ V, -4.2\ V$ Inputs open	1, 2, 3	-195	-70	mA
		$V_{EE} = -4.8\ V, -4.2\ V$ Inputs open	1, 2, 3	-185	-70	
Functional tests		$V_{EE} = -5.7\ V, -4.2\ V$ $V_{IH} = -1.018\ V$, $V_{IL} = -1.652\ V$ See 4.4.1b	7, 8			
Propagation delay time, CP to Q_n, $\overline{Q}_n$	t_{PLH1}, t_{PHL1}	See figure 4	9	0.4	2.2	ns
			10	0.4	2.5	
			11	0.4	2.3	
Propagation delay time, CP to $\overline{TC}$ (shift mode)	t_{PLH2}, t_{PHL2}		9	1.7	3.8	
			10	1.7	4.2	
			11	1.3	3.9	
Propagation delay time, CP to $\overline{TC}$ (count mode)	t_{PLH3}, t_{PHL3}		9	1.5	4.6	
			10	1.6	5.2	
			11	1.2	4.6	

See footnotes at end of table.

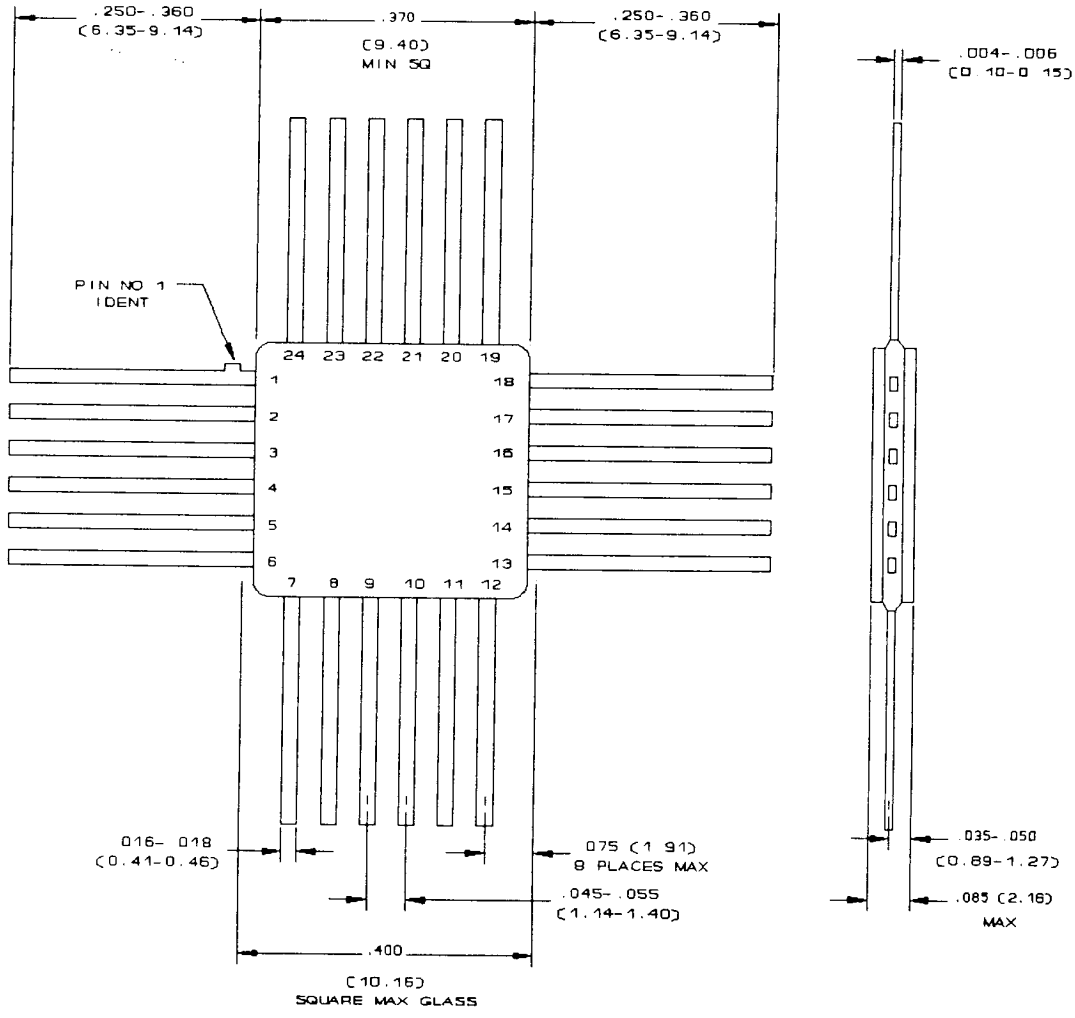
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $-5.7\ V \le V_{EE} \le -4.2\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay time, MR to Q_n, $\overline{Q}_n$	t_{PLH4}, t_{PHL4}	See figure 4	9	0.8	2.8	ns
			10	0.9	3.2	
			11	0.6	2.9	
Propagation delay time, MR to $\overline{TC}$ (count mode)	t_{PLH5}, t_{PHL5}		9	2.7	5.2	
			10	2.9	5.9	
			11	2.3	5.2	
Propagation delay time, MR to $\overline{TC}$ (shift mode)	t_{PHL6}		9	2.2	4.1	
			10	2.4	4.7	
			11	2.1	4.3	
Propagation delay time, D_0/CET to $\overline{TC}$	t_{PLH7}, t_{PHL7}		9	1.0	3.2	
			10	1.3	4.1	
			11	0.7	3.2	
Propagation delay time, S_n to $\overline{TC}$	t_{PLH8}, t_{PHL8}		9	1.5	4.2	
			10	1.7	4.9	
			11	1.3	4.1	
Transition time, 2/ Q_n, $\overline{Q}_n$	t_{TLH}, t_{THL}		9	0.2	1.8	
			10	0.2	2.0	
			11	0.2	1.9	

1/ Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals shall be terminated through 50Ω to -2 V. Input terminals not designated shall be high logic level or low logic level.

2/ This parameter is provided as design information only (not tested but guaranteed).

Case Y



NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Metric equivalents are in parentheses.

FIGURE 1. Case outline.

Device type	01	
Case outlines	X	Y
Terminal number	Terminal symbol	
1	$\overline{TC}$	S_2
2	Q_0	$\overline{CEP}$
3	$\overline{Q}_0$	$D_0/\overline{CET}$
4	$\overline{Q}_1$	$\overline{TC}$
5	Q_1	Q_0
6	V_{CC}	$\overline{Q}_0$
7	V_{CCA}	$\overline{Q}_1$
8	Q_2	Q_1
9	$\overline{Q}_2$	V_{CC}
10	$\overline{Q}_3$	V_{CCA}
11	Q_3	Q_2
12	D_3	$\overline{Q}_2$
13	P_3	$\overline{Q}_3$
14	P_2	Q_3
15	P_1	D_3
16	P_0	P_3
17	CP	P_2
18	V_{EE}	P_1
19	MR	P_0
20	S_0	CP
21	S_1	V_{EE}
22	S_2	MR
23	$\overline{CEP}$	S_0
24	$D_0/\overline{CET}$	S_1

FIGURE 2. Terminal connections.

Function select table

S_2	S_1	S_0	Function
L	L	L	Parallel load
L	L	H	Complement
L	H	L	Shift left
L	H	H	Shift right
H	L	L	Count down
H	L	H	Clear
H	H	L	Count up
H	H	H	Hold

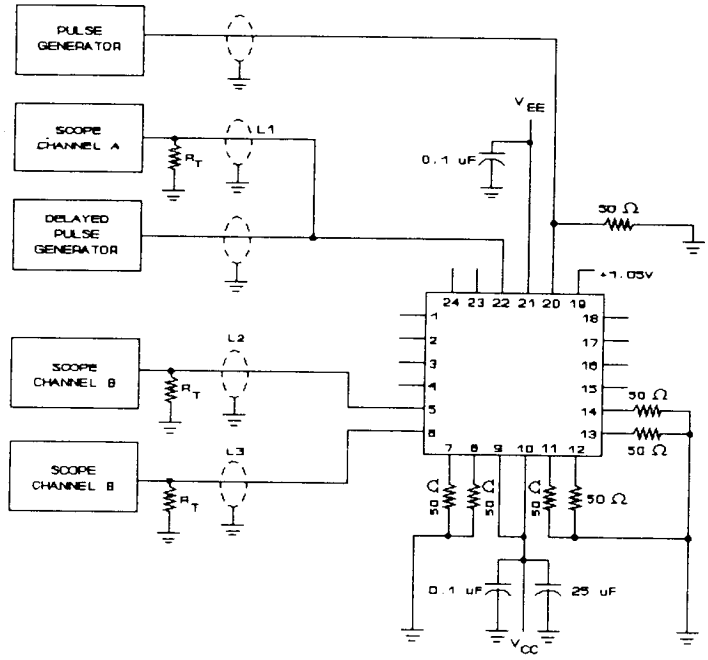
Truth table

Inputs								Outputs					
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	Mode
L	L	L	L	X	X	X	↑	P_3	P_2	P_1	P_0	L	Preset (parallel load)
L	L	L	H	X	X	X	↑	$\overline{Q}_3$	$\overline{Q}_2$	$\overline{Q}_1$	$\overline{Q}_0$	L	Invert
L	L	H	L	X	X	X	↑	D_3	Q_3	Q_2	Q_1	D_3	Shift to LSB (shift left)
L	L	H	H	X	X	X	↑	Q_2	Q_1	Q_0	D_0	Q_3 1/	Shift to MSB (shift right)
L	H	L	L	L	L	X	↑	(Q_{0-3}) minus 1				2/	Count down
L	H	L	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	2/	Count down with $\overline{CEP}$ not active
L	H	L	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count down with $\overline{CET}$ not active
L	H	L	H	X	X	X	↑	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↑	(Q_{0-3}) plus 1				3/	Count up
L	H	H	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	3/	Count up with $\overline{CEP}$ not active
L	H	H	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count up with $\overline{CET}$ not active
L	H	H	H	X	X	X	X	Q_3	Q_2	Q_1	Q_0	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

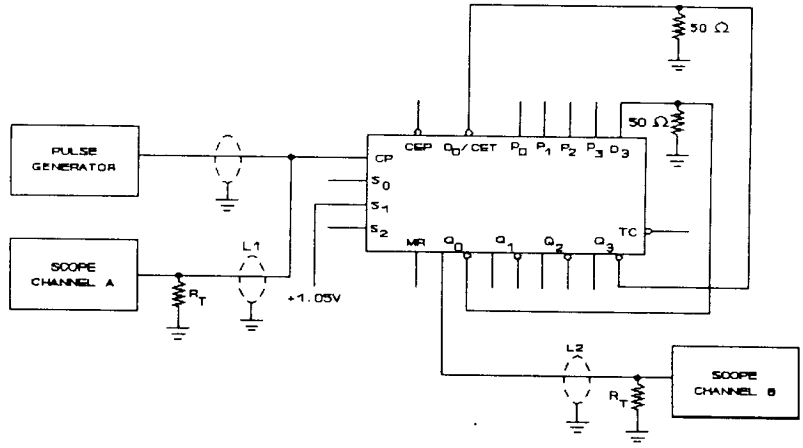
1/ Before the clock, $\overline{TC}$ is Q_3. After the clock, $\overline{TC}$ is Q_2.
2/ L if Q_0 to Q_3 = LLLL. H if Q_0 to Q_3 ≠ LLLL.
3/ L if Q_0 to Q_3 = HHHH. H if Q_0 to Q_3 ≠ HHHH.
H = High level voltage.
L = Low level voltage.
X = Irrelevant.
↑ = Low-to-high transition.
Q_0 = LSB.

FIGURE 3. Function select and truth tables.

AC test circuit



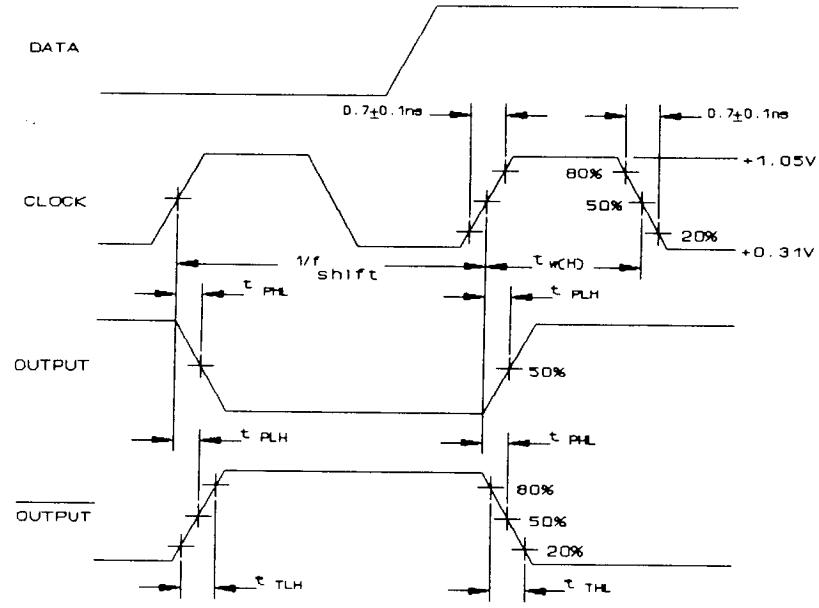
Shift frequency test circuit (shift left)



NOTES:
1. $V_{CC} = V_{CCA} = +2.0$ V, $V_{EE} = -2.5$ V.
2. L1, L2, and L3 = equal length 50Ω impedance lines.
3. $R_T = 50\Omega$ terminator internal to scope.
4. Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
5. All unused outputs are loaded with 50Ω to GND.
6. C_L = fixture and stray capacitance ≤ 3 pF.
7. Pin numbers shown are for case outline Y; for case outline X, see figure 2.
8. For shift right mode, $S_0 = +1.05$ V.

FIGURE 4. Test circuits and switching waveforms.

Propagation delay (clock) and transition times



Propagation delay (reset)

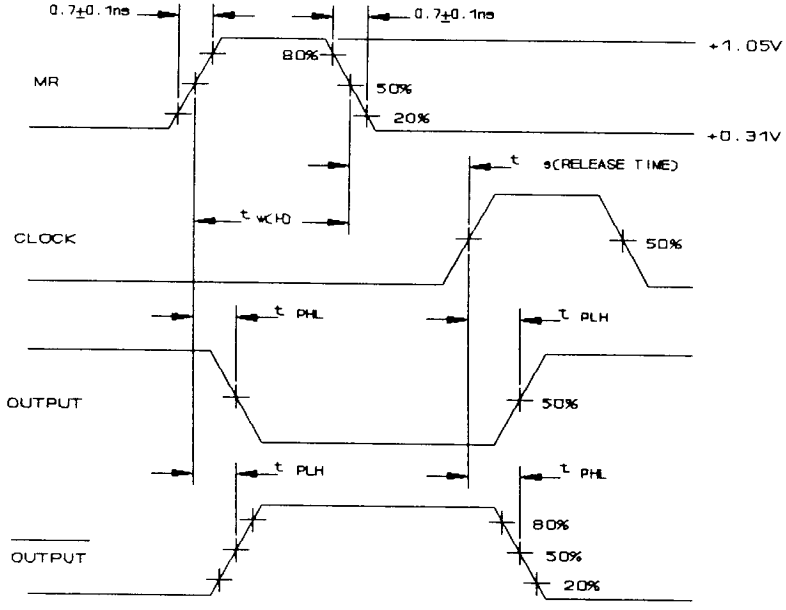
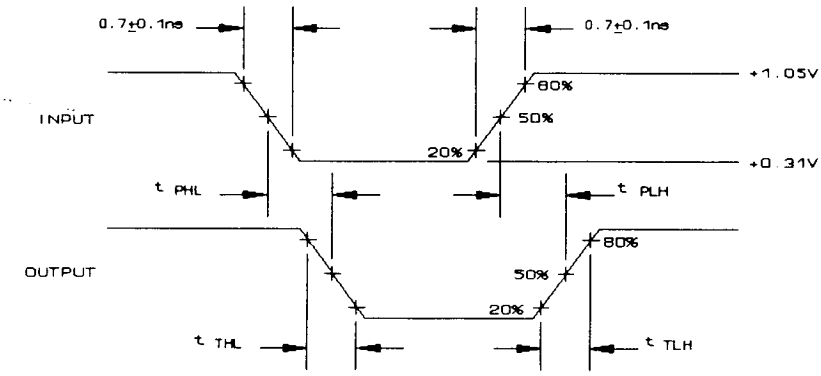


FIGURE 4. Test circuits and switching waveforms - Continued.

Propagation delay (serial data, selects)



Setup and hold times

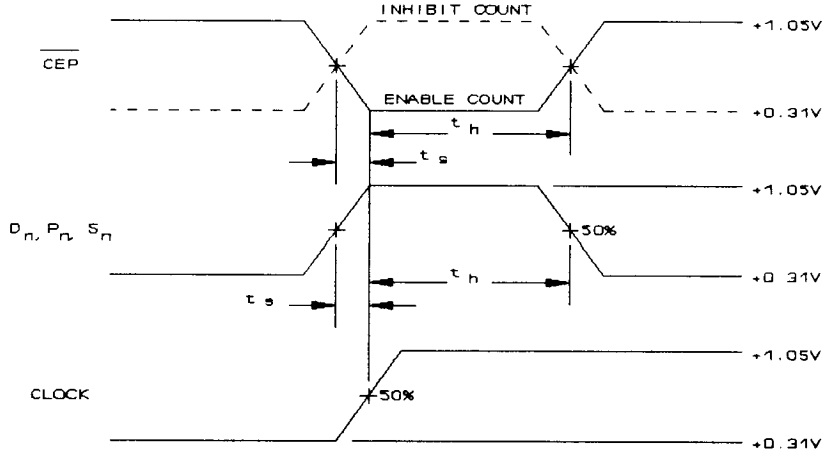
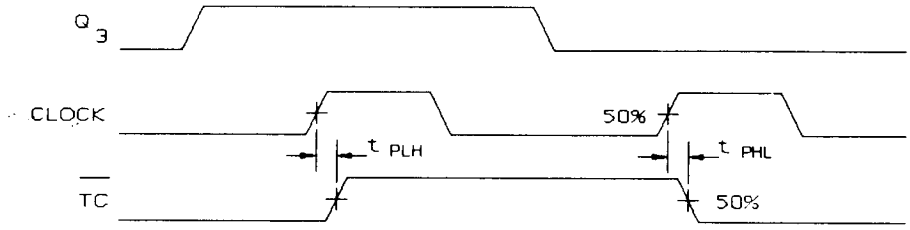
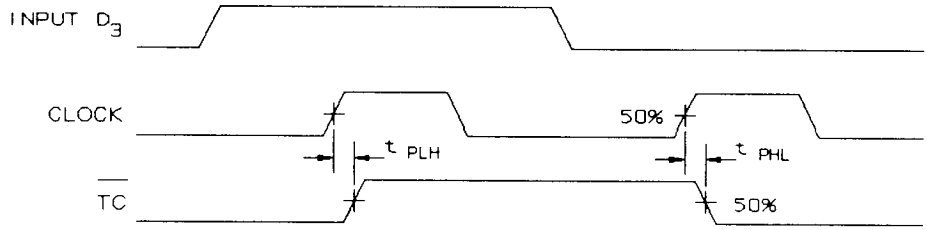


FIGURE 4. Test circuits and switching waveforms - Continued.

Propagation delay, clock to terminal count (shift right mode)



Propagation delay, clock to terminal count (shift left mode)



Propagation delay, clock to terminal count (count up and count down modes)

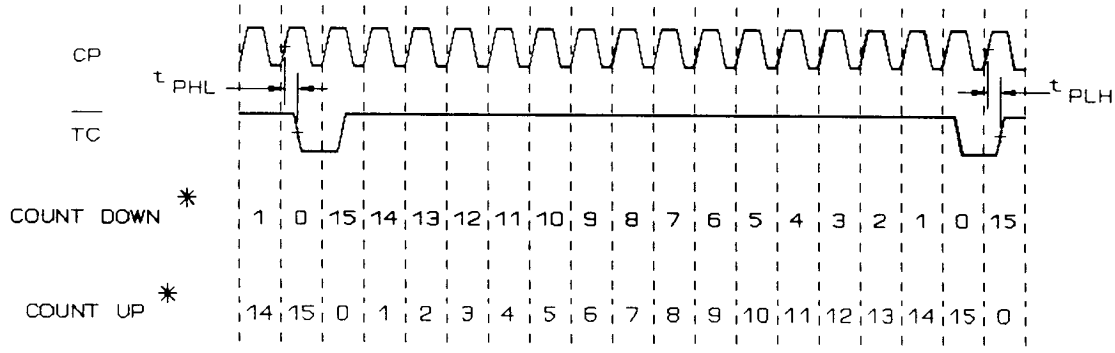
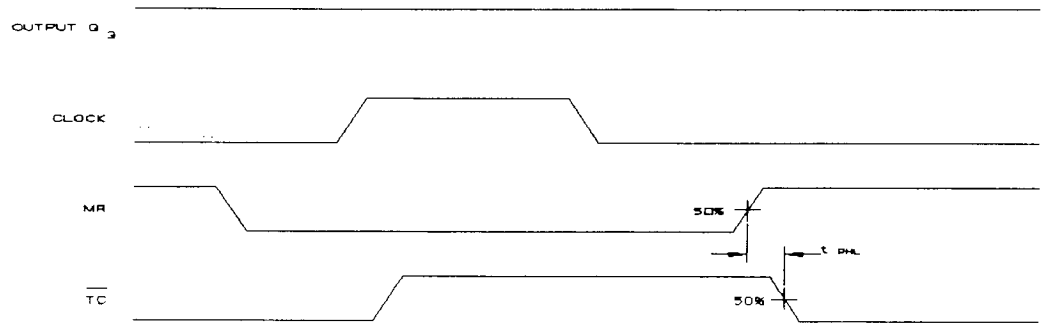
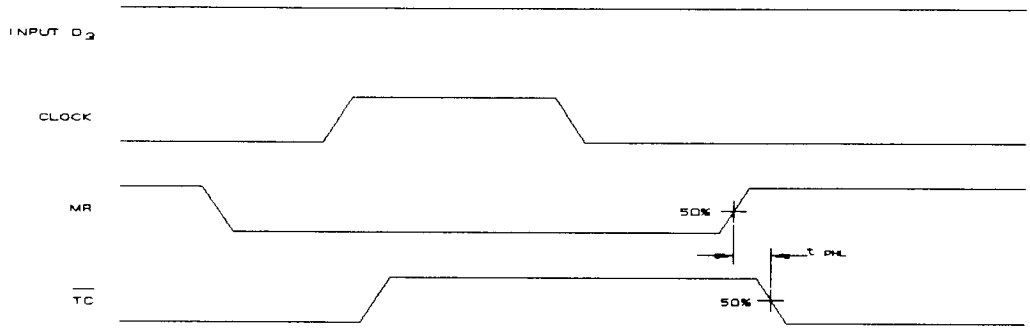


FIGURE 4. Test circuits and switching waveforms - Continued.

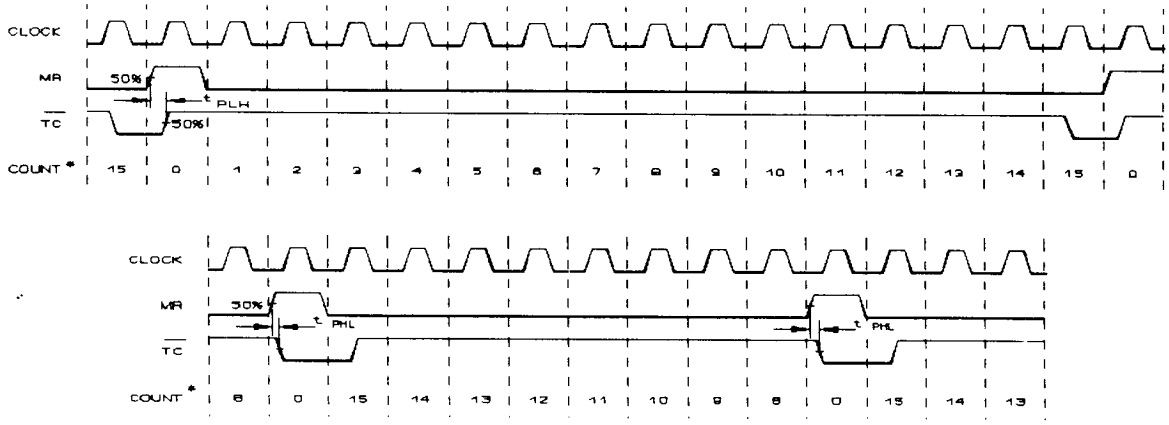
Propagation delay, master reset to terminal count (shift right mode)



Propagation delay, master reset to terminal count (shift left mode)



Propagation delay, master reset to terminal count (count up and count down modes)



NOTE:
* Decimal representation of binary outputs.

FIGURE 4. Test circuits and switching waveforms - Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1	1	1
Final electrical parameters (see 4.2)	1,2,3,7, 8,9 1/	1,2,3,7, 8,9 1/	1,2,3,7, 8,9,10,11 2/	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,2,3,7, 8,9,10,11		
Group C end-point electrical parameters (see 4.4)	1,2,3, 7,8	1,2,3, 7,8		1,2,3, 7,8	1,2,3, 7,8
Group D end-point electrical parameters (see 4.4)	1,2,3, 7,8	1,2,3, 7,8	1,2,3, 7,8	1,2,3, 7,8	1,2,3, 7,8
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.