FAIRCHILD SEMICONDUCTOR®

February 1994
Revised March 2005

74LCX245
Low Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

The LCX245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V and 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The T/$\overline{R}$ input determines the direction of data flow through the device. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state.

The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V to 3.6V V_{CC} specifications provided
- 7.0 ns t_{PD} max (V_{CC} = 3.3V), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Leadless DQFN Pb-Free package

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX245WM (Note 2)	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX245WMX_NL (Note 4)	M20B	Pb-Free 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX245SJ (Note 2)	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX245BQX (Note 3)	MLP020B	Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74LCX245MSA (Note 2)	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCX245MTC (Note 2)	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LCX245MTCX_NL (Note 4)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Pb-Free package per JEDEC J-STD-020B.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 3: DQFN package available in Tape and Reel only.

Note 4: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

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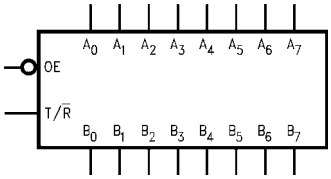
Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

Truth Table

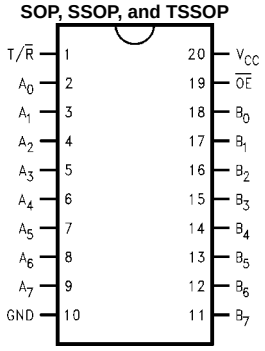
Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B_0 – B_7 Data to Bus A_0 – A_7
L	H	Bus A_0 – A_7 Data to Bus B_0 – B_7
H	X	HIGH Z State on A_0 – A_7, B_0 – B_7 (Note 5)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

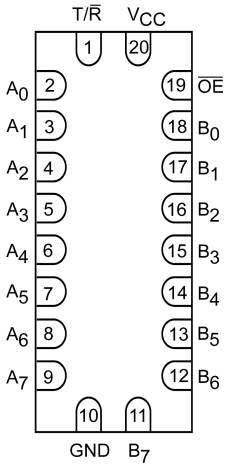
Note 5: Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Connection Diagrams

Pin Assignments for SOIC, SOP, SSOP, and TSSOP

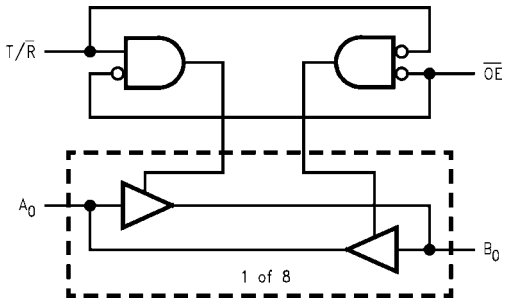


Pin Assignment for DQFN



(Top Through View)

Logic Diagram



Absolute Maximum Ratings(Note 6)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0 −0.5 to V_{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 7)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 8)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V to 3.6V		±24	mA
		V_{CC} = 2.7V to 3.0V		±12	
		V_{CC} = 2.3V to 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 6: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 7: I_O Absolute Maximum Rating must be observed.

Note 8: Unused inputs or I/O pins must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 to 2.7	1.7		V
			2.7 to 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 to 2.7		0.7	V
			2.7 to 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.3 to 3.6	V_{CC} − 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.3 to 3.6		0.2	V
		I_{OL} = 8mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 to 3.6		±5.0	μA
I_{OZ}	3-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.3 to 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 to 3.6		10	μA
		$3.6V \le V_I$, $V_O \le 5.5V$ (Note 9)	2.3 to 3.6		±10	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 to 3.6		500	μA

Note 9: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{PLH}	A_n to B_n or B_n to A_n	1.5	7.0	1.5	8.0	1.5	8.4	
t_{PZL}	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_{PZH}		1.5	8.5	1.5	9.5	1.5	10.5	
t_{PLZ}	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t_{PHZ}		1.5	7.5	1.5	8.5	1.5	9.0	
t_{OSHL}	Output to Output Skew		1.0					ns
t_{OSLH}	(Note 10)		1.0					

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7.0	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8.0	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	25.0	pF

AC LOADING and WAVEFORMS Generic for LCX Family

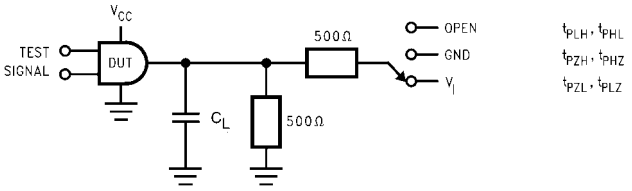
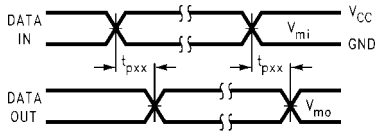
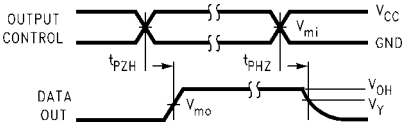


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

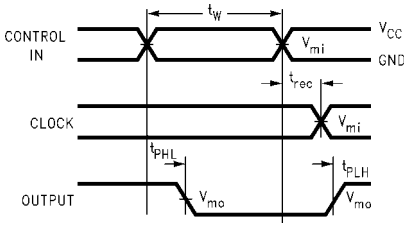
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3V ± 0.3V V_{CC} x 2 at V_{CC} = 2.5V ± 0.2V
t_{PZH}, t_{PHZ}	GND



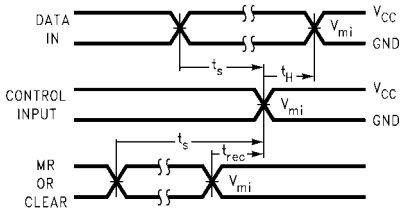
Waveform for Inverting and Non-Inverting Functions



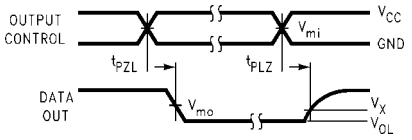
3-STATE Output High Enable and Disable Times for Logic



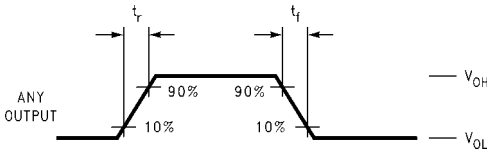
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

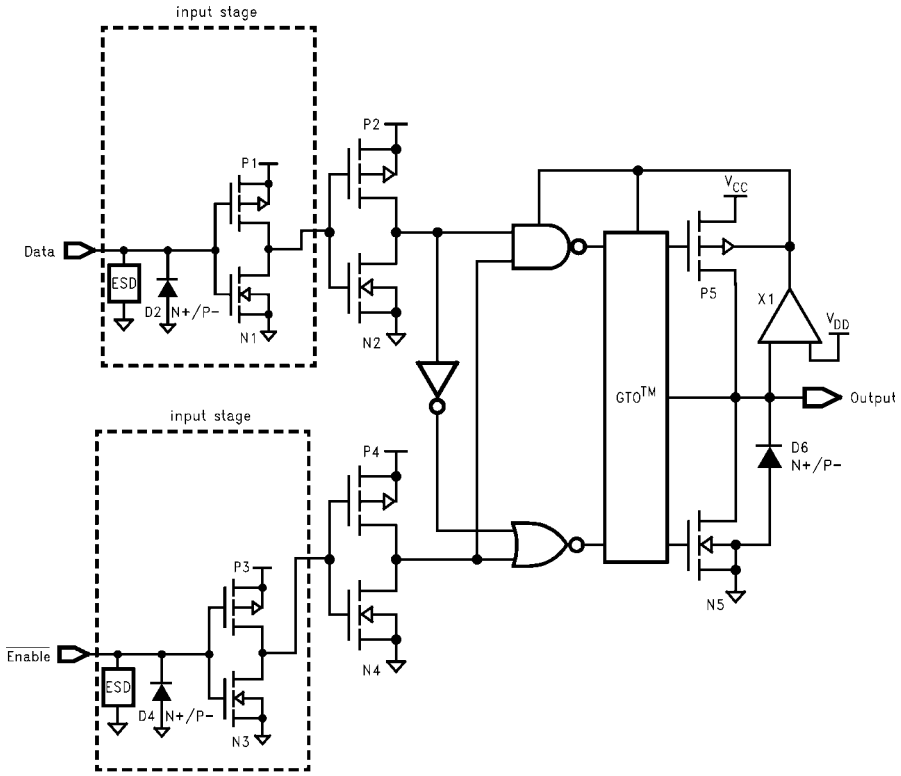


t_{rise} and t_{fall}

FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t_r = t_f = 3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.7V**	**2.5V ± 0.2V**
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCX Family

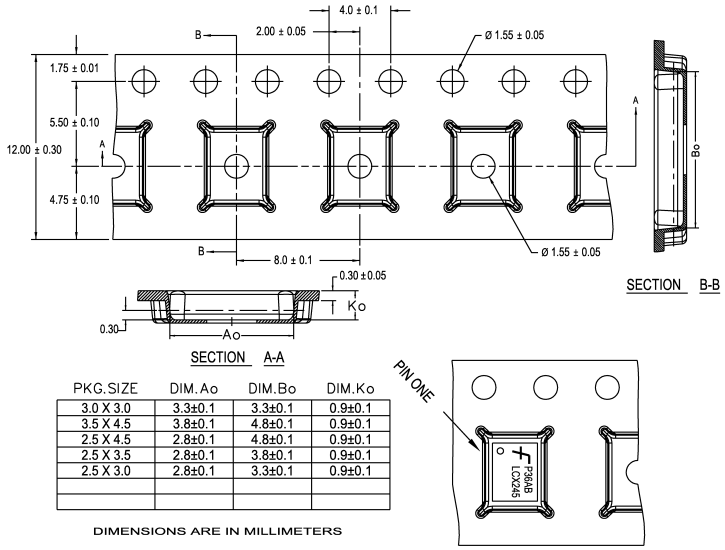


Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

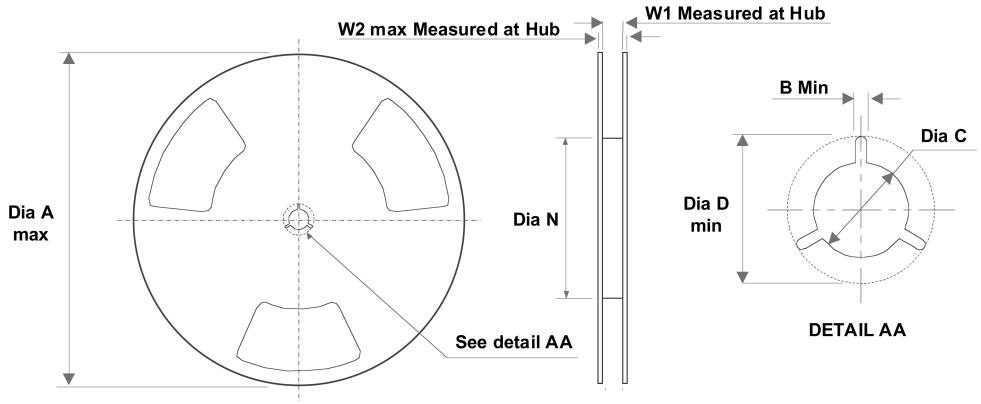


PKG.SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.0 X 3.0	3.3±0.1	3.3±0.1	0.9±0.1
3.5 X 4.5	3.8±0.1	4.8±0.1	0.9±0.1
2.5 X 4.5	2.8±0.1	4.8±0.1	0.9±0.1
2.5 X 3.5	2.8±0.1	3.8±0.1	0.9±0.1
2.5 X 3.0	2.8±0.1	3.3±0.1	0.9±0.1

DIMENSIONS ARE IN MILLIMETERS

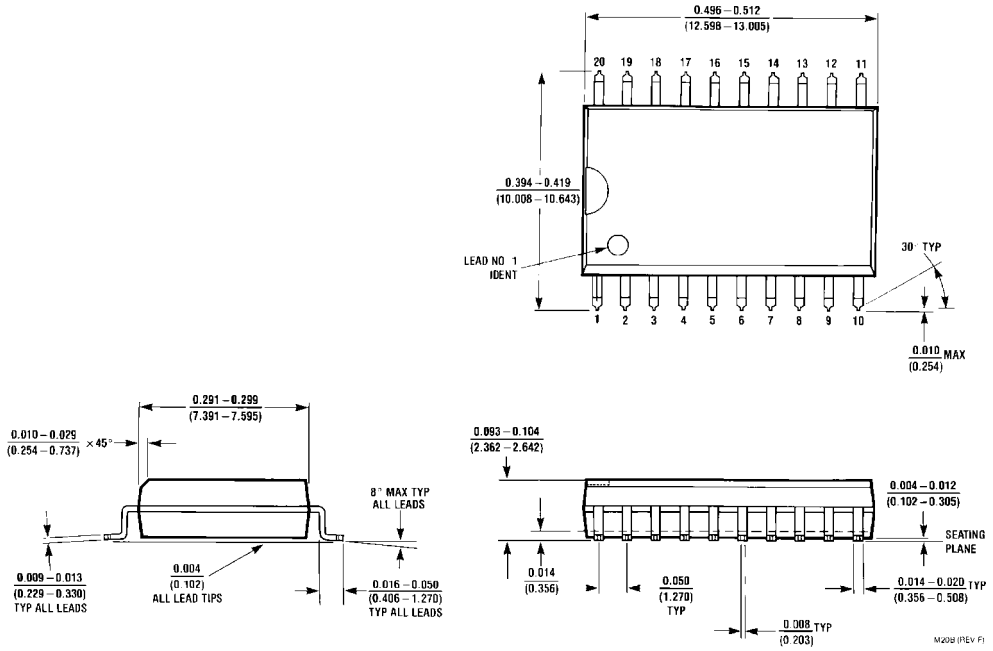
FSC MLP/DQFN CARRIER TAPE SPECIFICATIONS

REEL DIMENSIONS inches (millimeters)



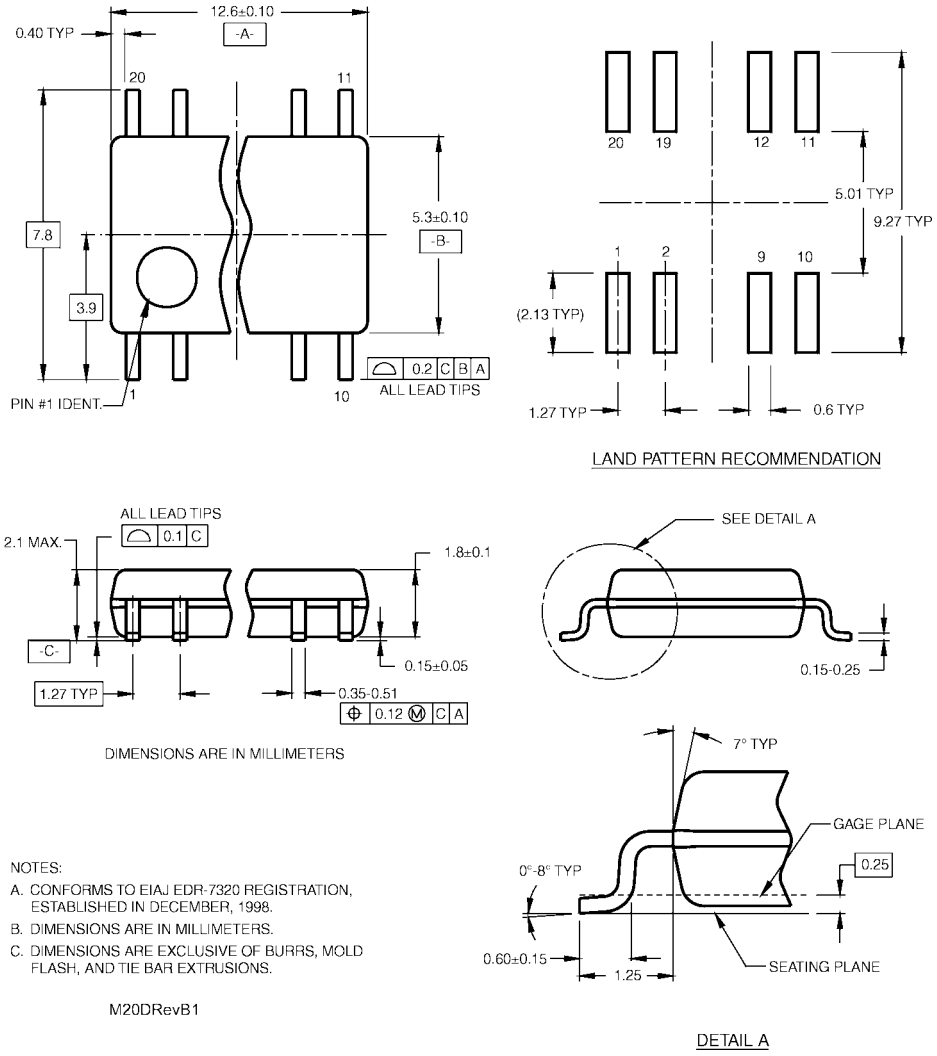
Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

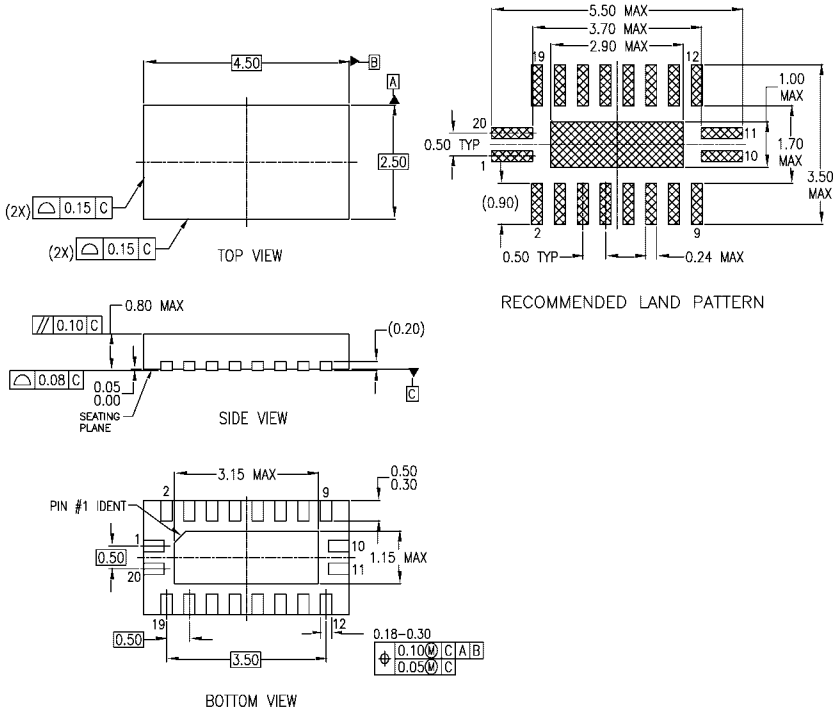
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



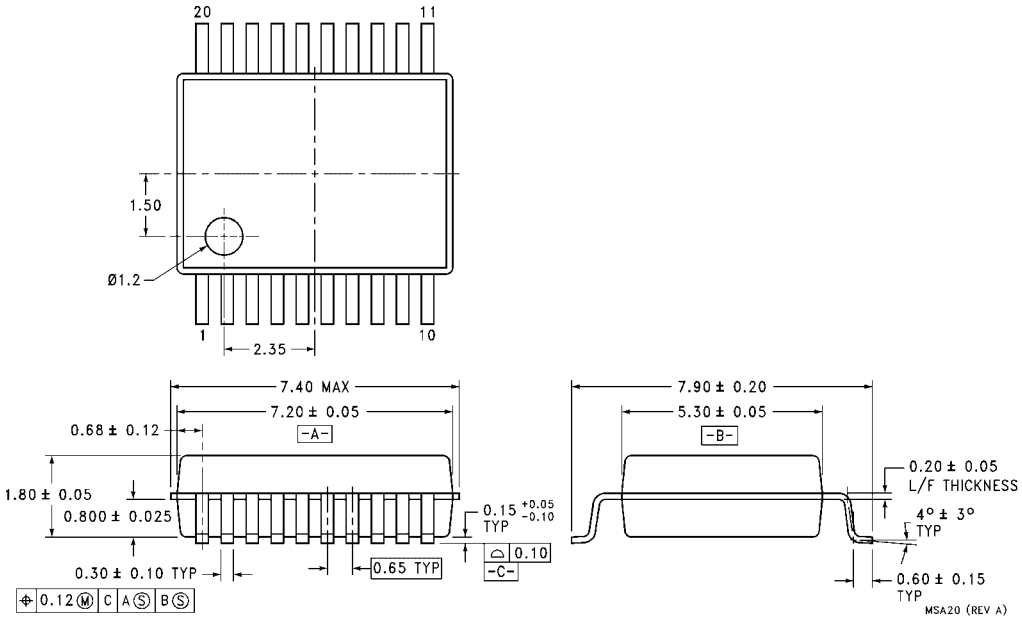
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AC
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP020BrevA

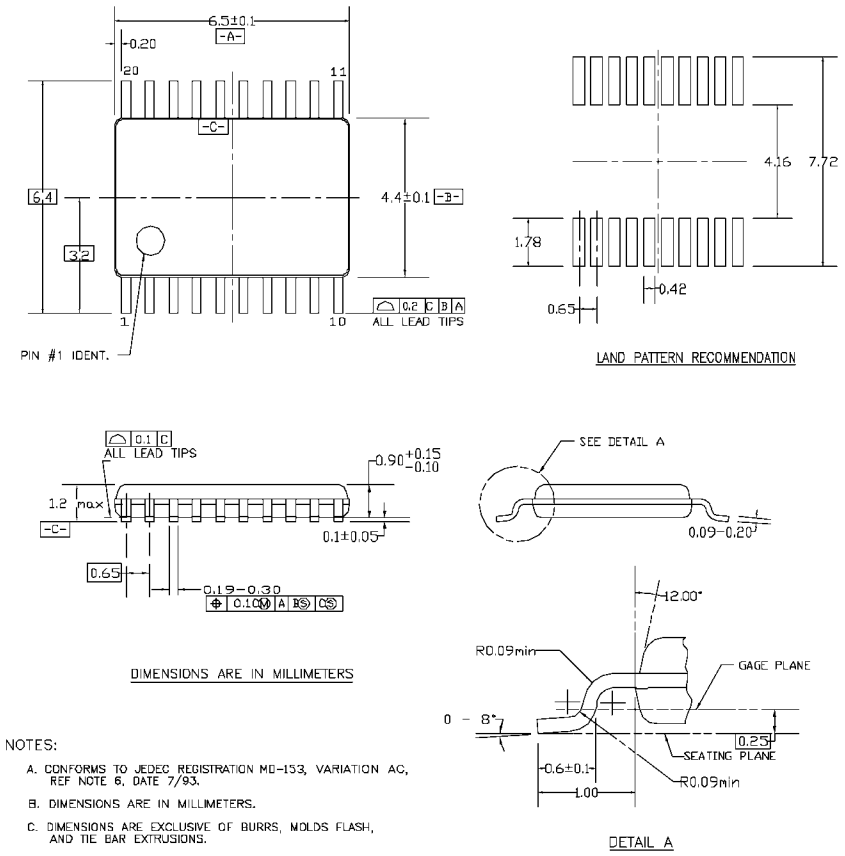
Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
Package Number MLP020B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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74LCX245

Low Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

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General description

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Features

- 5V tolerant inputs and outputs
- 2.3V to 3.6V V_{CC} specifications provided
- 7.0 ns t_{PD} max (V_{CC} = 3.3V), 10 µA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:

  Human body model > 2000V

Machine model > 200V

- Leadless DQFN Pb-Free package

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Product status/pricing/packaging BUY

Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
74LCX245BQX	Full Production	Full Production	$0.398	DQFN	20	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245MSA	Full Production	Full Production	$0.55	SSOP	20	RAIL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245MSAX	Full Production	Full Production	$0.451	SSOP	20	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245MSAX_NL	Full Production	Full Production	N/A	SSOP	20	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245MTC	Full Production	Full Production	$0.194	TSSOP	20	RAIL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245MTCX	Full Production	Full Production	$0.194	TSSOP	20	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245MTCX_NL	Full Production	Full Production	N/A	TSSOP	20	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245

74LCX245SJ	Full Production	Full Production	$0.265	SOP	20	RAIL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245SJX	Full Production	Full Production	$0.265	SOP	20	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245SJX_NL	Full Production	Full Production	N/A	SOP	20	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245WM	Full Production	Full Production	$0.233	SOIC-Wide	20	RAIL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245WMX	Full Production	Full Production	$0.233	SOIC-Wide	20	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245
74LCX245WMX_NL	Full Production	Full Production	N/A	SOIC-Wide	20	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: LCX245

* Fairchild 1,000 piece Budgetary Pricing
** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a Fairchild distributor to obtain samples

Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product 74LCX245 is available. Click here for more information .

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Models

Package & leads	Condition	Temperature range	Vcc range	Software version	Revision date
HSPICE					

DQFN-20	Slow	-40°C to 85°C	2.3V to 3.6V	2001.4	Oct 6, 2003
	Fast	-40°C to 85°C	2.3V to 3.6V	2001.4	Oct 6, 2003
	Typical	-40°C to 85°C	2.3V to 3.6V	2001.4	Oct 6, 2003
SOIC-Wide-20	Fast	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
	Typical	-40°C to 85°C	2V to 3.6V	98.4	Mar 10, 2003
	Slow	-40°C to 85°C	2V to 3.6V	98.4	Mar 10, 2003
SOP-20	Slow	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
	Fast	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
	Typical	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
SSOP-20	Slow	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
	Fast	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
	Typical	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
TSSOP-20	Typical	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
	Fast	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
	Slow	-40°C to 85°C	2V to 3.6V	2001.4	Mar 10, 2003
IBIS					
SOIC-Wide-20	All	-40°C to 85°C	3.15V to 3.45V	3.2	Dec 10, 2000
TSSOP-20	All	-40°C to 85°C	3V to 3.6V	2.1	Jan 27, 1998

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Application notes

AN-5054: Low Noise Leadless Packages Advance Portable Designs (51 K)
Jul 27, 2007
MS-520: Logic Design Considerations (216 K) Jul 27, 2007

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Qualification Support

Click on a product for detailed qualification data

Product
74LCX245BQX
74LCX245MSA

74LCX245MSAX
74LCX245MSAX_NL
74LCX245MTC
74LCX245MTCX
74LCX245MTCX_NL
74LCX245SJ
74LCX245SJX
74LCX245SJX_NL
74LCX245WM
74LCX245WMX
74LCX245WMX_NL

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