REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20													

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
94-01-21

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, UV ERASABLE PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-90799**

SHEET 1 OF 20

DESC FORM 193
JUL 91

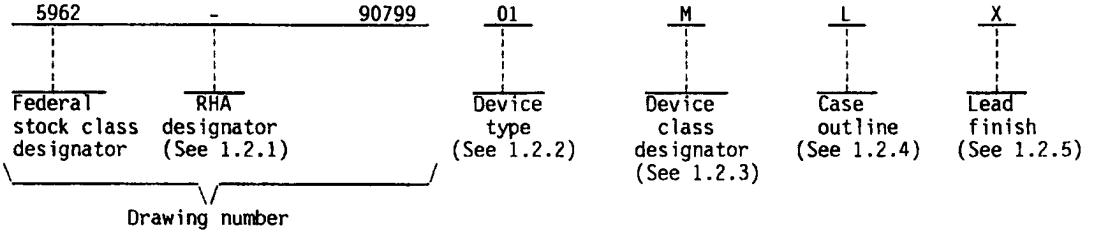
5962-E424-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device class M RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Propagation delay
01		24-Macrocell EPLD	35 ns
02		24-Macrocell EPLD	25 ns
03		24-Macrocell EPLD	20 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40, CDIP2-T40	40	Dual-in-line package 2/

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.

1.3 Absolute maximum ratings. 3/

Supply voltage range (V_{CC})	-2.0 V dc to +7.0 V dc
Programming supply voltage range (V_{PP})	-2.0 V dc to +13.5 V dc 4/
DC input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc 4/
Maximum power dissipation	1.0 W 5/
Lead temperature (soldering, 10 seconds)	+275°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline Q	See MIL-STD-1835
Junction temperature (T_J)	+150°C
Storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C
Endurance	25 erase/write cycles (minimum)
Data retention	10 years (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.0 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C 6/
Input rise time (t_R)	500 ns maximum
Input fall time (t_F)	500 ns maximum

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 7/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Minimum dc input voltage is -0.5 V. During transitions, inputs may undershoot to -2.0 V for periods less than 20 ns. Maximum dc voltage on output pins is V_{CC} + 0.5 V, which may overshoot to +7.0 V for periods less than 20 ns under no load conditions.
5/ Must withstand the added P_D due to short circuit test; e.g., I_{SC}.
6/ Case temperatures are instant on.
7/ Values will be added when they become available.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMDs).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standard Test Procedure for the Characterization LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Procedures from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are described in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPLD's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPLD's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6.

3.10.2 Programmability of EPLD's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7.

3.10.3 Verification of erasure or programmed EPLD's. When specified, devices shall be verified as either programmed (see 4.7 herein) to the specified pattern or erased (see 4.6 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OH} = -4.0 mA	1, 2, 3	All	2.4		V
Output low voltage 1/	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = 12.0 mA	1, 2, 3	All		0.5	V
Input high voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC} +.3 2/	V
Input low voltage	V_{IL}		1, 2, 3	All	-0.3 2/	0.8	V
Input leakage current	I_L	V_{CC} = 5.5 V, GND < V_{IN} < 5.5 V	1, 2, 3	All	-10	10	µA
Three-state output off current 2/	I_{OZ}	V_{CC} = 5.5 V, GND < V_{OUT} < 5.5 V	1, 2, 3	All	-10	10	µA
Output short circuit current 2/ 3/	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V	1, 2, 3	All	-30	-160	mA
Power supply current (turbo-off) 4/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} or GND, f_{in} = 1 MHz	1, 2, 3	All		12	mA
Power supply current (turbo-on) 4/	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} or GND, f = 1 MHz	1, 2, 3	All		180	mA
Power supply current (standby, nonturbo) 5/	I_{CC3}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND or V_{CC}	1, 2, 3	All		150	µA
Input capacitance	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0.0 V, T_A = +25°C, f = 1 MHz (see 4.4.1e)	4	All		8	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0.0 V, T_A = +25°C, f = 1 MHz (see 4.4.1e)	4	All		8	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
External synchronous switching characteristics							
V_{PP} capacitance	C_{VPP}	$V_{CC} = 5.0\ V$, $V_{OUT} = 0.0\ V$, VPP on C_{LK2}, $T_A = +25°C$, $f = 1\ MHz$ (see 4.4.1e)	4	All		12	pF
C_{CLK} capacitance	C_{CLK}	$V_{CC} = 5.0\ V$, $V_{OUT} = 0.0\ V$, $T_A = +25°C$, $f = 1\ MHz$ (see 4.4.1e)	4	All		10	pF
Functional tests		See 4.4.1c	7,8A,8B	All			
Input or I/O to nonregistered output 6/	t_{PD}	See figures 3 and 4 7/ $C_L = 30\ pF$	9, 10, 11	01		30	ns
				02		25	
				03		20	
Input or I/O to Asynchronous reset	t_{CLR}		9, 10, 11	01		33	ns
				02		28	
				03		23	
Input or I/O to output enable 2/ 8/	t_{PZX}		9, 10, 11	01		33	ns
				02		28	
				03		23	
Input or I/O to output disable 2/ 8/	t_{PXZ}	See figures 3 and 4 7/ $C_L = 5\ pF$	9, 10, 11	01		33	ns
				02		28	
				03		23	
Maximum frequency ($1/t_{CP}$) No feedback 6/ 9/ 10/	f_{MAX}	Synchronous clock mode See figures 3 and 4 7/ $C_L = 30\ pF$	9, 10, 11	01	40		MHz
				02	50		
				03	66		
Maximum counter frequency ($1/t_{SU} + t_{CO}$) External feedback 6/ 11/	f_{CNT1}		9, 10, 11	01	29		MHz
				02	33		
				03	40		
Maximum counter frequency, ($1/t_{CNT}$). Internal feedback 6/ 12/	f_{CNT2}		9, 10, 11	01	33		MHz
				02	40		
				03	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input or I/O setup time to CLK	t_{SU}	Synchronous clock mode See figures 3 and 4 7/ C_L = 30 pF	9, 10, 11	01	18		ns
				02	16		
				03	13		
Input or I/O hold time from CLK	t_H		9, 10, 11	All	0		ns
Clock high to output valid 6/	t_{CO1}		9, 10, 11	01		16	ns
				02		14	
				03		12	
Clock high to output valid, fed through combinatorial macrocell.	t_{CO2}		9, 10, 11	01		35	ns
				02		30	
				03		25	
Macrocell output feedback to to macrocell input, internal path 2/ 6/	t_{CNT}		9, 10, 11	01		30	ns
				02		25	
				03		20	
Clock high time 2/	t_{CH}		9, 10, 11	01	10		ns
				02	8		
				03	6		
Clock low time 2/	t_{CL}		9, 10, 11	01	10		ns
				02	8		
				03	6		
Clock period 2/	t_{CP}		9, 10, 11	01	25		ns
				02	20		
				03	15		
Maximum counter frequency 1/(tASU + tACO), external feedback. 6/	f_{ACNT1}	See figures 3 and 4 7/ C_L = 30 pF	9, 10, 11	01	23		MHz
				02	27.7		
				03	35.6		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Maximum counter frequency $1/(t_{ACNT})$, internal feedback. 6/ 13/	f_{ACNT2}	See figures 3 and 4 7/ C_L = 30 pF	9, 10, 11	01	33		MHz
				02	40		
				03	50		
Input or I/O setup time to asynchronous CLK	t_{ASU}		9, 10, 11	01	10		ns
				02	8		
				03	5		
Input or I/O hold time from asynchronous CLK	t_{AH}		9, 10, 11	01	13		ns
				02	11		
				03	9		
Asynchronous clock high to output valid 6/	t_{ACO1}		9, 10, 11	01		33	ns
				02		28	
				03		23	
Asynchronous clock high to output valid fed through combinatorial macrocell. 2/	t_{ACO2}		9, 10, 11	01		50	ns
				02		44	
				03		36	
Macrocell output feedback to macrocell input, internal path. 2/ 6/	t_{ACNT}		9, 10, 11	01		30	ns
				02		25	
				03		20	
Asynchronous clock high time 2/	t_{ACH}		9, 10, 11	01	12		ns
				02	10		
				03	8		
Asynchronous clock low time 2/	t_{ACL}		9, 10, 11	01	12		ns
				02	10		
				03	8		
Asynchronous clock period	t_{ACP}		9, 10, 11	01	30		ns
				02	25		
				03	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Maximum DC I_{OL} for the device is 96 mA for CLK1 group I/O 1 - I/O 12 and 96 mA for CLK2 group I/O 13 - I/O 24.
2/ Guaranteed but not tested.
3/ For test purposes, not more than one output at a time should be tested. Short circuit test duration should not exceed 1 second.
4/ Specified and correlated to device programmed as two 12-bit counters and no output loading.
5/ With turbo bit off, device automatically enters standby mode approximately 100 ns after last input transition.
6/ Measured with all eight I/Os switching.
7/ AC tests are performed with input rise and fall times of ≤ 3 ns, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3.
8/ t_{PZX} and t_{PXZ} are measured at ±0.5 V from steady-state voltage as driven by specification output load. t_{PXZ} is measured with C_L = 5 pF.
9/ f_{MAX} represents the highest clock frequency for pipelined data.
10/ Not tested directly, but derived from $1/t_{CP}$.
11/ Not tested directly, but derived from t_{SU} and t_{CO1}.
12/ Not tested directly, but derived from t_{CNT}.
13/ Not tested directly, but derived from $1/t_{ACP}$.

3.11 Endurance. A reprogrammability test shall be completed as part of the vendors reliability monitors, this reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. This test shall consist of 25 program/erase cycles on 25 devices with the following conditions:

a. All devices selected for testing shall be programmed in accordance with 3.2.3.1 herein.

b. Verify pattern (see 3.10.3).

c. Erase (see 3.10.1).

d. Verify pattern erasure (see 3.10.3).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

d. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.)

Margin test method .

(1) Program a minimum of 95 percent of the total number of cells, including the slowest programming cell (see 3.10.2).
(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C or for 2 hours at +300°C for unassembled devices only.
(3) Perform electrical test (see 4.2.1c) at +25°C including a margin test at V_m = 5.7 V and loose timing (i.e., 1 μs).
(4) Erase (see 3.10.1).
(5) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell (see 3.10.2).
(6) Perform electrical test (see 4.2.1c) at +25°C including a margin test at V_m = 5.7 V and loose timing (i.e., 1 μs).
(7) Perform burn-in (see 4.2.1b).
(8) Perform electrical test (see 4.2.1c) at +25°C including a margin test at V_m = 5.7 V and loose timing (i.e., 1 μs).
(9) Perform electrical tests at T_C = +125°C.
(10) Perform electrical tests at T_C = -55°C.
(11) Erase (see 3.10.1). Devices may be submitted for groups A, B, C, and D testing.
(12) Verify erasure (see 3.10.3).

Device types	All
Case outline	Q
Terminal number	Terminal symbol
1	CLK_1
2	I
3	I
4	I
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I
18	I
19	I
20	GND
21	CLK
22	I
23	I
24	I
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I
38	I
39	I
40	V_{CC}

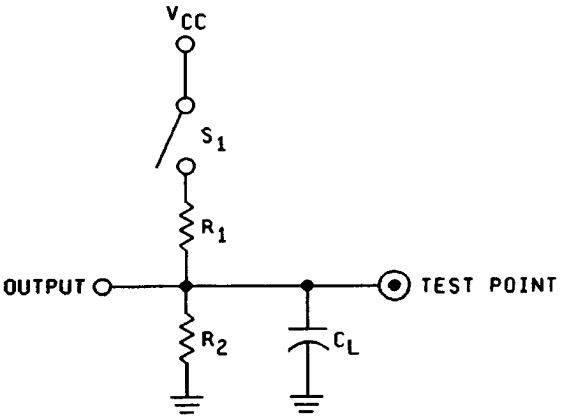
FIGURE 1. Terminal connections.

INPUT PINS													
CLK1	CLK2	I	I	I	I	I	I	I	I	I	I	I	I
X	X	X	X	X	X	X	X	X	X	X	X	X	X

OUTPUT PINS											
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Note: X = Don't care
Z = High impedance

FIGURE 2. Truth table.



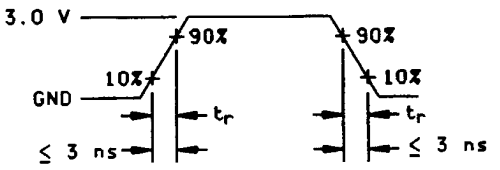
Switch test circuit

Specification	S_1	C_L	Commercial		Measured output value
			R_1	R_2	
t_{PD}	Closed	30 pF	200Ω	330Ω	1.5 V
t_{PZX}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} - 0.5 V L → Z: V_{OL} + 0.5 V

AC test conditions

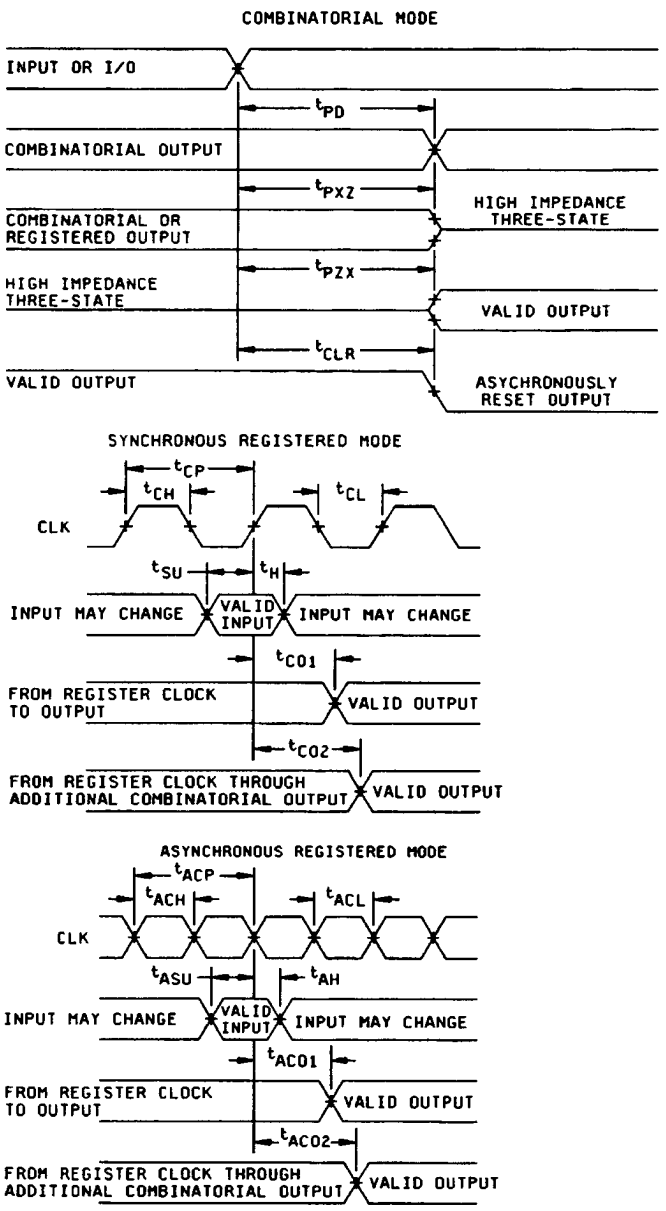
Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 3 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

Input pulses



NOTE: Power supply transients can affect ac measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under ac conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.

FIGURE 3. Output load circuit and test conditions.



NOTES:
1. t_R and t_F = 3 ns maximum.
2. All other timings are at 1.5 V. Input levels are at 0 V and 3 V.

FIGURE 4. Switching waveforms.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5)

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8A, 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8A, 8B shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (Latch-up) test shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, the procedures and circuits shall be maintained under document revision control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technology review board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. A sample size of 15 devices with no failures, and all input and output terminals shall be tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein. The devices selected for testing shall be programmed in accordance with 3.2.3.1 herein. After completion of testing, the devices shall be erased and verified (except devices submitted for group D testing, and devices to be archived, i.e., devices not to be sold).

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005,table I)	Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1	1,7,9	1,7,9
2	Static burn-in I and II method 1015	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters (programmed devices)	1*,2,3, 7*,8A,8B, 9	1*,2,3, 7*,8A,8B, 9,10,11	1*,2,3, 7*,8A,8B, 9,10,11
6a	Final electrical parameters (un-programmed devices)	1*,2,3, 7*,8A,8B	1*,2,3, 7*,8A,8B	1*,2,3, 7*,8A,8B
7	Group A test requirements	1,2,3, 4**,7, 9,10,11	1,2,3, 4**,7, 8A,8B,9, 10,11	1,2,3, 4**,7, 8A,8B,9, 10,11
8	Group C end-point electrical parameters	2,8A,10	1,2,3,7, 8A,8B Δ	1,2,3,7,8 9,10,11Δ
9	Group D end-point electrical parameters	2,8A,10	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high speed testers.
3/ Subgroups 7 and 8 functional tests shall also verify functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ (Δ) indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see line 1).
7/ See 4.4.1d

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC3}	±10% of specified value in table I
I_{OZ}	±10% of specified value in table I
I_L	±10% of specified value in table I

1/ The above parameters shall be recorded before and after the required burn-in and life test to determine the delta.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.7 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMDs. All proposed changes to existing SMDs will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1692, Engineering Change Proposal (Short Form).

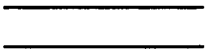
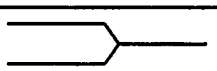
6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN'S. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.