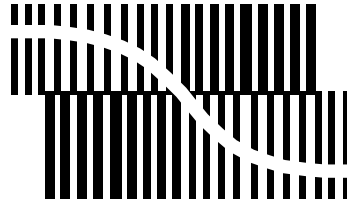


# DATA SHEET



BITSTREAM CONVERSION

## **UDA1342TS** **Audio CODEC**

Product specification  
Supersedes data of 2000 Mar 29  
File under Integrated Circuits, IC01

2000 Jul 31

**Audio CODEC****UDA1342TS****CONTENTS**

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## Audio CODEC

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**1 FEATURES****General**

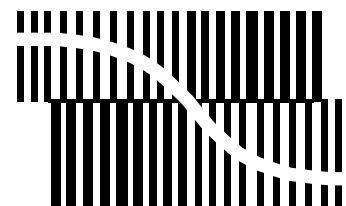
- 2.7 to 3.6 V power supply
- 5 V tolerant digital inputs
- High pin compatibility with UDA1341TS
- 24 bits data path
- Selectable control via L3-bus interface, I<sup>2</sup>C-bus interface or static pin control; choice of 2 device addresses in L3-bus and I<sup>2</sup>C-bus mode
- Supports sample frequencies from 16 to 110 kHz
- Separate power control for ADC and DAC
- ADC and Programmable Gain Amplifiers (PGA) plus integrated high-pass filter to cancel DC offset
- Integrated digital filter plus DAC
- Digital silence detection
- No analog post filtering required for DAC
- Slave mode only applications
- Easy application.

**Multiple format data interface**

- I<sup>2</sup>S-bus, MSB-justified and LSB-justified format compatible
- 1f<sub>s</sub> to 4f<sub>s</sub> input and 1f<sub>s</sub> output format data rate.

**DAC digital sound processing**

- Separate digital logarithmic volume control for left and right channels in L3-bus mode or I<sup>2</sup>C-bus mode
- Digital tone control, bass boost and treble in L3-bus mode or I<sup>2</sup>C-bus mode
- Digital de-emphasis for sample frequencies of 32, 44.1, 48 and 96 kHz in L3-bus mode or I<sup>2</sup>C-bus mode
- Soft or quick mute in L3-bus mode or I<sup>2</sup>C-bus mode
- Output signal polarity control in L3-bus mode or I<sup>2</sup>C-bus mode
- Digital mixer for ADC output signal and digital serial input signal.



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**Advanced audio configuration**

- 4 channel (2 × stereo) single-ended inputs with programmable gain amplifiers and 2 channel (1 × stereo) single-ended outputs configuration
- Output signal polarity control in L3-bus mode or I<sup>2</sup>C-bus mode
- High linearity, wide dynamic range, low distortion
- Double differential input configuration for enhanced ADC sound quality.

**2 APPLICATIONS**

- Eminently suitable for MiniDisc (MD) home and portable applications.

**3 GENERAL DESCRIPTION**

The UDA1342TS is a single-chip 4 channel analog-to-digital converter and 2 channel digital-to-analog converter with signal processing features employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

The UDA1342TS supports the I<sup>2</sup>S-bus data format with word lengths of up to 24 bits, the MSB-justified data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits. The device also supports a combination of the MSB-justified output format and the LSB-justified input format.

The UDA1342TS has special sound processing features in the playback mode such as de-emphasis, volume, mute, bass boost and treble, which can be controlled by the microcontroller via the L3-bus or I<sup>2</sup>C-bus interface.

## Audio CODEC

## UDA1342TS

## 4 QUICK REFERENCE DATA

| SYMBOL                             | PARAMETER  | CONDITIONS   | MIN. | TYP. | MAX. | UNIT         |
|------------------------------------|--|--|------|------|------|--------------|
| <b>Supplies</b>                    |  |  |      |      |      |              |
| $V_{DDA(ADC)}$                     | ADC analog supply voltage  |  | 2.7  | 3.0  | 3.6  | V            |
| $V_{DDA(DAC)}$                     | DAC analog supply voltage  |  | 2.7  | 3.0  | 3.6  | V            |
| $V_{DDD}$                          | digital supply voltage   |  | 2.7  | 3.0  | 3.6  | V            |
| $I_{DDA(ADC)}$                     | ADC analog supply current  | 1 ADC + 1 PGA enabled                                | –    | 10.0 | –    | mA           |
|                                    |  | 2 ADCs + 2 PGAs enabled                              | –    | 20.0 | –    | mA           |
|                                    |  | all ADCs + all PGAs power-down                       | –    | 200  | –    | $\mu$ A      |
| $I_{DDA(DAC)}$                     | DAC analog supply current  | operating  | –    | 6.0  | –    | mA           |
|                                    |  | DAC power-down                                       | –    | 250  | –    | $\mu$ A      |
| $I_{DDD}$                          | digital supply current   | operating  | –    | 9.0  | –    | mA           |
|                                    |  | ADC power-down                                       | –    | 4.5  | –    | mA           |
|                                    |  | DAC power-down                                       | –    | 5.5  | –    | mA           |
| $T_{amb}$                          | ambient temperature  |  | –40  | –    | +85  | $^{\circ}$ C |
| <b>Analog-to-digital convertor</b> |  |  |      |      |      |              |
| $V_{i(rms)}$                       | input voltage (RMS value)  | at 0 dB (FS) digital output                          | –    | 0.9  | –    | V            |
| $(THD+N)/S_{48}$                   | total harmonic distortion-plus-noise to signal ratio at $f_s = 48$ kHz | normal mode  | –    | –90  | –    | dB           |
|                                    |  | at –1 dB   | –    | –90  | –    | dB           |
|                                    |  | at –60 dB; A-weighted                                | –    | –40  | –    | dB           |
|                                    |  | double differential                                  | –    | –93  | –    | dB           |
| $(THD+N)/S_{96}$                   | total harmonic distortion-plus-noise to signal ratio at $f_s = 96$ kHz | at –1 dB   | –    | –84  | –    | dB           |
|                                    |  | at –60 dB; A-weighted                                | –    | –39  | –    | dB           |
| $S/N_{48}$                         | signal-to-noise ratio at $f_s = 48$ kHz                                | normal mode;<br>$V_i = 0$ V; A-weighted              | –    | 100  | –    | dB           |
|                                    |  | double differential mode;<br>$V_i = 0$ V; A-weighted | –    | 101  | –    | dB           |
| $S/N_{96}$                         | signal-to-noise ratio at $f_s = 96$ kHz                                | normal mode;<br>$V_i = 0$ V; A-weighted              | –    | 99   | –    | dB           |
| $\alpha_{cs}$                      | channel separation   |  | –    | 100  | –    | dB           |

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| SYMBOL                             | PARAMETER  | CONDITIONS                         | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|--|------------------------------------|------|------|------|------|
| <b>Digital-to-analog convertor</b> |  |                                    |      |      |      |      |
| $V_{o(rms)}$                       | output voltage (RMS value)   | at 0 dB (FS) digital input; note 1 | –    | 0.9  | –    | V    |
| $(THD+N)/S_{48}$                   | total harmonic distortion-plus-noise to signal ratio at $f_s = 48$ kHz | at 0 dB                            | –    | –90  | –    | dB   |
|                                    |  | at –60 dB; A-weighted              | –    | –40  | –    | dB   |
| $(THD+N)/S_{96}$                   | total harmonic distortion-plus-noise to signal ratio at $f_s = 96$ kHz | at 0 dB                            | –    | –83  | –    | dB   |
|                                    |  | at –60 dB; A-weighted              | –    | –39  | –    | dB   |
| $S/N_{48}$                         | signal-to-noise ratio at $f_s = 48$ kHz                                | code = 0; A-weighted               | –    | 100  | –    | dB   |
| $S/N_{96}$                         | signal-to-noise ratio at $f_s = 96$ kHz                                | code = 0; A-weighted               | –    | 99   | –    | dB   |
| $\alpha_{CS}$                      | channel separation   |                                    | –    | 100  | –    | dB   |

**Note**

1. The output voltage of the DAC is proportionally to the DAC power supply voltage.

**5 ORDERING INFORMATION**

| TYPE NUMBER | PACKAGE |   |          |
|-------------|---------|---|----------|
|             | NAME    | DESCRIPTION   | VERSION  |
| UDA1342TS   | SSOP28  | plastic shrink small outline package; 28 leads; body width 5.3 mm | SOT341-1 |

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6 BLOCK DIAGRAM

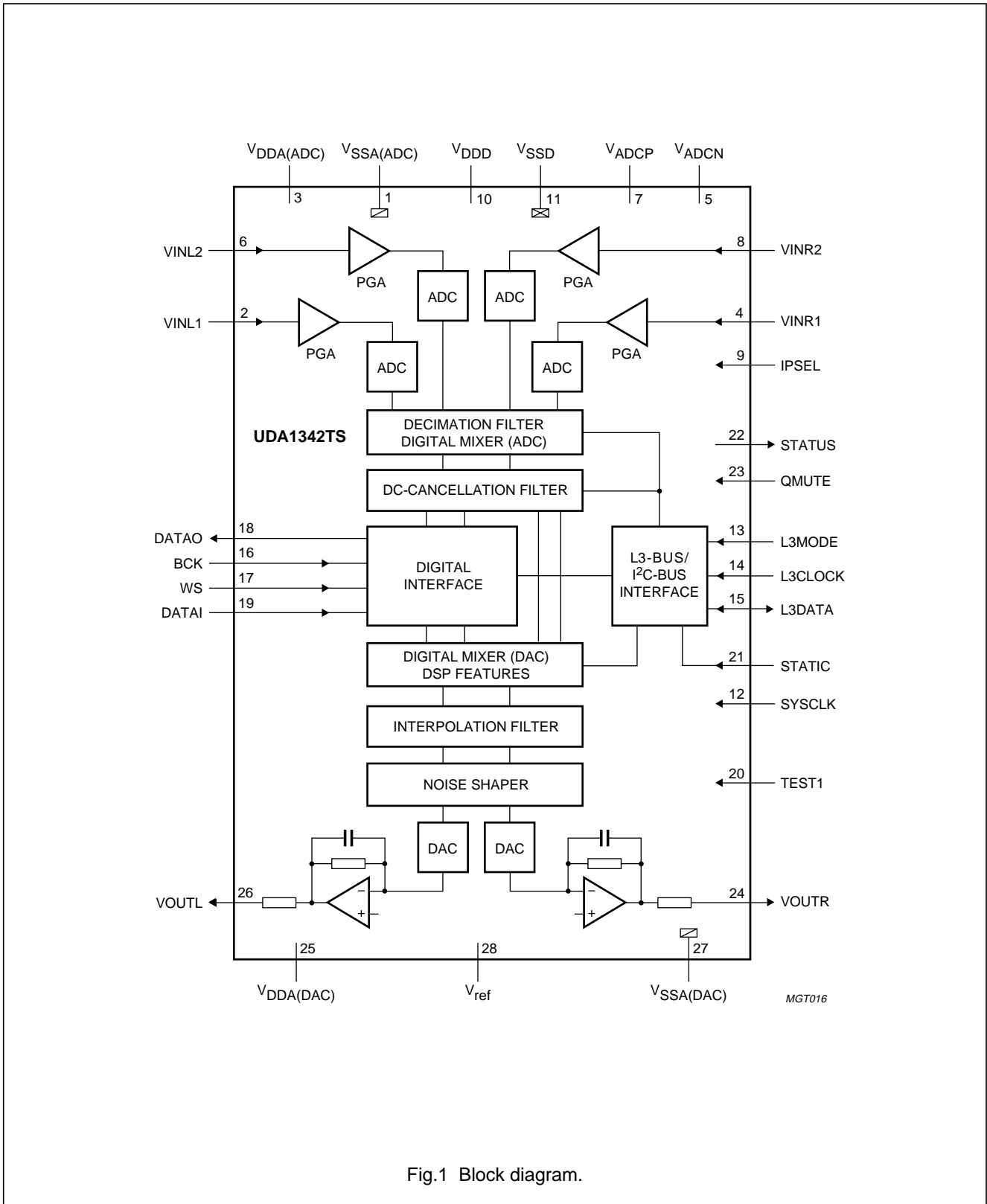


Fig.1 Block diagram.

## Audio CODEC

## UDA1342TS

## 7 PINNING

| SYMBOL                | PIN | TYPE  | DESCRIPTION  |
|-----------------------|-----|---|--|
| V <sub>SSA(ADC)</sub> | 1   | analog ground pad                                     | ADC analog ground  |
| VINL1                 | 2   | analog input pad                                      | ADC input left 1   |
| V <sub>DDA(ADC)</sub> | 3   | analog supply pad                                     | ADC analog supply voltage  |
| VINR1                 | 4   | analog input pad                                      | ADC input right 1  |
| V <sub>ADCN</sub>     | 5   | analog pad  | ADC reference voltage N  |
| VINL2                 | 6   | analog input pad                                      | ADC input left 2   |
| V <sub>ADCP</sub>     | 7   | analog pad  | ADC reference voltage P  |
| VINR2                 | 8   | analog input pad                                      | ADC input right 2  |
| IPSEL                 | 9   | 5 V tolerant digital input pad                        | channel select input: input left 1 and right 1 or input left 2 and right 2                         |
| V <sub>DDD</sub>      | 10  | digital supply pad                                    | digital supply voltage   |
| V <sub>SSD</sub>      | 11  | digital ground pad                                    | digital ground   |
| SYSCLK                | 12  | 5 V tolerant digital input pad                        | system clock input: 256f <sub>s</sub> , 384f <sub>s</sub> , 512f <sub>s</sub> or 768f <sub>s</sub> |
| L3MODE                | 13  | 5 V tolerant digital input pad                        | L3-bus mode input or mode selection input  |
| L3CLOCK               | 14  | 5 V tolerant digital input pad                        | L3-bus/I <sup>2</sup> C-bus clock input or clock selection input                                   |
| L3DATA                | 15  | 5 V tolerant open drain input/output                  | L3-bus/I <sup>2</sup> C-bus data input/output or format selection input                            |
| BCK                   | 16  | 5 V tolerant digital input pad                        | bit clock input  |
| WS                    | 17  | 5 V tolerant digital input pad                        | word select input  |
| DATAO                 | 18  | 5 V tolerant 2 mA slew rate controlled digital output | data output  |
| DATAI                 | 19  | 5 V tolerant digital input pad                        | data input   |
| TEST1                 | 20  | 5 V tolerant digital input pad                        | test control input; to be connected to ground  |
| STATIC                | 21  | 5 V tolerant digital input pad                        | mode selection input: static pin control or L3-bus/I <sup>2</sup> C-bus control                    |
| STATUS                | 22  | 5 V tolerant 2 mA slew rate controlled digital output | general purpose output   |
| QMUTE                 | 23  | 5 V tolerant digital input pad                        | quick mute input   |
| VOUTR                 | 24  | analog output pad                                     | DAC output right   |
| V <sub>DDA(DAC)</sub> | 25  | analog supply pad                                     | DAC analog supply voltage  |
| VOUTL                 | 26  | analog output pad                                     | DAC output left  |
| V <sub>SSA(DAC)</sub> | 27  | analog ground pad                                     | DAC analog ground  |
| V <sub>ref</sub>      | 28  | analog pad  | reference voltage for ADC and DAC  |

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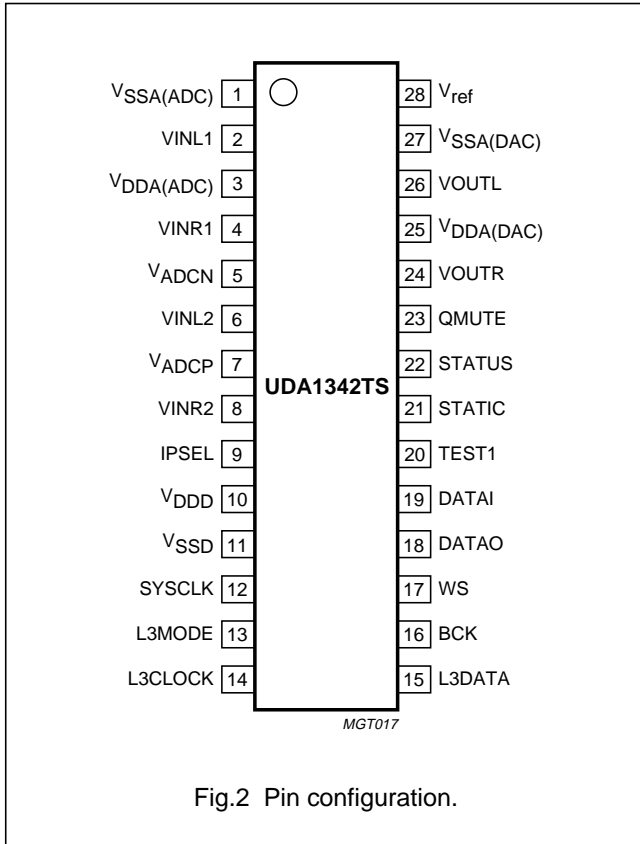


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1342TS operates in slave mode only, this means that in all applications the system must provide the system clock. The system clock frequency is selectable and depends on the mode of operation:

- L3-bus/I<sup>2</sup>C-bus mode: 256f<sub>s</sub>, 384f<sub>s</sub>, 512f<sub>s</sub> or 768f<sub>s</sub>
- Static pin mode: 256f<sub>s</sub> or 384f<sub>s</sub>.

The system clock must be locked in frequency to the digital interface signals.

Remarks:

- The bit clock frequency f<sub>BCK</sub> can be up to 128f<sub>s</sub>, or in other words the bit clock frequency is 128 times the word select frequency f<sub>WS</sub> or less: f<sub>BCK</sub> ≤ 128f<sub>WS</sub>
- The WS edge MUST fall on the negative edge of the BCK signal at all times for proper operation of the digital interface
- The UDA1342TS operates with sample frequencies from 16 to 110 kHz, however for a system clock of 768f<sub>s</sub> the sampling frequency must be limited to 55 kHz.

8.2 ADC analog front-end

The analog front-end of the UDA1342TS consists of two stereo ADCs with a programmable gain stage (gain from 0 to 24 dB with 3 dB steps) which can be controlled via the L3-bus/I<sup>2</sup>C-bus interface.

8.2.1 APPLICATION WITH 2 V (RMS) INPUT

In applications in which a 2 V (RMS) input signal is used, a 15 kΩ resistor must be used in series with the input of the ADC (see Fig.3). This forms a voltage divider together with the internal ADC resistor and ensures that only 1 V (RMS) maximum is input to the IC. Using this application for a 2 V (RMS) input signal, the gain switch must be set to 0 dB. When a 1 V (RMS) input signal is input to the ADC in the same application, the gain switch must be set to 6 dB.

An overview of the maximum input voltages allowed against the presence of an external resistor and the setting of the gain switch is given in Table 1.

Table 1 Application modes using input gain stage

| RESISTOR (15 kΩ) | PGA GAIN | MAXIMUM INPUT VOLTAGE |
|------------------|----------|-----------------------|
| Present          | 0 dB     | 2 V (RMS)             |
| Present          | 6 dB     | 1 V (RMS)             |
| Absent           | 0 dB     | 1 V (RMS)             |
| Absent           | 6 dB     | 0.5 V (RMS)           |

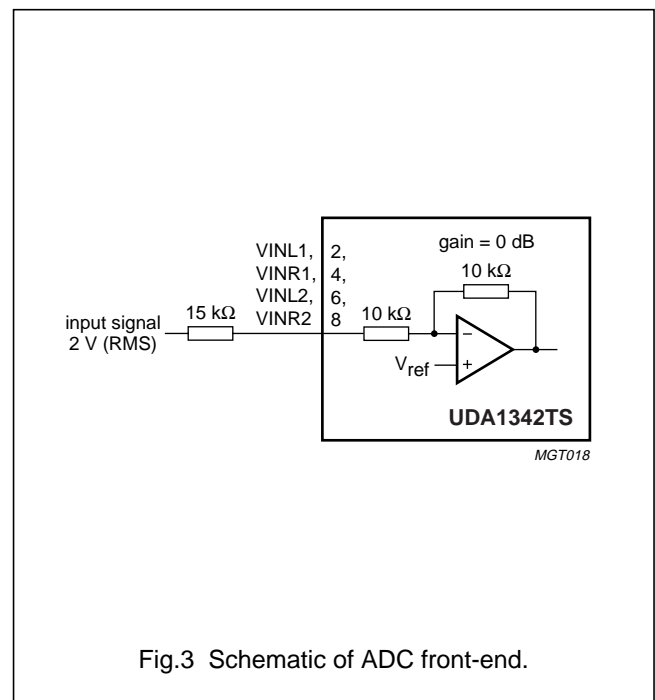


Fig.3 Schematic of ADC front-end.



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## 8.2.2 DOUBLE DIFFERENTIAL MODE

Since the UDA1342TS is equipped with two stereo ADCs, these two pairs of stereo ADCs can be used to convert a single stereo signal to a signal with a higher performance by using the ADCs in the double differential mode.

This mode and the input signals, being channel 1 or 2 as input to the double differential configuration, can be selected via the L3-bus/I<sup>2</sup>C-bus interface.

## 8.3 Decimation filter (ADC)

The decimation from 64f<sub>s</sub> to 1f<sub>s</sub> is performed in two stages.

The first stage realizes a  $\left(\frac{\sin x}{x}\right)^4$  characteristic with a

decimation factor of 8. The second stage consists of three half-band filters, each decimating by a factor of 2. The filter characteristics are shown in Table 2.

**Table 2** Decimation filter characteristics

| ITEM             | CONDITION               | VALUE (dB) |
|------------------|-------------------------|------------|
| Pass-band ripple | 0 to 0.45f <sub>s</sub> | ±0.01      |
| Pass-band droop  | 0.45f <sub>s</sub>      | -0.2       |
| Stop band        | >0.55f <sub>s</sub>     | -70        |
| Dynamic range    | 0 to 0.45f <sub>s</sub> | >135       |

## 8.4 Digital mixer (ADC)

The two stereo ADC outputs are mixed with gain coefficients from +24 to -63.5 dB to be set via the microcontroller interface.

In front of the mixer there is a DC filter. In order to prevent clipping, it is needed to filter out the DC component before mixing or amplifying the signals.

The mixing function can be enabled via the microcontroller interface.

## 8.5 Interpolation filter (DAC)

The digital interpolation filter interpolates from 1f<sub>s</sub> to 64f<sub>s</sub> by means of a cascade of FIR filters. The filter characteristics are shown in Table 3.

**Table 3** Interpolation filter characteristics

| ITEM             | CONDITION               | VALUE (dB) |
|------------------|-------------------------|------------|
| Pass-band ripple | 0 to 0.45f <sub>s</sub> | ±0.025     |
| Stop band        | >0.55f <sub>s</sub>     | -60        |
| Dynamic range    | 0 to 0.45f <sub>s</sub> | >135       |

## 8.6 Mute

Muting the DAC will result in a cosine roll-off soft mute, using 32 × 32 = 1024 samples in the normal mode: this results in 24 ms at f<sub>s</sub> = 44.1 kHz. The cosine roll-off curve is illustrated in Fig.4.

This cosine roll-off functions are implemented in the DAC data path before the digital mixer and before the master mute (see Fig.5).

In the L3-bus and I<sup>2</sup>C-bus mode, the setting of the master mute can be overruled always by pin QMUTE. This quick mute uses the same cosine roll-off, but now for only 32 samples: this is 750 μs at f<sub>s</sub> = 44.1 kHz.

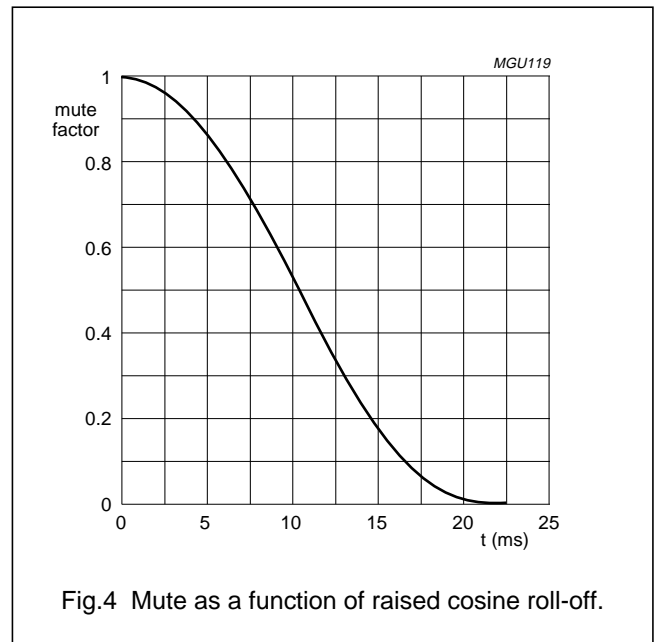


Fig.4 Mute as a function of raised cosine roll-off.

## 8.7 Digital mixer (DAC)

The ADC output signal and the digital interface input signal can be mixed without an external DSP (see Fig.5).

This mixer can be controlled via the microcontroller interface.

In order to prevent clipping when mixing two 0 dB signals, the signals are attenuated digitally by -6 dB before mixing. After mixing the signal is gained by 6 dB after the master volume. This way clipping at the digital mixer is prevented. After the 6 dB gain, the signals can clip again, but this clipping can be removed by decreasing the master volume.

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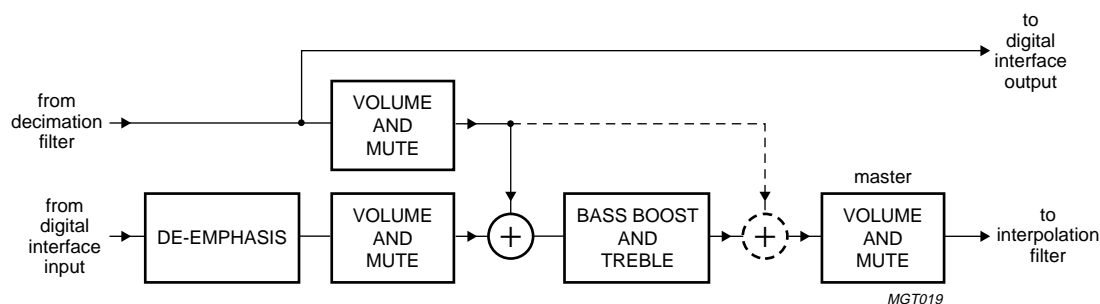


Fig.5 Digital mixer (DAC).

### 8.8 Noise shaper

The 5th-order noise shaper operates at  $64f_s$ . It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream Digital-to-Analog Converter (FSDAC).

### 8.9 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC is proportionally to the power supply voltage.

### 8.10 Digital interface

The UDA1342TS supports the following data input/output formats for the various modes (see Fig.6).

L3-bus and I<sup>2</sup>C-bus mode:

- I<sup>2</sup>S-bus format with data word length of up to 24 bits
- MSB-justified serial format with data word length of up to 24 bits
- LSB-justified serial format with data word lengths of 16, 20 or 24 bits
- MSB-justified data output and LSB-justified 16, 20 and 24 bits data input.

Static pin mode:

- I<sup>2</sup>S-bus format with data word length of up to 24 bits
- MSB-justified data output and LSB-justified 16, 20 and 24 bits data input.

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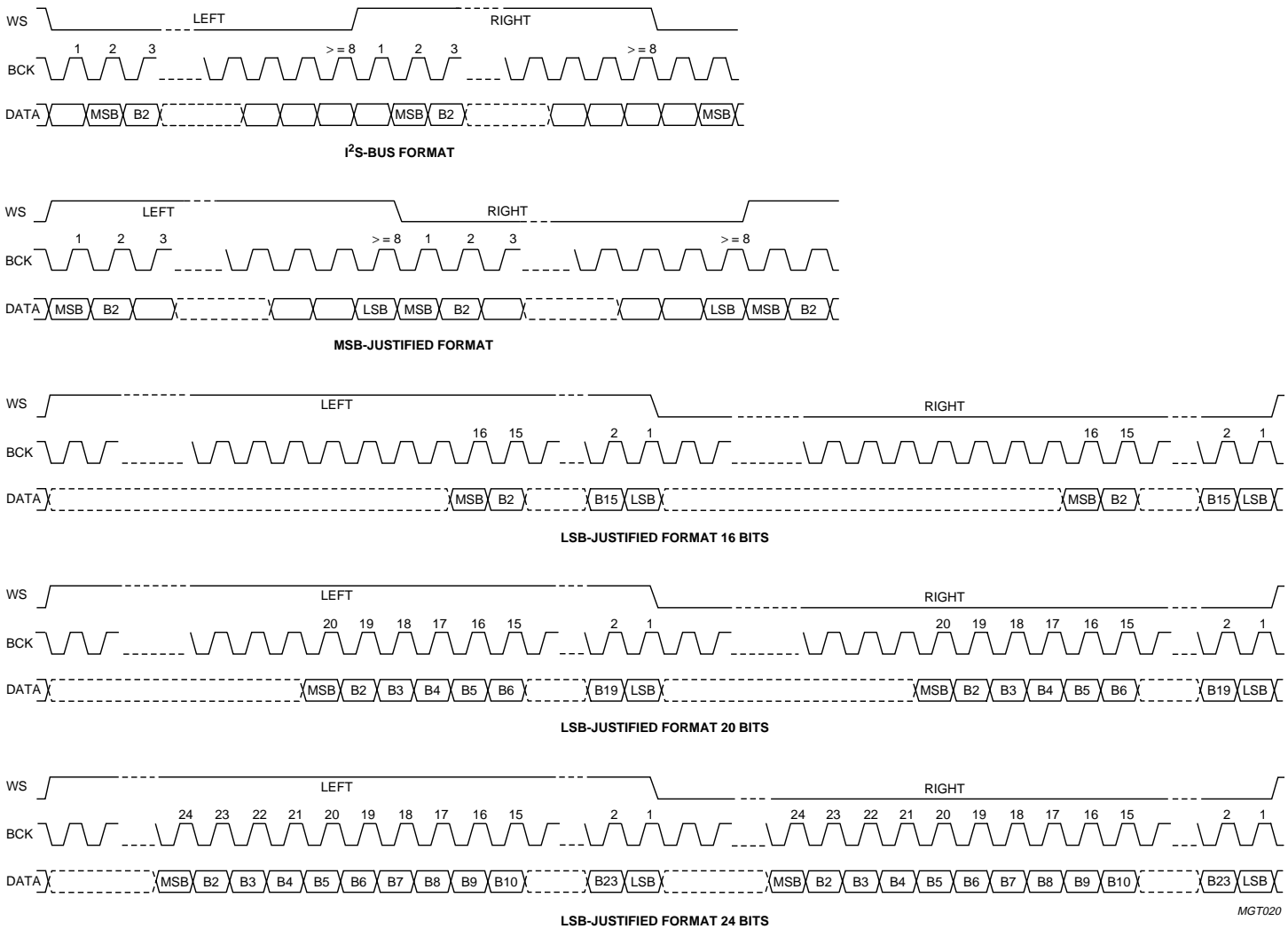


Fig.6 Serial interface input/output formats.

Audio CODEC

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8.11 Sampling speed

The UDA1342TS operates with sample frequencies from 16 to 110 kHz. This range holds for the CODEC as a whole. The DAC part can be configured in the L3-bus and I<sup>2</sup>C-bus mode to accept 2 times and even 4 times the data speed (e.g.  $f_s$  is 96 or 192 kHz), but in these modes not all of the features can be used.

**Important:** in the double speed mode an input signal of 0 dB is allowed, but in the quad speed mode the input signal must be limited to -6 dB to prevent the system from clipping.

Some examples of the input oversampling rate settings are shown in Table 4.

Table 4 Examples of the input oversampling rate settings

| SYSTEM CLOCK                 | SYSTEM CLOCK FREQUENCY SETTING | SAMPLING FREQUENCY (kHz) | INPUT OVER-SAMPLING RATE | FEATURES SUPPORTED          |
|------------------------------|--------------------------------|--------------------------|--------------------------|-----------------------------|
| 12.288 MHz (256 × 48 kHz)    | 256 $f_s$                      | 48                       | single speed             | all                         |
|                              |                                | 96                       | double speed             | only master volume and mute |
|                              |                                | 192                      | quad speed               | no features                 |
| 22.5792 MHz (512 × 44.1 kHz) | 512 $f_s$                      | 44.1                     | single speed             | all                         |
|                              | 256 $f_s$                      | 88.2                     | single speed             | all                         |
|                              |                                | 176.4                    | double speed             | only master volume and mute |
| 33.8688 MHz (768 × 44.1 kHz) | 768 $f_s$                      | 44.1                     | single speed             | all                         |
|                              | 384 $f_s$                      | 88.2                     | single speed             | all                         |
|                              |                                | 176.4                    | double speed             | only master volume and mute |

8.12 Power-on reset

The UDA1342TS has an internal Power-on reset circuit (see Fig.7) which resets the test control block. All the digital sound processing features and the system controlling features are set to their default setting in the L3-bus and I<sup>2</sup>C-bus mode.

The reset time (see Fig.8) is determined by an external capacitor which is connected between pin  $V_{ref}$  and ground. The reset time should be at least 1  $\mu$ s for  $V_{ref} < 1.25$  V. When  $V_{DDA(DAC)}$  is switched off, the device will be reset again for  $V_{ref} < 0.75$  V.

During the reset time the system clock should be running.

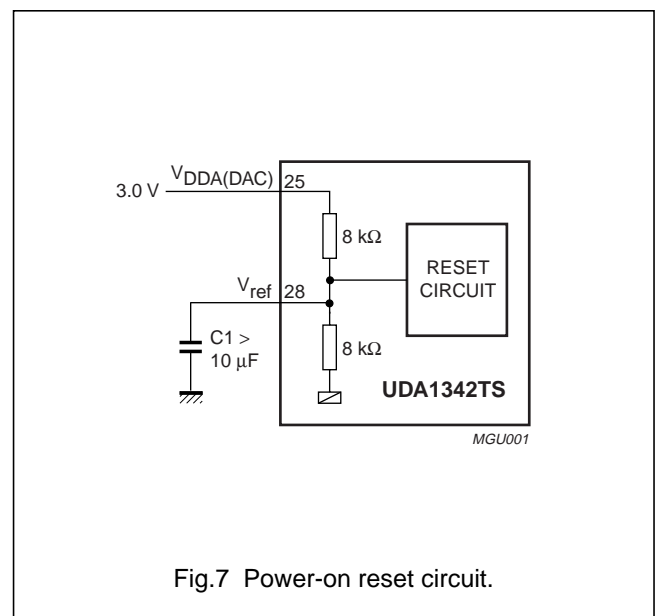


Fig.7 Power-on reset circuit.

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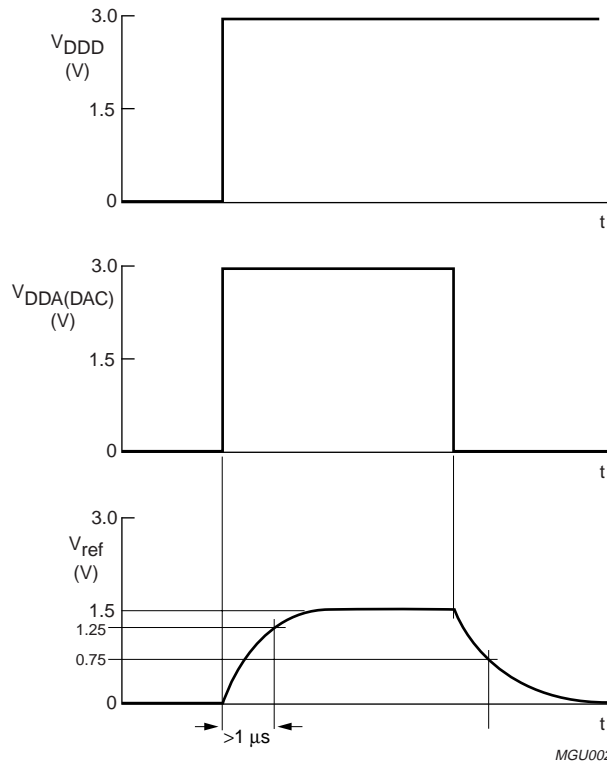


Fig.8 Power-on reset timing.

8.13 Control modes

The control mode can be set with pin STATIC and pin L3MODE:

- Static pin mode
- I<sup>2</sup>C-bus mode
- L3-bus mode.

Table 5 Mode selection

| PIN STATIC | PIN L3MODE | SELECTION                 |
|------------|------------|---------------------------|
| LOW        | –          | L3-bus mode               |
| HIGH       | LOW        | I <sup>2</sup> C-bus mode |
| HIGH       | HIGH       | static pin mode           |

The pin functions in the various modes are summarized in Table 6.

Table 6 Pin function in the selected mode

| PIN NAME | FUNCTION    |                           |                 |
|----------|-------------|---------------------------|-----------------|
|          | L3-BUS MODE | I <sup>2</sup> C-BUS MODE | STATIC PIN MODE |
| L3CLOCK  | L3CLOCK     | SCL                       | clock select    |
| L3MODE   | L3MODE      | LOW level                 | HIGH level      |
| L3DATA   | L3DATA      | SDA                       | format select   |
| QMUTE    | QMUTE       | QMUTE                     | format select   |
| IPSEL    | A0          | A0                        | channel select  |

All features in the L3-bus and I<sup>2</sup>C-bus mode are explained in Sections 8.15 and 8.16.

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8.14 Static pin mode

The controllable features in the static pin mode are:

- System clock frequency
- Data input and output format select
- ADC input channel select.

8.14.1 SYSTEM CLOCK SETTING SELECT

In the static pin mode pin L3CLOCK is used to select the system clock setting.

Table 7 System clock setting

| PIN L3CLOCK | SYSTEM CLOCK SETTING |
|-------------|----------------------|
| 0           | 256f <sub>s</sub>    |
| 1           | 384f <sub>s</sub>    |

8.14.2 DIGITAL INTERFACE FORMAT SELECT

In the static pin mode the digital interface audio formats can be selected via pins L3DATA and QMUTE. The following interface formats can be selected (see Table 8):

- I<sup>2</sup>S-bus format with data word length of up to 24 bits
- MSB-justified output format and LSB-justified input format with data word length of 16, 20 or 24 bits.

Table 8 Data format select in static pin mode

| PIN L3DATA | PIN QMUTE | INPUT/OUTPUT FORMAT                                  |
|------------|-----------|--|
| 0          | 0         | I <sup>2</sup> S                                     |
| 0          | 1         | LSB-justified 16 bits input and MSB-justified output |
| 1          | 0         | LSB-justified 20 bits input and MSB-justified output |
| 1          | 1         | LSB-justified 24 bits input and MSB-justified output |

8.14.3 ADC INPUT CHANNEL SELECT

In the static pin mode pin IPSEL selects the ADC input channel.

Table 9 ADC input channel select

| PIN IPSEL | CHANNEL SELECT                         |
|-----------|--|
| 0         | input channel 1 (pins VINL1 and VINR1) |
| 1         | input channel 2 (pins VINL2 and VINR2) |

8.15 L3-bus interface

All digital processing features and system controlling features of the UD1342TS can be controlled by a microcontroller via the L3-bus interface.

The controllable features are:

- Reset
- System clock frequency
- Data input and output format
- Multi purpose output
- ADC features
  - Operation mode control
  - Polarity control
  - Input amplifier gain control
  - Mixer control
  - DC filtering.
- DAC features
  - Power control
  - Polarity control
  - Input data oversampling rate
  - Mixer position selection
  - Mixer control
  - Silence detector
  - De-emphasis
  - Volume
  - Flat/min./max. switch
  - Bass boost
  - Treble
  - Mute
  - Quick mute mode.

8.15.1 INTRODUCTION

The exchange of data and control information between the microcontroller and the UDA1342TS is accomplished through a serial hardware interface comprising the following pins:

- L3DATA: microcontroller interface data line
- L3MODE: microcontroller interface mode line
- L3CLOCK: microcontroller interface clock line.

The UDA1342TS acts as a slave receiver or a slave transmitter. Therefore L3CLOCK and L3MODE lines transfer only input data and the L3DATA line transfers bidirectional data.

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Information transfer via the microcontroller bus is organized LSB first and in accordance with the so called 'L3' format, in which two different modes of operation can be distinguished: address mode and data transfer mode.

**Important:**

- When the device is powered-up, at least one L3CLOCK pulse must be sent to the L3-bus interface to wake-up the interface prior to sending information to the device. This is only needed once after the device is powered-up.
- Inside the microcontroller there is a hand-shake mechanism which handles proper data transfer from the microcontroller clock to destination clock domains. This means that when data is sent to the microcontroller interface, the system clock must be running.
- The L3-bus interface is designed in such a way that data is clocked into the device (write mode) on the positive clock edge, while the device starts the output data (read mode) on the negative clock edge. The microcontroller must read the data from the device on the positive clock edge to ensure the data is always stable.

8.15.2 DEVICE ADDRESSING

The device address mode is used to select a device for subsequent data transfer. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 bits. The fundamental timing in the address mode is shown in Fig.13.

The device address consists of one byte, which is split up in two parts (see Table 10):

- Bits 0 and 1 are called Data Operation Mode (DOM) bits and represent the type of data transfer
- Bits 2 to 7 represent a 6-bit device address.

**Table 10** L3-bus interface slave address

| DOM |       | DEVICE ADDRESS |       |       |       |       |     |
|-----|-------|----------------|-------|-------|-------|-------|-----|
| LSB | BIT 1 | BIT 2          | BIT 3 | BIT 4 | BIT 5 | BIT 6 | MSB |
| R/W | 1     | IPSEL          | 0     | 1     | 0     | 0     | 0   |

The UDA1342TS can be set to different addresses (00 1000 or 10 1000) by setting pin IPSEL to HIGH or LOW level. In the event that the device receives a different address, it will deselect its microcontroller interface logic.

Basically, 2 types of data transfer can be defined: data transfer to the device and data transfer from the device (see Table 11).

**Table 11** Selection of data transfer

| DOM   |       | TRANSFER                   |
|-------|-------|----------------------------|
| BIT 0 | BIT 1 |                            |
| 0     | 0     | not used                   |
| 1     | 0     | not used                   |
| 0     | 1     | data write or prepare read |
| 1     | 1     | data read                  |

8.15.3 REGISTER ADDRESSING

After sending the device address, including the flags (DOM bits) whether the information is read or written, the data transfer mode is entered and one byte is sent with the destination register address (see Table 12) using 7 bits, and one bit which signals whether information will be read or written.

The fundamental timing for the data transfer mode is given in Fig.14.

**Table 12** L3-bus register address

| LSB | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5 | BIT 6 | MSB |
|-----|-------|-------|-------|-------|-------|-------|-----|
| R/W | A6    | A5    | A4    | A3    | A2    | A1    | A0  |

Basically there are 3 cases for register addressing:

1. Register addressing for L3-bus write: the first bit is at logic 0 indicating a write action to the destination register, and is followed by 7 bits indicating the register address.
2. Prepare read addressing: the first bit of the byte is at logic 1, signalling data will be read from the register indicated.
3. Read action itself: in this case the device returns a register address prior to sending data from that register. When the first bit of the byte is at logic 0, the register address was valid and if the first bit is at logic 1 the register address was invalid.

**Important:**

1. Each time a new destination address needs to be written, the device address must be sent again.
2. When addressing the device for the first time after power-up of the device, at least one L3CLOCK cycle must be given to enable the L3-bus interface.

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8.15.4 DATA WRITE MODE

The data write format is given in Table 13 and illustrated in Fig.9.

When writing data to a device four bytes must be sent:

1. One byte with the device address, being '01X0 1000' where 'X' stands for the IPSEL value, including '01' for signalling write to the device.
2. One byte starting with a logic 0 for signalling write followed by 7 bits indicating the register address.
3. One byte which is the Most Significant Data (MSD) byte 1.
4. One byte which is the Least Significant Data (LSD) byte 2.

8.15.5 DATA READ MODE

The data write format is given in Table 14 and illustrated in Fig.10.

When reading from the device, a prepare read must first be done. After the prepare read, the device address is sent again. The device then returns with the register address, indicating whether the address was valid or not, and the data of the register.

The data read mode is explained below:

1. One byte with the device address, being '01X0 1000' where 'X' stands for the IPSEL value, including '01' for signalling write to the device.
2. One byte is sent with the register address which needs to be read. This byte starts with a logic 1, which indicates that there will be a read action from the register.
3. One byte with the device address including '11' is sent to the device. The '11' indicates that the device must write data to the microcontroller.
4. The device now writes the requested register address on the L3-bus, indicating whether the requested register was valid (logic 0) or invalid (logic 1).
5. The device writes data from the requested register to the L3-bus with the MSD byte 1 first, followed by the LSD byte 2.

**Table 13** L3-bus format for data write

| L3MODE          | DATA TYPE        | FIRST IN TIME |       |       |       |       | LAST IN TIME |       |       |
|-----------------|------------------|---------------|-------|-------|-------|-------|--------------|-------|-------|
|                 |                  | BIT 0         | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5        | BIT 6 | BIT 7 |
| Address         | device address   | 0             | 1     | IPSEL | 0     | 1     | 0            | 0     | 0     |
| Data transfer 1 | register address | 0             | A6    | A5    | A4    | A3    | A2           | A1    | A0    |
| Data transfer 2 | MSD byte 1       | D15           | D14   | D13   | D12   | D11   | D10          | D9    | D8    |
| Data transfer 3 | LSD byte 2       | D7            | D6    | D5    | D4    | D3    | D2           | D1    | D0    |

**Table 14** L3-bus format for prepare read and read data

| L3MODE              | DATA TYPE        | FIRST IN TIME |       |       |       |       | LAST IN TIME |       |       |
|---------------------|------------------|---------------|-------|-------|-------|-------|--------------|-------|-------|
|                     |                  | BIT 0         | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5        | BIT 6 | BIT 7 |
| <b>Prepare read</b> |                  |               |       |       |       |       |              |       |       |
| Address             | device address   | 0             | 1     | IPSEL | 0     | 1     | 0            | 0     | 0     |
| Data transfer 1     | register address | 1             | A6    | A5    | A4    | A3    | A2           | A1    | A0    |
| <b>Read data</b>    |                  |               |       |       |       |       |              |       |       |
| Address             | device address   | 1             | 1     | IPSEL | 0     | 1     | 0            | 0     | 0     |
| Data transfer 1     | register address | 0/1           | A6    | A5    | A4    | A3    | A2           | A1    | A0    |
| Data transfer 2     | MSD byte 1       | D15           | D14   | D13   | D12   | D11   | D10          | D9    | D8    |
| Data transfer 3     | LSD byte 2       | D7            | D6    | D5    | D4    | D3    | D2           | D1    | D0    |



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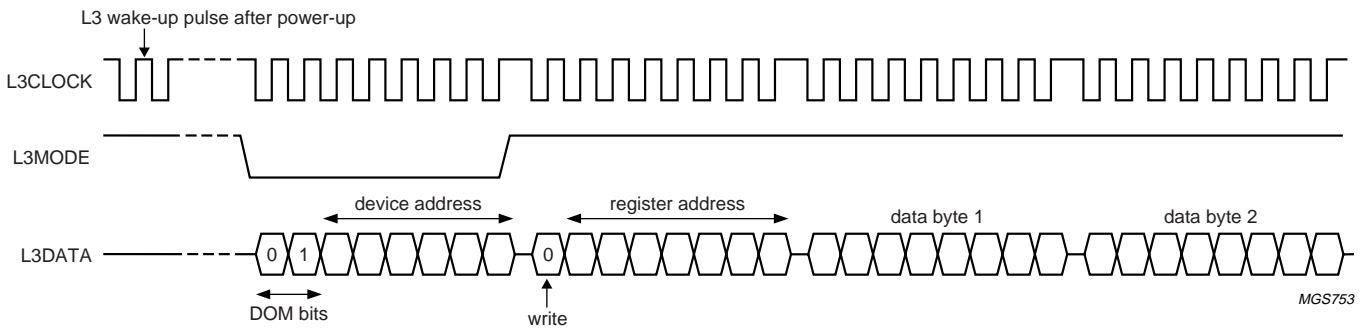


Fig.9 Data write mode for L3-bus version 2.

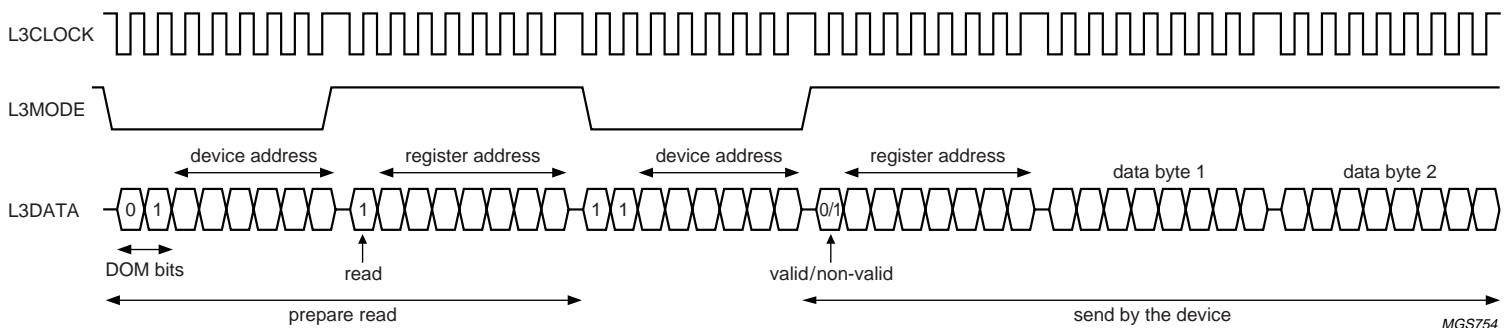


Fig.10 Data read mode for L3-bus version 2.

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**8.16 I<sup>2</sup>C-bus interface**

Besides the L3-bus mode the UDA1342TS supports the I<sup>2</sup>C-bus mode; all the features can be controlled by the microcontroller with the same register addresses as used in the L3-bus mode.

The exchange of data and control information between the microcontroller and the UDA1342TS in the I<sup>2</sup>C-bus mode is accomplished through a serial hardware interface comprising the following pins and signals:

- L3CLOCK: Serial Clock Line (SCL)
- L3DATA: Serial Data line (SDA).

The clock and data timing of the I<sup>2</sup>C-bus transfer is shown in Fig.15.

**8.16.1 ADDRESSING**

Before any data is transmitted on the I<sup>2</sup>C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the START procedure (S).

**8.16.2 SLAVE ADDRESS**

The UDA1342TS acts as a slave receiver or a slave transmitter. Therefore, the clock signal SCL is only an input signal. The data signal SDA is an input or output signal (bidirectional line).

The UDA1342TS slave address format is shown in Table 15.

**Table 15** I<sup>2</sup>C-bus slave address format

| MSB | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB |
|-----|-------|-------|-------|-------|-------|-------|-----|
| 0   | 0     | 1     | 1     | 0     | 1     | IPSEL | R/W |

The slave address bit IPSEL corresponds to the hardware address pin IPSEL which allows selecting the slave address.

**8.16.3 REGISTER ADDRESS**

The UDA1342TS register address format is given in Table 16.

**Table 16** I<sup>2</sup>C-bus register address format

| MSB | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB |
|-----|-------|-------|-------|-------|-------|-------|-----|
| 0   | A6    | A5    | A4    | A3    | A2    | A1    | A0  |

The register mapping of the I<sup>2</sup>C-bus and L3-bus interfaces is the same (see Section 9).

## 8.16.4 WRITE CYCLE

The write cycle is used to write data from the microcontroller to the internal registers. The I<sup>2</sup>C-bus format for a write cycle is shown in Table 17.

The device and register addresses are one byte each, data is always two bytes (2-bytes data).

The format of the write cycle is as follows:

1. The microcontroller starts with a START condition S.
2. The first byte (8 bits) contains the device address 0011 01X and a write command (bit  $R/\overline{W}$  = 0).
3. This is followed by an acknowledge (A) from the UDA1342TS.
4. The microcontroller then writes the register address (8 bits) where writing of the register content of the UDA1342TS must start.
5. The UDA1342TS acknowledges this register address.
6. The microcontroller sends 2-bytes data with the Most Significant Data (MSD) byte first and then the Least Significant Data (LSD) byte, where each byte is acknowledged by the UDA1342TS.
7. After the last acknowledge the UDA1342TS frees the I<sup>2</sup>C-bus and the microcontroller can generate a STOP condition (P).

**Table 17** Master transmitter writes to UDA1342TS registers

|   |                | ACKNOWLEDGE FROM UDA1342TS |   |                  |   |                     |   |        |   |        |   |        |   |        |   |        |   |   |  |
|---|----------------|----------------------------|---|------------------|---|---------------------|---|--------|---|--------|---|--------|---|--------|---|--------|---|---|--|
|   | DEVICE ADDRESS | R/ $\overline{W}$          |   | REGISTER ADDRESS |   | DATA <sup>(1)</sup> |   |        |   |        |   |        |   |        |   |        |   |   |  |
| S | 0011 01X       | 0                          | A | 0XXX XXXX        | A | MSD1                | A | LSD1   | A | MSD2   | A | LSD2   | A | MSDn   | A | LSDn   | A | P |  |
|   | 8 bits         |                            |   | 8 bits           |   | 8 bits              |   | 8 bits |   | 8 bits |   | 8 bits |   | 8 bits |   | 8 bits |   |   |  |

**Note**

1. Auto increment of the register address is carried out if repeated groups of 2 bytes are transmitted.

## 8.16.5 READ CYCLE

The read cycle is used to read data from the internal registers of the UDA1342TS to the microcontroller. The I<sup>2</sup>C-bus format for a read cycle is shown in Table 18.

The format of the read cycle is as follows:

1. The microcontroller starts with a START condition S.
2. The first byte (8 bits) contains the device address 0011 01X and a write command (bit  $R/\bar{W} = 0$ ).
3. This is followed by an acknowledge (A) from the UDA1342TS.
4. The microcontroller then writes the register address where reading of the register content of the UDA1342TS must start.
5. The UDA1342TS acknowledges this register address.
6. Then the microcontroller generates a repeated START (Sr).
7. Again the device address 0011 01X is given, but this time followed by a read command (bit  $R/\bar{W} = 1$ ).
8. The UDA1342TS sends the two-byte data with the Most Significant Data (MSD) byte first and then the Least Significant Data (LSD) byte, where each byte is acknowledged by the microcontroller (master).
9. The microcontroller stops this cycle by generating a negative acknowledge (NA).
10. The UDA1342TS then frees the I<sup>2</sup>C-bus and the microcontroller can generate a STOP condition (P).

**Table 18** Master transmitter reads from UDA1342TS registers

|   |                |              | ACKNOWLEDGE FROM UDA1342TS |                  |   |    |                |              | ACKNOWLEDGE FROM MASTER |                     |   |        |   |        |   |        |   |        |   |        |    |   |
|---|----------------|--------------|----------------------------|------------------|---|----|----------------|--------------|-------------------------|---------------------|---|--------|---|--------|---|--------|---|--------|---|--------|----|---|
|   | DEVICE ADDRESS | R/ $\bar{W}$ |                            | REGISTER ADDRESS |   |    | DEVICE ADDRESS | R/ $\bar{W}$ |                         | DATA <sup>(1)</sup> |   |        |   |        |   |        |   |        |   |        |    |   |
| S | 0011 01X       | 0            | A                          | 0XXX XXXX        | A | Sr | 0011 01X       | 1            | A                       | MSD1                | A | LSD1   | A | MSD2   | A | LSD2   | A | MSDn   | A | LSDn   | NA | P |
|   | 8 bits         |              |                            | 8 bits           |   |    | 8 bits         |              |                         | 8 bits              |   | 8 bits |   | 8 bits |   | 8 bits |   | 8 bits |   | 8 bits |    |   |

**Note**

1. Auto increment of the register address is carried out if repeated groups of 2 bytes are transmitted.

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## 9 REGISTER MAPPING

The addresses of the control registers with default values at Power-on reset are shown in Table 19. Functions of the registers are shown in Tables 20 to 45.

**Table 19** Register map

| ADDRESS    | FUNCTION                           | D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|------------|------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 00H        | system                             | RST | QS  | MDC | DC  | AM2 | AM1 | AM0 | PAD | 0   | SC1 | SC0 | IF2 | IF1 | IF0 | DP  | PDA |
|            |                                    | –   | 0   | 0   | 1   | 1   | 0   | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| 01H        | sub system                         | –   | –   | –   | –   | –   | –   | –   | –   | OS1 | OS0 | MPS | MIX | SD1 | SD0 | MP1 | MP0 |
|            |                                    | –   | –   | –   | –   | –   | –   | –   | –   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 02H to 0FH | reserved                           | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   |
| 10H        | DAC features                       | M1  | M0  | BB3 | BB2 | BB1 | BB0 | TR1 | TR0 | SDS | MTB | MTA | MT  | QM  | DE2 | DE1 | DE0 |
|            |                                    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 11H        | DAC master volume                  | VL7 | VL6 | VL5 | VL4 | VL3 | VL2 | VL1 | VL0 | VR7 | VR6 | VR5 | VR4 | VR3 | VR2 | VR1 | VR0 |
|            |                                    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 12H        | DAC mixer volume                   | VB7 | VB6 | VB5 | VB4 | VB3 | VB2 | VB1 | VB0 | VA7 | VA6 | VA5 | VA4 | VA3 | VA2 | VA1 | VA0 |
|            |                                    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 13H to 1FH | reserved                           | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   |
| 20H        | ADC input and mixer gain channel 1 | 0   | 0   | 0   | 0   | IA3 | IA2 | IA1 | IA0 | MA7 | MA6 | MA5 | MA4 | MA3 | MA2 | MA1 | MA0 |
|            |                                    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 21H        | ADC input and mixer gain channel 2 | 0   | 0   | 0   | 0   | IB3 | IB2 | IB1 | IB0 | MB7 | MB6 | MB5 | MB4 | MB3 | MB2 | MB1 | MB0 |
|            |                                    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 22H to 2FH | reserved                           | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   |
| 30H        | evaluation                         | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 31H to FFH | reserved                           | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   | –   |

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**9.1 Reset**

A 1-bit value to initialize the L3-bus and I<sup>2</sup>C-bus registers except the system register (00H) with default settings by setting bit RST = 1.

**Table 20** Reset bit

| RST | FUNCTION                   |
|-----|----------------------------|
| 0   | no reset                   |
| 1   | reset registers to default |

**9.2 Quick mode switch**

A 1-bit value to enable the quick mode change of the ADC. The soft mode change works only between modes if bit AM2 = 1.

**Table 21** Quick mode switch

| QS | FUNCTION          |
|----|-------------------|
| 0  | soft mode change  |
| 1  | quick mode change |

**9.3 Bypass mixer DC filter**

A 1-bit value to disable the DC filter of the ADC mixer. This DC filter is in front of the mixer to prevent clipping inside the mixer due to DC signals.

**Table 22** Mixer DC filtering

| MDC | FUNCTION                   |
|-----|----------------------------|
| 0   | enable mixer DC filtering  |
| 1   | disable mixer DC filtering |

**9.4 DC filter**

A 1-bit value to enable the DC filter of the ADC output. This DC filter is inside the decimation filter.

**Table 23** DC-filtering

| DC | FUNCTION                    |
|----|-----------------------------|
| 0  | disable output DC filtering |
| 1  | enable output DC filtering  |

**9.5 ADC mode**

A 3-bit value to select the mode of the ADC.

**Table 24** ADC mode

| AM2 | AM1 | AM0 | FUNCTION                                  |
|-----|-----|-----|---|
| 0   | 0   | 0   | ADC power-off                             |
| 0   | 0   | 1   | input 1 select (input 2 off)              |
| 0   | 1   | 0   | input 2 select (input 1 off)              |
| 0   | 1   | 1   | not used                                  |
| 1   | 0   | 0   | channel swap and signal inversion         |
| 1   | 0   | 1   | input 1 select (double differential mode) |
| 1   | 1   | 0   | input 2 select (double differential mode) |
| 1   | 1   | 1   | mixing mode                               |

**9.6 ADC polarity**

A 1-bit value to control the ADC polarity.

**Table 25** Polarity control of the ADC

| PAD | FUNCTION      |
|-----|---------------|
| 0   | non-inverting |
| 1   | inverting     |

**9.7 System clock frequency**

A 2-bit value to select the external clock frequency.

**Table 26** System clock frequency settings

| SC1 | SC0 | FUNCTION          |
|-----|-----|-------------------|
| 0   | 0   | 256f <sub>s</sub> |
| 0   | 1   | 384f <sub>s</sub> |
| 1   | 0   | 512f <sub>s</sub> |
| 1   | 1   | 768f <sub>s</sub> |

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## 9.8 Data format

A 3-bit value to select the data format.

**Table 27** Data format selection

| IF2 | IF1 | IF0 | FUNCTION   |
|-----|-----|-----|--|
| 0   | 0   | 0   | I <sup>2</sup> S-bus                                 |
| 0   | 0   | 1   | LSB-justified 16 bits                                |
| 0   | 1   | 0   | LSB-justified 20 bits                                |
| 0   | 1   | 1   | LSB-justified 24 bits                                |
| 1   | 0   | 0   | MSB-justified  |
| 1   | 0   | 1   | LSB-justified 16 bits input and MSB-justified output |
| 1   | 1   | 0   | LSB-justified 20 bits input and MSB-justified output |
| 1   | 1   | 1   | LSB-justified 24 bits input and MSB-justified output |

## 9.9 DAC power control

A 1-bit value to disable the DAC to reduce power consumption. The DAC power-off is not recommended when the DAC outputs are DC loaded.

**Table 28** DAC power control

| DP | FUNCTION      |
|----|---------------|
| 0  | DAC power-off |
| 1  | DAC power-on  |

## 9.10 Input oversampling rate

A 2-bit value to select the oversampling rate of the input signal (see Table 32). In the quad speed input rate, care must be taken that the input signal is smaller than -5.67 dB (FS).

**Table 32** Input oversampling rate

| OS1 | OS0 | MODE         | SAMPLING FREQUENCY | ADC           | DAC FEATURES  |
|-----|-----|--------------|--------------------|---------------|---|
| 0   | 0   | single speed | 16 to 110 kHz      | supported     | all digital filters and all features, including mixing are available                        |
| 0   | 1   | double speed | 32 to 220 kHz      | not supported | first digital filter is bypassed, only master volume and master mute features are available |
| 1   | 0   | quad speed   | 64 to 440 kHz      | not supported | no mixing nor any sound feature is supported  |
| 1   | 1   | reserved     | –                  | –             | –   |

## 9.11 DAC polarity

A 1-bit value to control the DAC polarity.

**Table 29** Polarity control of DAC

| PDA | FUNCTION      |
|-----|---------------|
| 0   | non-inverting |
| 1   | inverting     |

## 9.12 DAC mixing position switch

A 1-bit value to select the mixing position of the ADC signal in the DAC.

**Table 30** DAC mixing position switch

| MPS | FUNCTION              |
|-----|-----------------------|
| 0   | before sound features |
| 1   | after sound features  |

## 9.13 DAC mixer

A 1-bit value to enable the digital mixer of the DAC.

**Table 31** DAC mixer

| MIX | FUNCTION      |
|-----|---------------|
| 0   | disable mixer |
| 1   | enable mixer  |

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**9.14 Silence detection period**

A 2-bit value to define the silence period for the silence detector.

**Table 33** Silence detection period

| SD1 | SD0 | FUNCTION      |
|-----|-----|---------------|
| 0   | 0   | 3200 samples  |
| 0   | 1   | 4800 samples  |
| 1   | 0   | 9600 samples  |
| 1   | 1   | 19200 samples |

**9.15 Multi purpose output**

A 2-bit value to select the output signal on pin STATUS.

**Table 34** Multi purpose output selection

| MP1 | MP0 | FUNCTION                  |
|-----|-----|---------------------------|
| 0   | 0   | no output                 |
| 0   | 1   | overflow (ADC) detection  |
| 1   | 0   | reserved                  |
| 1   | 1   | digital silence detection |

**9.16 Mode**

A 2-bit value to program the mode of the sound processing filters of bass boost and treble.

**Table 35** Flat/min./max. switch position

| M1 | M0 | FUNCTION |
|----|----|----------|
| 0  | 0  | flat     |
| 0  | 1  | min.     |
| 1  | 0  | min.     |
| 1  | 1  | max.     |

**9.17 Bass boost**

A 4-bit value to program the bass boost settings. The used set depends on the setting of bits M1 and M0.

At  $f_s = 44.1$  kHz the  $-3$  dB point for minimum setting is 250 Hz and the  $-3$  dB point for maximum setting is 300 Hz. The default value is 0000.

**Table 36** Bass boost settings

| BB3 | BB2 | BB1 | BB0 | BASS BOOST (dB) |      |      |
|-----|-----|-----|-----|-----------------|------|------|
|     |     |     |     | FLAT            | MIN. | MAX. |
| 0   | 0   | 0   | 0   | 0               | 0    | 0    |
| 0   | 0   | 0   | 1   | 0               | 2    | 2    |
| 0   | 0   | 1   | 0   | 0               | 4    | 4    |
| 0   | 0   | 1   | 1   | 0               | 6    | 6    |
| 0   | 1   | 0   | 0   | 0               | 8    | 8    |
| 0   | 1   | 0   | 1   | 0               | 10   | 10   |
| 0   | 1   | 1   | 0   | 0               | 12   | 12   |
| 0   | 1   | 1   | 1   | 0               | 14   | 14   |
| 1   | 0   | 0   | 0   | 0               | 16   | 16   |
| 1   | 0   | 0   | 1   | 0               | 18   | 18   |
| 1   | 0   | 1   | 0   | 0               | 18   | 20   |
| 1   | 0   | 1   | 1   | 0               | 18   | 22   |
| 1   | 1   | 0   | 0   | 0               | 18   | 24   |
| 1   | 1   | 0   | 1   | 0               | 18   | 24   |
| 1   | 1   | 1   | 0   | 0               | 18   | 24   |
| 1   | 1   | 1   | 1   | 0               | 18   | 24   |

**9.18 Treble**

A 2-bit value to program the treble setting. The used set depends on the setting of bits M1 and M0. At  $f_s = 44.1$  kHz the  $-3$  dB point for minimum setting is 3.0 kHz and the  $-3$  dB point for maximum setting is 1.5 kHz. The default value is 00.

**Table 37** Treble settings

| TR1 | TR0 | TREBLE (dB) |      |      |
|-----|-----|-------------|------|------|
|     |     | FLAT        | MIN. | MAX. |
| 0   | 0   | 0           | 0    | 0    |
| 0   | 1   | 0           | 2    | 2    |
| 1   | 0   | 0           | 4    | 4    |
| 1   | 1   | 0           | 6    | 6    |



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### 9.19 Silence detector switch

A 1-bit value to enable the silence detector.

**Table 38** Silence detector switch

| SDS | FUNCTION                 |
|-----|--------------------------|
| 0   | disable silence detector |
| 1   | enable silence detector  |

### 9.20 Mute

Three 1-bit values to enable the digital mute. Bit MT is the master mute, using bit MTA the signal from the digital interface can be soft muted when the DAC mixer is enabled and using bit MTB the signal from ADC can be soft muted.

**Table 39** Mute

| MT<br>MTA<br>MTB | FUNCTION  |
|------------------|-----------|
| 0                | no muting |
| 1                | muting    |

### 9.21 Quick mute mode

A 1-bit value to enable the quick mute function of the master mute.

**Table 40** Quick mute mode settings

| QM | FUNCTION        |
|----|-----------------|
| 0  | soft mute mode  |
| 1  | quick mute mode |

### 9.22 De-emphasis

A 3-bit value to enable the digital de-emphasis filter.

**Table 41** De-emphasis settings

| DE2 | DE1 | DE0 | FUNCTION                        |
|-----|-----|-----|---------------------------------|
| 0   | 0   | 0   | no de-emphasis                  |
| 0   | 0   | 1   | de-emphasis at $f_s = 32$ kHz   |
| 0   | 1   | 0   | de-emphasis at $f_s = 44.1$ kHz |
| 0   | 1   | 1   | de-emphasis at $f_s = 48$ kHz   |
| 1   | 0   | 0   | de-emphasis at $f_s = 96$ kHz   |

### 9.23 ADC input amplifier gain

Two 4-bit values to program the gain of the input amplifiers. Bits IA applies for input amplifier A and bits IB to input amplifier B.

**Table 42** ADC input amplifier gain settings

| IA3<br>IB3 | IA2<br>IB2 | IA1<br>IB1 | IA0<br>IB0 | AMPLIFIER GAIN (dB) |
|------------|------------|------------|------------|---------------------|
| 0          | 0          | 0          | 0          | 0                   |
| 0          | 0          | 0          | 1          | 3                   |
| 0          | 0          | 1          | 0          | 6                   |
| 0          | 0          | 1          | 1          | 9                   |
| 0          | 1          | 0          | 0          | 12                  |
| 0          | 1          | 0          | 1          | 15                  |
| 0          | 1          | 1          | 0          | 18                  |
| 0          | 1          | 1          | 1          | 21                  |
| 1          | 0          | 0          | 0          | 24                  |

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**9.24 DAC volume control**

Four 8-bit values to program the volume attenuations. The range is from 0 to  $-66$  dB and  $-\infty$  dB in steps of 0.25 dB. Bits VL and VR are master volumes for the left and right channels.

**Table 43** DAC volume settings

| VL7<br>VR7 | VL6<br>VR6 | VL5<br>VR5 | VL4<br>VR4 | VL3<br>VR3 | VL2<br>VR2 | VL1<br>VR1 | VL0<br>VR0 | VOLUME (dB) |
|------------|------------|------------|------------|------------|------------|------------|------------|-------------|
| 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0           |
| 0          | 0          | 0          | 0          | 0          | 0          | 0          | 1          | -0.25       |
| 0          | 0          | 0          | 0          | 0          | 0          | 1          | 0          | -0.50       |
| 0          | 0          | 0          | 0          | 0          | 0          | 1          | 1          | -0.75       |
| 0          | 0          | 0          | 0          | 0          | 1          | 0          | 0          | -1.00       |
| :          | :          | :          | :          | :          | :          | :          | :          | :           |
| 1          | 1          | 0          | 0          | 0          | 1          | 0          | 0          | -49.0       |
| 1          | 1          | 0          | 0          | 0          | 1          | 0          | 1          | -49.25      |
| 1          | 1          | 0          | 0          | 0          | 1          | 1          | 0          | -49.5       |
| 1          | 1          | 0          | 0          | 0          | 1          | 1          | 1          | -49.75      |
| 1          | 1          | 0          | 0          | 1          | 0          | 0          | 0          | -50.0       |
| 1          | 1          | 0          | 0          | 1          | 1          | 0          | 0          | -52.0       |
| 1          | 1          | 0          | 1          | 0          | 0          | 0          | 0          | -54.0       |
| 1          | 1          | 0          | 1          | 0          | 1          | 0          | 0          | -57.0       |
| 1          | 1          | 0          | 1          | 1          | 0          | 0          | 0          | -60.0       |
| 1          | 1          | 0          | 1          | 1          | 1          | 0          | 0          | -66.0       |
| 1          | 1          | 1          | 0          | 0          | 0          | 0          | 0          | $-\infty$   |
| :          | :          | :          | :          | :          | :          | :          | :          | :           |
| 1          | 1          | 1          | 1          | 1          | 1          | 1          | 1          | $-\infty$   |

**9.25 DAC mixer volume control**

Four 8-bit values to program the volume attenuations. The range is from 0 to  $-60$  dB and  $-\infty$  dB in steps of 0.25 dB. When the DAC mixer is enabled, the signal from the digital interface can be controlled by bits VA and the signal from the ADC can be controlled by bits VB.

**Table 44** DAC volume settings

| VA7<br>VB7 | VA6<br>VB6 | VA5<br>VB5 | VA4<br>VB4 | VA3<br>VB3 | VA2<br>VB2 | VA1<br>VB1 | VA0<br>VB0 | VOLUME (dB) |
|------------|------------|------------|------------|------------|------------|------------|------------|-------------|
| 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0           |
| 0          | 0          | 0          | 0          | 0          | 0          | 0          | 1          | -0.25       |
| 0          | 0          | 0          | 0          | 0          | 0          | 1          | 0          | -0.50       |
| 0          | 0          | 0          | 0          | 0          | 0          | 1          | 1          | -0.75       |
| 0          | 0          | 0          | 0          | 0          | 1          | 0          | 0          | -1.00       |
| :          | :          | :          | :          | :          | :          | :          | :          | :           |
| 1          | 0          | 1          | 0          | 1          | 1          | 0          | 0          | -43.0       |
| 1          | 0          | 1          | 0          | 1          | 1          | 0          | 1          | -43.25      |

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| VA7<br>VB7 | VA6<br>VB6 | VA5<br>VB5 | VA4<br>VB4 | VA3<br>VB3 | VA2<br>VB2 | VA1<br>VB1 | VA0<br>VB0 | VOLUME (dB) |
|------------|------------|------------|------------|------------|------------|------------|------------|-------------|
| 1          | 0          | 1          | 0          | 1          | 1          | 1          | 0          | -43.5       |
| 1          | 0          | 1          | 0          | 1          | 1          | 1          | 1          | -43.75      |
| 1          | 0          | 1          | 1          | 0          | 0          | 0          | 0          | -44.0       |
| 1          | 0          | 1          | 1          | 0          | 1          | 0          | 0          | -46.0       |
| 1          | 0          | 1          | 1          | 1          | 0          | 0          | 0          | -48.0       |
| 1          | 0          | 1          | 1          | 1          | 1          | 0          | 0          | -51.0       |
| 1          | 1          | 0          | 0          | 0          | 0          | 0          | 0          | -54.0       |
| 1          | 1          | 0          | 0          | 0          | 1          | 0          | 0          | -60.0       |
| 1          | 1          | 0          | 0          | 1          | 0          | 0          | 0          | -∞          |
| :          | :          | :          | :          | :          | :          | :          | :          | :           |
| 1          | 1          | 1          | 1          | 1          | 1          | 1          | 1          | -∞          |

9.26 ADC mixer gain control

Two 8-bit values to program the channel 1 and 2 mixing, when the mixer mode is selected. Bits MA applies to channel 1 and bits MB to channel 2. The range is from +24 to -63.5 dB and -∞ dB in steps of 0.5 dB.

Table 45 ADC mixer gain settings

| MA7<br>MB7 | MA6<br>MB6 | MA5<br>MB5 | MA4<br>MB4 | MA3<br>MB3 | MA2<br>MB2 | MA1<br>MB1 | MA0<br>MB0 | MIXER GAIN (dB) |
|------------|------------|------------|------------|------------|------------|------------|------------|-----------------|
| 0          | 0          | 1          | 1          | 0          | 0          | 0          | 0          | +24.0           |
| 0          | 0          | 1          | 0          | 1          | 1          | 1          | 1          | +23.5           |
| 0          | 0          | 1          | 0          | 1          | 1          | 1          | 0          | +23.0           |
| :          | :          | :          | :          | :          | :          | :          | :          | :               |
| 0          | 0          | 0          | 0          | 0          | 0          | 1          | 0          | +1.0            |
| 0          | 0          | 0          | 0          | 0          | 0          | 0          | 1          | +0.5            |
| 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0               |
| 1          | 1          | 1          | 1          | 1          | 1          | 1          | 1          | -0.5            |
| :          | :          | :          | :          | :          | :          | :          | :          | :               |
| 1          | 0          | 0          | 0          | 0          | 1          | 0          | 0          | -62.0           |
| 1          | 0          | 0          | 0          | 0          | 0          | 1          | 1          | -62.5           |
| 1          | 0          | 0          | 0          | 0          | 0          | 1          | 0          | -63.0           |
| 1          | 0          | 0          | 0          | 0          | 0          | 0          | 1          | -63.5           |
| 1          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | -∞              |

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**10 LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL          | PARAMETER                      | CONDITIONS   | MIN.  | MAX.  | UNIT |
|-----------------|--------------------------------|--|-------|-------|------|
| $V_{DD}$        | supply voltage                 | note 1   | –     | 4     | V    |
| $T_{xtal(max)}$ | maximum crystal temperature    |  | –     | 150   | °C   |
| $T_{stg}$       | storage temperature            |  | –65   | +125  | °C   |
| $T_{amb}$       | ambient temperature            |  | –40   | +85   | °C   |
| $V_{es}$        | electrostatic handling voltage | note 2   | –1100 | +1100 | V    |
|                 |                                | note 3   | –250  | +250  | V    |
| $I_{lu(prot)}$  | latch-up protection current    | $T_{amb} = 125\text{ °C}; V_{DD} = 3.6\text{ V}$     | –     | 200   | mA   |
| $I_{sc(DAC)}$   | short-circuit current of DAC   | $T_{amb} = 0\text{ °C}; V_{DD} = 3\text{ V};$ note 4 |       |       |      |
|                 |                                | output short-circuited to $V_{SSA(DAC)}$             | –     | 450   | mA   |
|                 |                                | output short-circuited to $V_{DDA(DAC)}$             | –     | 325   | mA   |

**Notes**

1. All supply connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 k $\Omega$  series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 0.75  $\mu$ H series inductor.
4. DAC operation after short-circuiting cannot be warranted.

**11 HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

**12 QUALITY SPECIFICATION**

In accordance with “SNW-FQ-611-E”.

**13 THERMAL CHARACTERISTICS**

| SYMBOL        | PARAMETER                                   | CONDITIONS  | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 90    | K/W  |

**14 DC CHARACTERISTICS**

$V_{DDD} = V_{DDA(ADC)} = V_{DDA(DAC)} = 3.0\text{ V}; T_{amb} = 25\text{ °C}; R_L = 5\text{ k}\Omega;$  all voltages measured with respect to ground; unless otherwise specified.

| SYMBOL                  | PARAMETER                 | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-------------------------|---------------------------|------------|------|------|------|------|
| <b>Supplies; note 1</b> |                           |            |      |      |      |      |
| $V_{DDA(ADC)}$          | ADC analog supply voltage |            | 2.7  | 3.0  | 3.6  | V    |
| $V_{DDA(DAC)}$          | DAC analog supply voltage |            | 2.7  | 3.0  | 3.6  | V    |
| $V_{DDD}$               | digital supply voltage    |            | 2.7  | 3.0  | 3.6  | V    |

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| SYMBOL  | PARAMETER                                 | CONDITIONS                                     | MIN.                 | TYP.                  | MAX.                 | UNIT |
|---|---|--|----------------------|-----------------------|----------------------|------|
| I <sub>DDA(ADC)</sub>                                   | ADC analog supply current                 | 1 ADC + 1 PGA enabled                          | –                    | 10                    | –                    | mA   |
|   |   | 2 ADCs + 2 PGAs enabled                        | –                    | 20                    | –                    | mA   |
|   |   | all ADCs + all PGAs power-down                 | –                    | 200                   | –                    | μA   |
| I <sub>DDA(DAC)</sub>                                   | DAC analog supply current                 | operating                                      | –                    | 6.0                   | –                    | mA   |
|   |   | DAC power-down                                 | –                    | 250                   | –                    | μA   |
| I <sub>DDD</sub>  | digital supply current                    | operating                                      | –                    | 9.0                   | –                    | mA   |
|   |   | ADC power-down                                 | –                    | 4.5                   | –                    | mA   |
|   |   | DAC power-down                                 | –                    | 5.5                   | –                    | mA   |
| <b>Digital input pins (5 V tolerant TTL compatible)</b> |   |  |                      |                       |                      |      |
| V <sub>IH</sub>   | HIGH-level input voltage                  |  | 2.0                  | –                     | 5.5                  | V    |
| V <sub>IL</sub>   | LOW-level input voltage                   |  | –0.5                 | –                     | +0.8                 | V    |
| I <sub>LI</sub>   | input leakage current                     |  | –                    | –                     | 1                    | μA   |
| C <sub>i</sub>  | input capacitance                         |  | –                    | –                     | 10                   | pF   |
| <b>Digital output pins</b>                              |   |  |                      |                       |                      |      |
| V <sub>OH</sub>   | HIGH-level output voltage                 | I <sub>OH</sub> = –2 mA                        | 0.85V <sub>DDD</sub> | –                     | –                    | V    |
| V <sub>OL</sub>   | LOW-level output voltage                  | I <sub>OL</sub> = 2 mA                         | –                    | –                     | 0.4                  | V    |
| <b>Reference voltage</b>                                |   |  |                      |                       |                      |      |
| V <sub>ref</sub>  | reference voltage                         | with respect to V <sub>SSA(ADC)</sub> ; note 2 | 0.45V <sub>DDA</sub> | 0.5V <sub>DDA</sub>   | 0.55V <sub>DDA</sub> | V    |
| R <sub>O(Vref)</sub>                                    | output resistance on pin V <sub>ref</sub> |  | –                    | 5                     | –                    | kΩ   |
| <b>Analog-to-digital converter</b>                      |   |  |                      |                       |                      |      |
| V <sub>ADCP</sub>                                       | positive reference voltage of the ADC     |  | –                    | V <sub>DDA(ADC)</sub> | –                    | V    |
| V <sub>ADCN</sub>                                       | negative reference voltage of the ADC     |  | –                    | 0.0                   | –                    | V    |
| R <sub>i</sub>  | input resistance                          |  | –                    | 10                    | –                    | kΩ   |
| C <sub>i</sub>  | input capacitance                         |  | –                    | 24                    | –                    | pF   |
| <b>Digital-to-analog converter</b>                      |   |  |                      |                       |                      |      |
| I <sub>o(max)</sub>                                     | maximum output current                    | (THD + N)/S < 0.1%                             | –                    | 1.6                   | –                    | mA   |
| R <sub>L</sub>  | load resistance                           |  | 3                    | –                     | –                    | kΩ   |
| C <sub>L</sub>  | load capacitance                          | note 3   | –                    | –                     | 50                   | pF   |

**Notes**

1. All supply connections must be made to the same power supply unit.
2. V<sub>DDA</sub> = V<sub>DDA(DAC)</sub> = V<sub>DDA(ADC)</sub>.
3. When higher capacitive loads must be driven, a 100 Ω resistor must be connected in series with the DAC output in order to prevent oscillations in the output operational amplifier.

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## 15 AC CHARACTERISTICS

$V_{DD} = V_{DDA(ADC)} = V_{DDA(DAC)} = 3.0\text{ V}$ ;  $f_i = 1\text{ kHz}$  at  $-1\text{ dB}$ ;  $T_{amb} = 25\text{ °C}$ ;  $R_L = 5\text{ k}\Omega$ ; all voltages measured with respect to ground; unless otherwise specified.

| SYMBOL                             | PARAMETER   | CONDITIONS                                      | MIN. | TYP.  | MAX. | UNIT |  |
|------------------------------------|---|---|------|-------|------|------|--|
| <b>Analog-to-digital converter</b> |   |   |      |       |      |      |  |
| $V_{i(rms)}$                       | input voltage<br>(RMS value)  | 0 dB setting                                    | –    | 900   | –    | mV   |  |
|                                    |   | 3 dB setting                                    | –    | 640   | –    | mV   |  |
|                                    |   | 6 dB setting                                    | –    | 450   | –    | mV   |  |
|                                    |   | 9 dB setting                                    | –    | 320   | –    | mV   |  |
|                                    |   | 12 dB setting                                   | –    | 225   | –    | mV   |  |
|                                    |   | 15 dB setting                                   | –    | 160   | –    | mV   |  |
|                                    |   | 18 dB setting                                   | –    | 122.5 | –    | mV   |  |
|                                    |   | 21 dB setting                                   | –    | 80    | –    | mV   |  |
|                                    |   | 24 dB setting                                   | –    | 61.25 | –    | mV   |  |
| $\Delta V_i$                       | unbalance between channels  |   | –    | <0.1  | –    | dB   |  |
| $(THD + N)/S_{48}$                 | total harmonic distortion-plus-noise to signal ratio at $f_s = 48\text{ kHz}$ | normal mode; at $-1\text{ dB}$                  |      |       |      |      |  |
|                                    |   | 0 dB setting                                    | –    | –90   | –    | dB   |  |
|                                    |   | 3 dB setting                                    | –    | –90   | –    | dB   |  |
|                                    |   | 6 dB setting                                    | –    | –90   | –    | dB   |  |
|                                    |   | 9 dB setting                                    | –    | –90   | –    | dB   |  |
|                                    |   | 12 dB setting                                   | –    | –89   | –    | dB   |  |
|                                    |   | 15 dB setting                                   | –    | –89   | –    | dB   |  |
|                                    |   | 18 dB setting                                   | –    | –88   | –    | dB   |  |
|                                    |   | 21 dB setting                                   | –    | –87   | –    | dB   |  |
|                                    |   | 24 dB setting                                   | –    | –85   | –    | dB   |  |
|                                    |   | normal mode; at $-60\text{ dB}$ ; A-weighted    |      |       |      |      |  |
|                                    |   | 0 dB setting                                    | –    | –40   | –    | dB   |  |
|                                    |   | 3 dB setting                                    | –    | –37   | –    | dB   |  |
|                                    |   | 6 dB setting                                    | –    | –36   | –    | dB   |  |
|                                    |   | 9 dB setting                                    | –    | –35   | –    | dB   |  |
|                                    |   | 12 dB setting                                   | –    | –33   | –    | dB   |  |
|                                    |   | 15 dB setting                                   | –    | –31   | –    | dB   |  |
|                                    |   | 18 dB setting                                   | –    | –30   | –    | dB   |  |
|                                    |   | 21 dB setting                                   | –    | –28   | –    | dB   |  |
|                                    |   | 24 dB setting                                   | –    | –26   | –    | dB   |  |
|                                    |   | double differential mode                        |      |       |      |      |  |
|                                    |   | at 0 dB gain                                    | –    | –93   | –    | dB   |  |
|                                    |   | at 0 dB gain; $-60\text{ dB}$ input; A-weighted | –    | –41   | –    | dB   |  |

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| SYMBOL                             | PARAMETER   | CONDITIONS   | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|---|--|------|------|------|------|
| (THD + N)/S <sub>96</sub>          | total harmonic distortion-plus-noise to signal ratio at f <sub>s</sub> = 96 kHz | normal mode  | –    | –84  | –    | dB   |
|                                    |   | at 0 dB gain<br>at –60 dB; A-weighted                          | –    | –39  | –    | dB   |
| S/N <sub>48</sub>                  | signal-to-noise ratio at f <sub>s</sub> = 48 kHz                                | V <sub>i</sub> = 0 V; A-weighted<br>normal mode                | –    | 100  | –    | dB   |
|                                    |   | double differential mode                                       | –    | 101  | –    | dB   |
| S/N <sub>96</sub>                  | signal-to-noise ratio at f <sub>s</sub> = 96 kHz                                | V <sub>i</sub> = 0 V; A-weighted; normal mode                  | –    | 99   | –    | dB   |
| α <sub>CS</sub>                    | channel separation  |  | –    | 100  | –    | dB   |
| PSRR                               | power supply rejection ratio  | f <sub>ripple</sub> = 1 kHz; V <sub>ripple</sub> = 30 mV (p-p) | –    | 30   | –    | dB   |
| <b>Digital-to-analog converter</b> |   |  |      |      |      |      |
| V <sub>o(rms)</sub>                | output voltage (RMS value)  | at 0 dB (FS) digital input                                     | –    | 0.9  | –    | V    |
| ΔV <sub>o</sub>                    | unbalance between channels  |  | –    | <0.1 | –    | dB   |
| (THD+N)/S <sub>48</sub>            | total harmonic distortion-plus-noise to signal ratio at f <sub>s</sub> = 48 kHz | at 0 dB  | –    | –90  | –    | dB   |
|                                    |   | at –60 dB; A-weighted  | –    | –40  | –    | dB   |
| (THD+N)/S <sub>96</sub>            | total harmonic distortion-plus-noise to signal ratio at f <sub>s</sub> = 96 kHz | at 0 dB  | –    | –83  | –    | dB   |
|                                    |   | at –60 dB; A-weighted  | –    | –39  | –    | dB   |
| S/N <sub>48</sub>                  | signal-to-noise ratio at f <sub>s</sub> = 48 kHz                                | code = 0; A-weighted   | –    | 100  | –    | dB   |
| S/N <sub>96</sub>                  | signal-to-noise at f <sub>s</sub> = 96 kHz                                      | code = 0; A-weighted   | –    | 99   | –    | dB   |
| α <sub>CS</sub>                    | channel separation  |  | –    | 100  | –    | dB   |
| PSRR                               | power supply rejection ratio  | f <sub>ripple</sub> = 1 kHz; V <sub>ripple</sub> = 30 mV (p-p) | –    | 60   | –    | dB   |

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**16 TIMING**

$V_{DD} = V_{DDA(ADC)} = V_{DDA(DAC)} = 2.7$  to  $3.6$  V;  $T_{amb} = -20$  to  $+85$  °C; all voltages referenced to ground; unless otherwise specified.

| SYMBOL  | PARAMETER                                | CONDITIONS                                       | MIN.         | TYP. | MAX.                     | UNIT |
|---|--|--|--------------|------|--------------------------|------|
| <b>System clock timing; note 1 (see Fig.11)</b>               |  |  |              |      |                          |      |
| $T_{sys}$   | system clock cycle time                  | $f_{sys} = 256f_s$                               | 35           | 81   | 250                      | ns   |
|   |  | $f_{sys} = 384f_s$                               | 23           | 54   | 170                      | ns   |
|   |  | $f_{sys} = 512f_s$                               | 17           | 41   | 130                      | ns   |
|   |  | $f_{sys} = 768f_s$                               | 17           | 27   | 90                       | ns   |
| $t_{CWL}$   | system clock LOW time                    | $f_{sys} < 19.2$ MHz                             | $0.3T_{sys}$ | –    | $0.7T_{sys}$             | ns   |
|   |  | $f_{sys} \geq 19.2$ MHz                          | $0.4T_{sys}$ | –    | $0.6T_{sys}$             | ns   |
| $t_{CWH}$   | system clock HIGH time                   | $f_{sys} < 19.2$ MHz                             | $0.3T_{sys}$ | –    | $0.7T_{sys}$             | ns   |
|   |  | $f_{sys} \geq 19.2$ MHz                          | $0.4T_{sys}$ | –    | $0.6T_{sys}$             | ns   |
| <b>Serial interface input/output data timing (see Fig.12)</b> |  |  |              |      |                          |      |
| $f_{BCK}$   | bit clock frequency                      |  | –            | –    | $128f_s$                 | Hz   |
| $T_{cy(BCK)}$   | bit clock cycle time                     | $T_{cy(s)} = \text{sample frequency cycle time}$ | –            | –    | $\frac{1}{128}T_{cy(s)}$ | s    |
| $t_{BCKH}$  | bit clock HIGH time                      |  | 30           | –    | –                        | ns   |
| $t_{BCKL}$  | bit clock LOW time                       |  | 30           | –    | –                        | ns   |
| $t_r$   | rise time                                |  | –            | –    | 20                       | ns   |
| $t_f$   | fall time                                |  | –            | –    | 20                       | ns   |
| $t_{su(WS)}$  | word select set-up time                  |  | 10           | –    | –                        | ns   |
| $t_{h(WS)}$   | word select hold time                    |  | 10           | –    | –                        | ns   |
| $t_{su(DATAI)}$   | data input set-up time                   |  | 10           | –    | –                        | ns   |
| $t_{h(DATAI)}$  | data input hold time                     |  | 10           | –    | –                        | ns   |
| $t_{h(DATAO)}$  | data output hold time                    |  | 0            | –    | –                        | ns   |
| $t_d(DATAO-BCK)$  | data output to bit clock delay           |  | –            | –    | 30                       | ns   |
| $t_d(DATAO-WS)$   | data output to word select delay         |  | –            | –    | 30                       | ns   |
| <b>L3-bus interface timing (see Figs 13 and 14)</b>           |  |  |              |      |                          |      |
| $t_r$   | rise time                                | note 2   | –            | –    | 10                       | ns/V |
| $t_f$   | fall time                                | note 2   | –            | –    | 10                       | ns/V |
| $T_{cy(CLK)L3}$   | L3CLOCK cycle time                       | note 3   | 500          | –    | –                        | ns   |
| $t_{CLK(L3)H}$  | L3CLOCK HIGH time                        |  | 250          | –    | –                        | ns   |
| $t_{CLK(L3)L}$  | L3CLOCK LOW time                         |  | 250          | –    | –                        | ns   |
| $t_{su(L3)A}$   | L3MODE set-up time in address mode       |  | 190          | –    | –                        | ns   |
| $t_{h(L3)A}$  | L3MODE hold time in address mode         |  | 190          | –    | –                        | ns   |
| $t_{su(L3)D}$   | L3MODE set-up time in data transfer mode |  | 190          | –    | –                        | ns   |
| $t_{h(L3)D}$  | L3MODE hold time in data transfer mode   |  | 190          | –    | –                        | ns   |



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| SYMBOL  | PARAMETER  | CONDITIONS | MIN.                   | TYP. | MAX. | UNIT          |
|---|--|------------|------------------------|------|------|---------------|
| $t_{\text{stp(L3)}}$                                    | L3MODE stop time in data transfer mode               |            | 190                    | –    | –    | ns            |
| $t_{\text{su(L3)DA}}$                                   | L3DATA set-up time in address and data transfer mode |            | 190                    | –    | –    | ns            |
| $t_{\text{h(L3)DA}}$                                    | L3DATA hold time in address and data transfer mode   |            | 30                     | –    | –    | ns            |
| $t_{\text{su(L3)R}}$                                    | L3DATA set-up time for read data                     |            | 50                     | –    | –    | ns            |
| $t_{\text{h(L3)R}}$                                     | L3DATA hold time for read data                       |            | 360                    | –    | –    | ns            |
| $t_{\text{en(L3)R}}$                                    | L3DATA enable time for read data                     |            | 380                    | –    | –    | ns            |
| $t_{\text{dis(L3)R}}$                                   | L3DATA disable time for read data                    |            | 50                     | –    | –    | ns            |
| <b>I<sup>2</sup>C-bus interface timing</b> (see Fig.15) |  |            |                        |      |      |               |
| $f_{\text{SCL}}$  | SCL clock frequency                                  |            | 0                      | –    | 400  | kHz           |
| $t_{\text{LOW}}$  | SCL LOW time   |            | 1.3                    | –    | –    | $\mu\text{s}$ |
| $t_{\text{HIGH}}$                                       | SCL HIGH time  |            | 0.6                    | –    | –    | $\mu\text{s}$ |
| $t_{\text{r}}$  | rise time SDA and SCL                                | note 4     | $20 + 0.1C_{\text{b}}$ | –    | 300  | ns            |
| $t_{\text{f}}$  | fall time SDA and SCL                                | note 4     | $20 + 0.1C_{\text{b}}$ | –    | 300  | ns            |
| $t_{\text{HD;STA}}$                                     | hold time START condition                            | note 5     | 0.6                    | –    | –    | $\mu\text{s}$ |
| $t_{\text{SU;STA}}$                                     | set-up time repeated START                           |            | 0.6                    | –    | –    | $\mu\text{s}$ |
| $t_{\text{SU;STO}}$                                     | set-up time STOP condition                           |            | 0.6                    | –    | –    | $\mu\text{s}$ |
| $t_{\text{BUF}}$  | bus free time between a STOP and START condition     |            | 1.3                    | –    | –    | $\mu\text{s}$ |
| $t_{\text{SU;DAT}}$                                     | data set-up time                                     |            | 100                    | –    | –    | ns            |
| $t_{\text{HD;DAT}}$                                     | data hold time                                       |            | 0                      | –    | –    | $\mu\text{s}$ |
| $t_{\text{SP}}$   | pulse width of spikes                                | note 6     | 0                      | –    | 50   | ns            |
| $C_{\text{b}}$  | capacitive load for each bus line                    |            | –                      | –    | 400  | pF            |

**Notes**

1. The typical value of the timing is specified at 48 kHz sampling frequency.
2. In order to prevent digital noise interfering with the L3-bus communication, it is best to have the rise and fall times as small as possible.
3. When the sampling frequency is below 32 kHz, the L3CLOCK cycle must be limited to  $\frac{1}{64f_{\text{s}}}$  cycle.
4.  $C_{\text{b}}$  is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
5. After this period, the first clock pulse is generated.
6. To be suppressed by the input filter.

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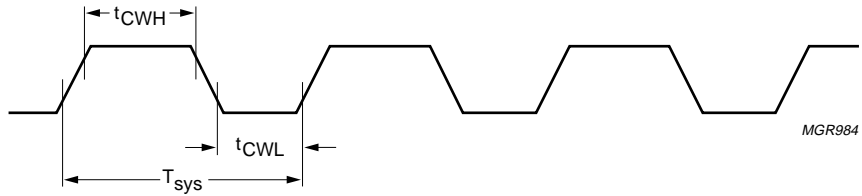


Fig.11 Timing of system clock.

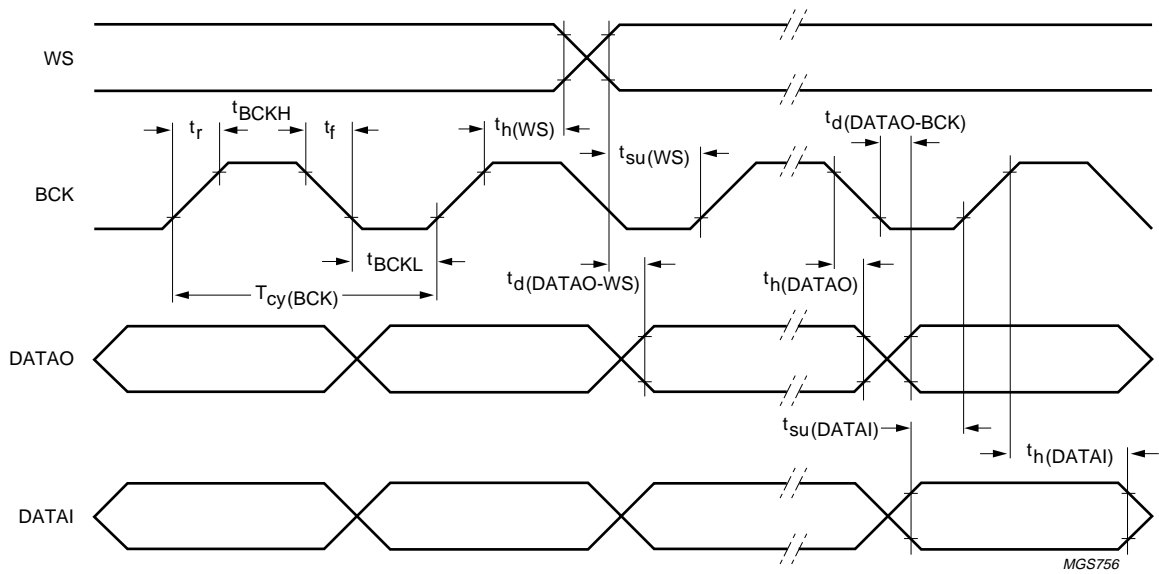


Fig.12 Serial interface input data timing.

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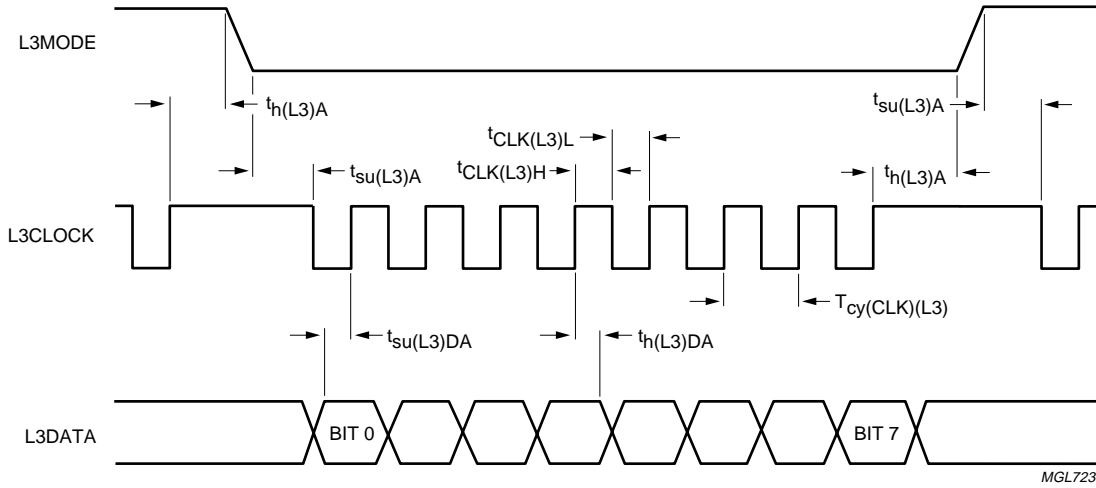


Fig.13 Timing of address mode.

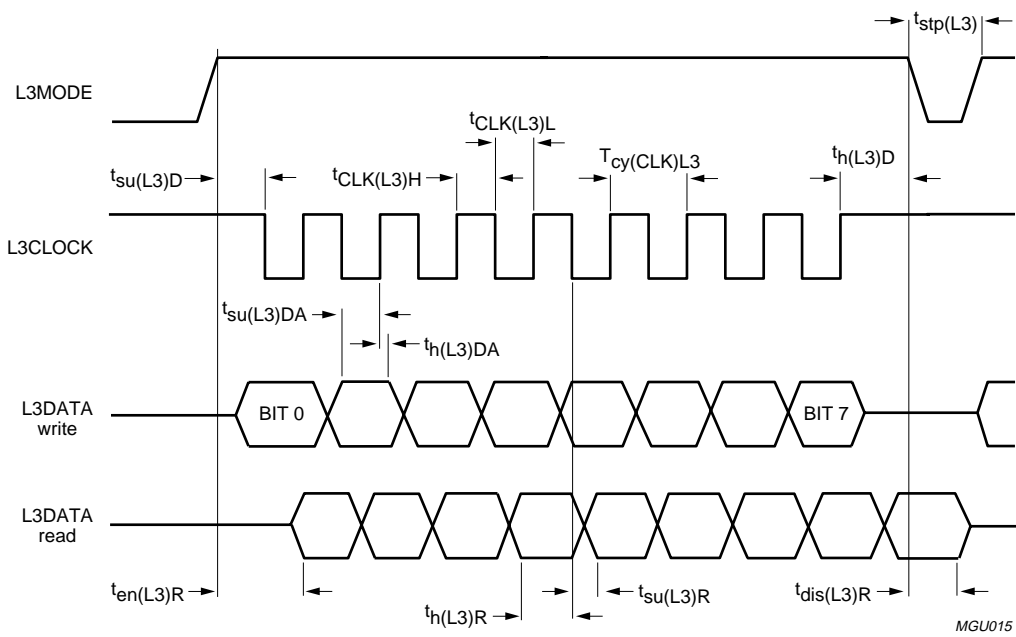


Fig.14 Timing of data transfer mode for write and read.

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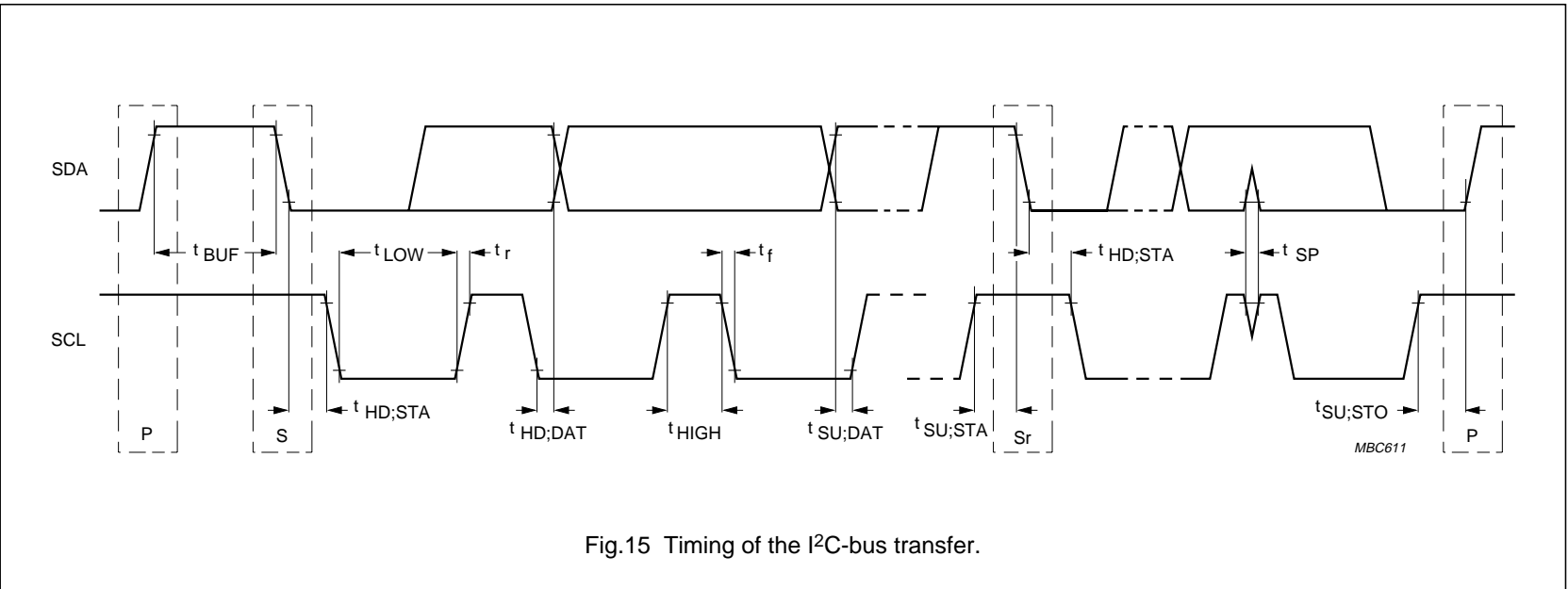


Fig.15 Timing of the I<sup>2</sup>C-bus transfer.

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17 APPLICATION INFORMATION

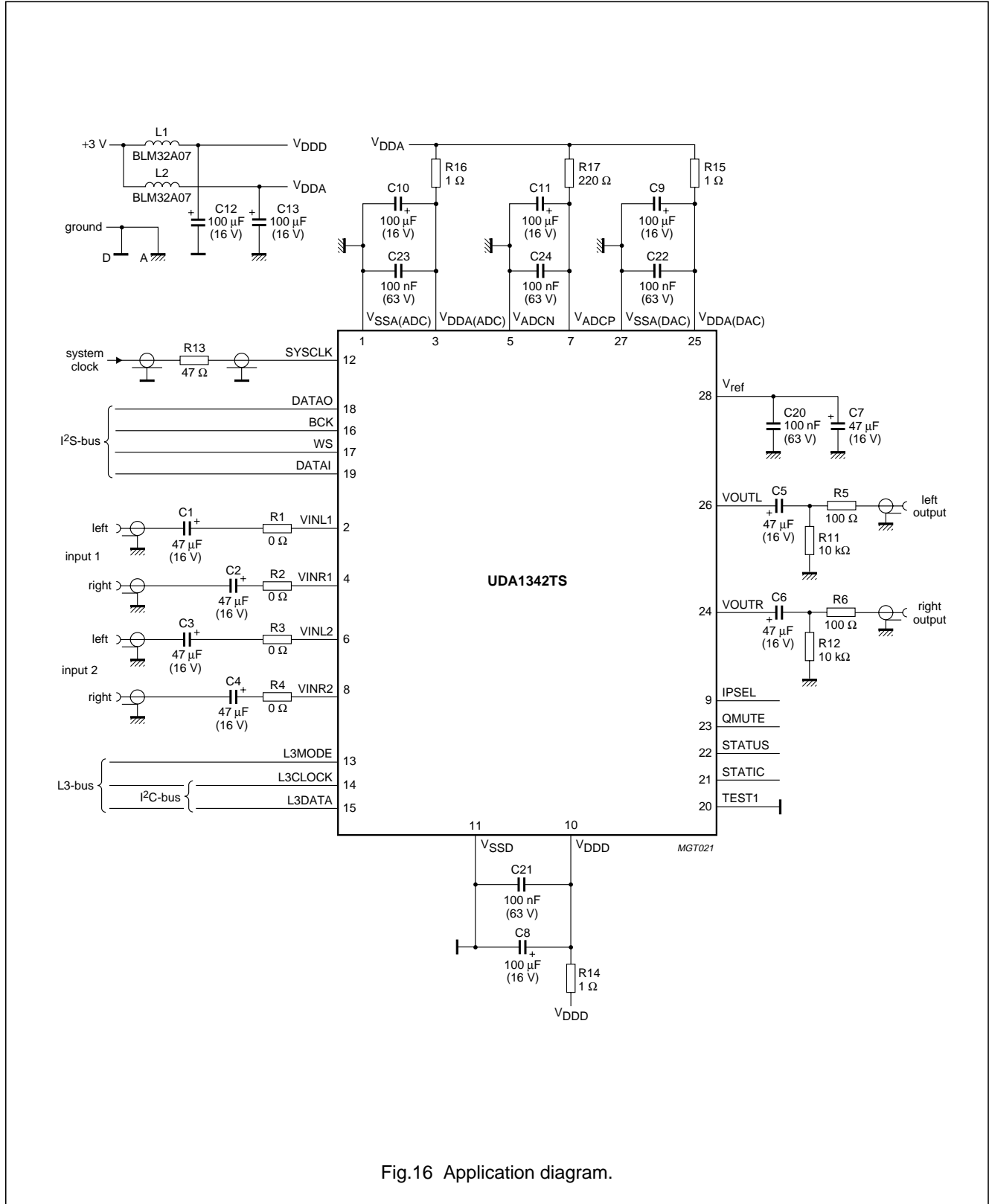


Fig.16 Application diagram.

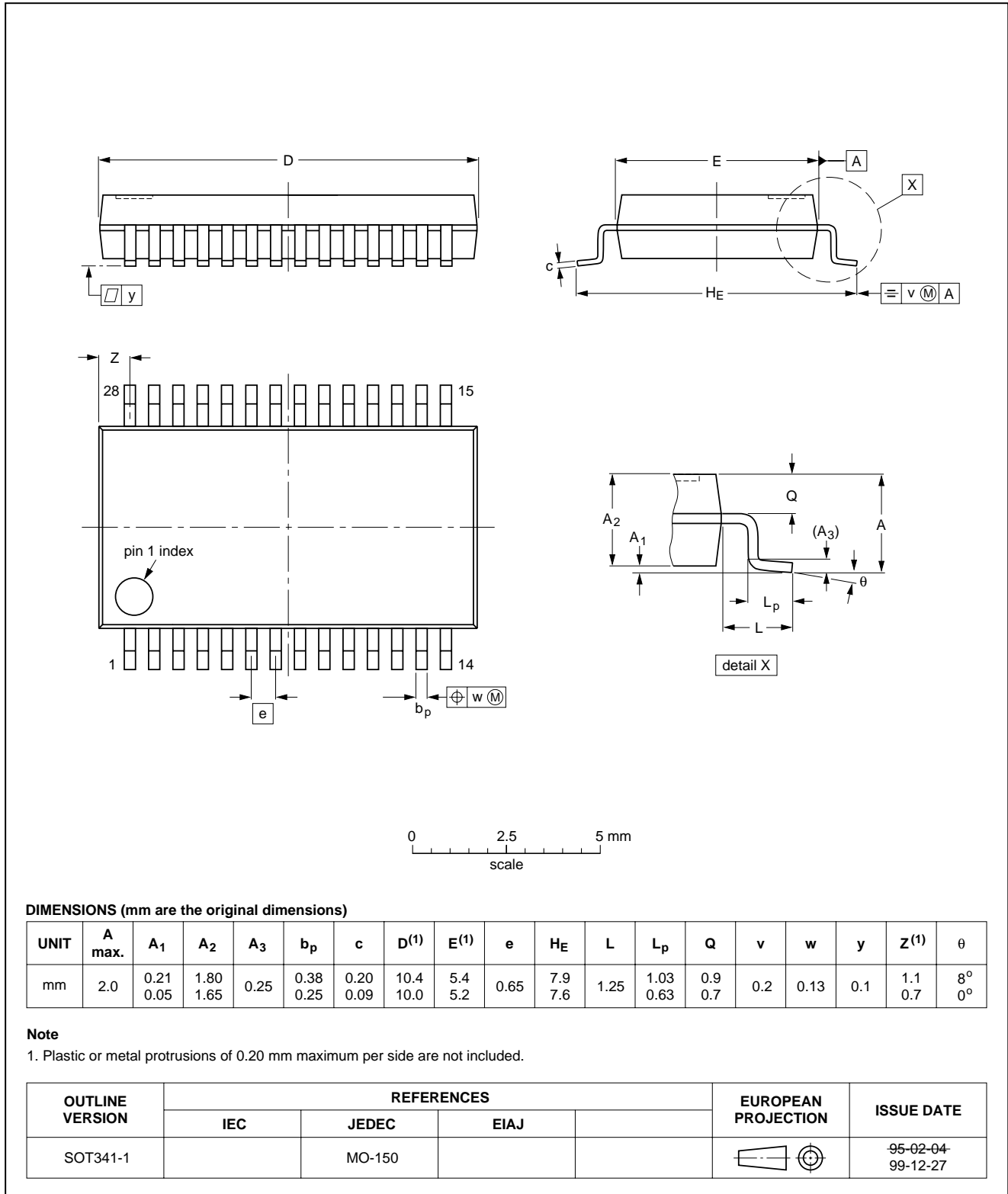
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18 PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm

SOT341-1



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### 19 SOLDERING

#### 19.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### 19.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### 19.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 19.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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19.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE                                      | SOLDERING METHOD                  |                       |
|--|-----------------------------------|-----------------------|
|  | WAVE                              | REFLOW <sup>(1)</sup> |
| BGA, LFBGA, SQFP, TFBGA                      | not suitable                      | suitable              |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS | not suitable <sup>(2)</sup>       | suitable              |
| PLCC <sup>(3)</sup> , SO, SOJ                | suitable                          | suitable              |
| LQFP, QFP, TQFP                              | not recommended <sup>(3)(4)</sup> | suitable              |
| SSOP, TSSOP, VSO                             | not recommended <sup>(5)</sup>    | suitable              |

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.



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## 20 DATA SHEET STATUS

| DATA SHEET STATUS         | PRODUCT STATUS | DEFINITIONS <sup>(1)</sup>   |
|---------------------------|----------------|--|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.  |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.   |

**Note**

1. Please consult the most recently issued data sheet before initiating or completing a design.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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**NOTES**

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## UDA1342TS

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### Datasheet

#### UDA1342TS

(Product Specification)  
31-Jul-00,44 Pages, 201  
kB

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## Audio CODEC

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### General description

The UDA1342TS is a single-chip 4 channel analog-to-digital converter and 2 channel digital-to-analog converter with signal processing features employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

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The UDA1342TS supports the I<sup>2</sup>S-bus data format with word lengths of up to 24 bits, the MSB-justified data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits. The device also supports a combination of the MSB-justified output format and the LSB-justified input format.

The UDA1342TS has special sound processing features in the playback mode such as de-emphasis, volume, mute, bass boost and treble, which can be controlled by the microcontroller via the L3-bus or I<sup>2</sup>C-bus interface.

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### Features

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2.7 to 3.6 V power supply  
5 V tolerant digital inputs  
High pin compatibility with UDA1341TS  
24 bits data path  
Selectable control via L3-bus interface, I<sup>2</sup>C-bus interface or static pin control; choice of 2 device addresses in L3-bus and I<sup>2</sup>C-bus mode  
Supports sample frequencies from 16 to 110 kHz  
Separate power control for ADC and DAC  
ADC and Programmable Gain Amplifiers (PGA) plus integrated high-pass filter to cancel DC offset  
Integrated digital filter plus DAC  
Digital silence detection

No analog post filtering required for DAC  
 Slave mode only applications  
 Easy application.

### Multiple format data interface

I<sup>2</sup>S-bus, MSB-justified and LSB-justified format compatible  
 1f<sub>s</sub> to 4f<sub>s</sub> input and 1f<sub>s</sub> output format data rate.

### DAC digital sound processing

Separate digital logarithmic volume control for left and right channels in L3-bus mode or I<sup>2</sup>C-bus mode  
 Digital tone control, bass boost and treble in L3-bus mode or I<sup>2</sup>C-bus mode  
 Digital de-emphasis for sample frequencies of 32, 44.1, 48 and 96 kHz in L3-bus mode or I<sup>2</sup>C-bus mode  
 Soft or quick mute in L3-bus mode or I<sup>2</sup>C-bus mode  
 Output signal polarity control in L3-bus mode or I<sup>2</sup>C-bus mode  
 Digital mixer for ADC output signal and digital serial input signal.







### Advanced audio configuration

4 channel (2 x stereo) single-ended inputs with programmable gain amplifiers and 2 channel (1 x stereo) single-ended outputs configuration  
 Output signal polarity control in L3-bus mode or I<sup>2</sup>C-bus mode  
 High linearity, wide dynamic range, low distortion  
 Double differential input configuration for enhanced ADC sound quality.

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### Products/packages

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| Type number  | North American Type number | Ordering code (12NC) | Product status    | Package           | Packing                 | Marking          | Chemical content   | Leadfree conversion date |
|--------------|----------------------------|----------------------|-------------------|-------------------|-------------------------|------------------|--|--------------------------|
| UDA1342TS/N1 | UDA1342TSDB                | 9352 629 09512       | Volume production | SOT341-1 (SSOP28) | Tube Dry Pack           | Standard Marking | UDA1342TS/N1    | week 18, 2005            |
| UDA1342TS/N1 | UDA1342TSDB-T              | 9352 629 09518       | Volume production | SOT341-1 (SSOP28) | Reel Dry Pack, SMD, 13" | Standard Marking | UDA1342TS/N1    | week 18, 2005            |

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### Pricing/ordering/availability

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| Type number  | Ordering code(12NC) | Indicative price/unit(\$) | Region | Distributor        | In stock | Inventory date | Buy online                 | Samples       |
|--------------|---------------------|---------------------------|--------|--------------------|----------|----------------|----------------------------|---------------|
| UDA1342TS/N1 | 9352 629 09512      |                           | NA     | MOUSER ELECTRONICS | 1,000    | 4/20/2008      | <a href="#">Buy online</a> | not available |

|              |                |  |    |                      |     |           |            |               |
|--------------|----------------|--|----|----------------------|-----|-----------|------------|---------------|
|              |                |  | NA | DIGI-KEY CORPORATION | 974 | 4/20/2008 | Buy online |               |
| UDA1342TS/N1 | 9352 629 09518 |  |    |                      |     |           |            | Order samples |

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## Applications

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Eminently suitable for MiniDisc (MD) home and portable applications.

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## Technical documents

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### Support Documents

75007723; Audio Dataconversion Ics (2001-11-23)

75014374\_ap; Audio Processing ()

75011122; P9xC557Ex 8-bit 80C51 with up to 64 Kbytes of internal program memory, 5 I/O ports and 10-bit ADC (2003-03-07)

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