Integrated Device Technology, Inc.

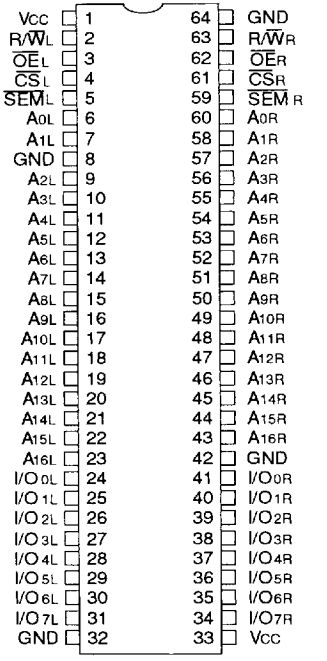
128K x 8
64K x 8
CMOS DUAL-PORT STATIC RAM MODULE

IDT7M1001
IDT7M1003

FEATURES

- High-density 1M/512K CMOS Dual-Port Static RAM module
- Fast access times:
  —Commercial 35, 40, 50, 65ns
  —Military 40, 50, 65, 80ns
- Fully asynchronous read/write operation from either port
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted LCC (leadless chip carriers) components on a 64-pin sidebraze DIP (Dual In-line Package)
- Multiple Vcc and GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Input/outputs directly TTL-compatible

PIN CONFIGURATION[1]



DIP
TOP VIEW

2804 drw 01

NOTE:
1. For the IDT7M1003 (64K x 8) version, Pins 23 & 43 must be connected to GND for proper operation of the module

DESCRIPTION:

The IDT7M1001/IDT7M1003 is a 128K x 8/64K x 8 high-speed CMOS Dual-Port Static RAM module constructed on a multilayer ceramic substrate using eight IDT7006 (16K x 8) Dual-Port RAMs and two IDT FCT138 decoders or depopulated using only four IDT7006s and two decoders.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via semaphore ($\overline{SEM}$) "handshake" signaling. The IDT7M1001/1003 module is designed to be used as stand-alone Dual-Port RAM where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M1001/1003 module is packaged on a multilayer co-fired ceramic 64-pin DIP (Dual In-line Package) with dimensions of only 3.2" x 0.62" x 0.38". Maximum access times as fast as 35ns over the commercial temperature range are available.

All inputs and outputs of the IDT7M1001/1003 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

All IDT military module semiconductor components are manufacured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN NAMES

Left Port	Right Port	Description
A (0–16)L	A (0–16)R	Address Inputs
I/O (0–7)L	I/O (0–7)R	Data Inputs/Outputs
R/$\overline{W}$L	R/$\overline{W}$R	Read/Write Enables
$\overline{CS}$L	$\overline{CS}$R	Chip Select
$\overline{OE}$L	$\overline{OE}$R	Output Enable
$\overline{SEM}$L	$\overline{SEM}$R	Semaphore Control
Vcc		Power
GND		Ground

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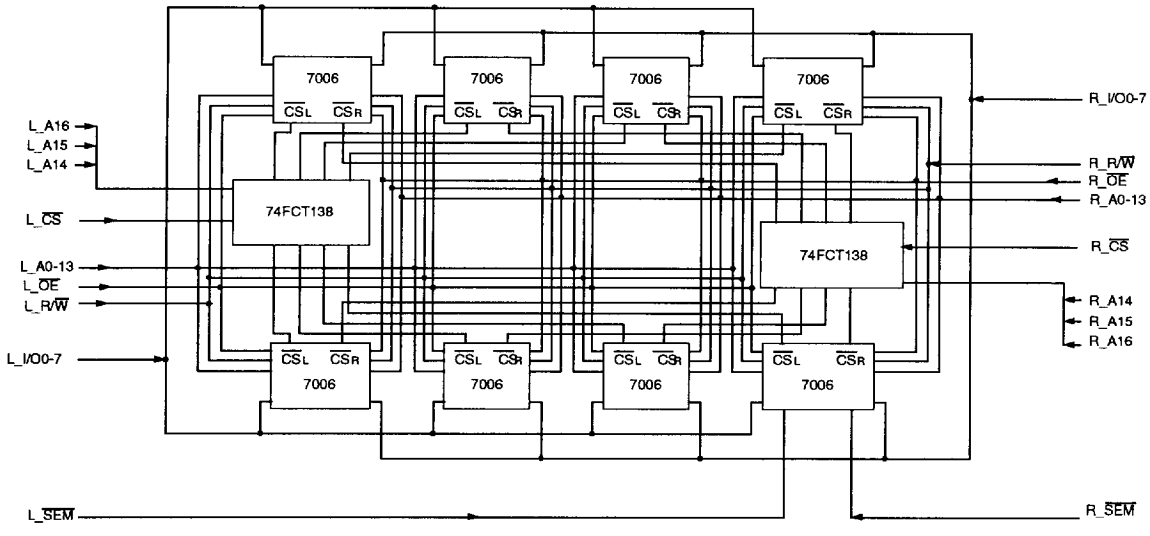
FUNCTIONAL BLOCK DIAGRAM

INTEGRATED DEVICE

7M1001



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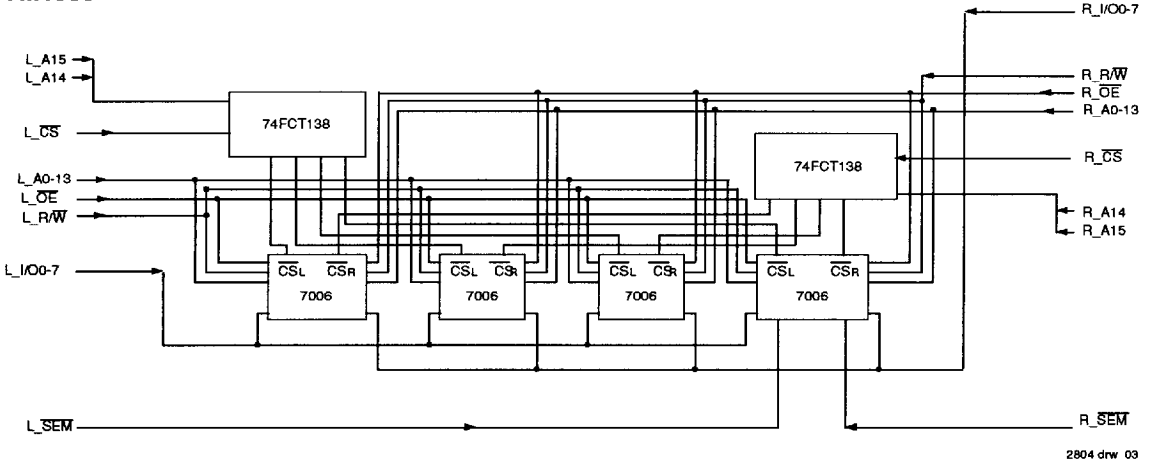
7M1003



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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0 5 to +7 0	–0 5 to +7 0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

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NOTE:
1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability

CAPACITANCE(1) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	Max.	Unit
CIN1	Input Capacitance ($\overline{CS}$ or $\overline{SEM}$)	VIN = 0V	15	pF
CIN2	Input Capacitance (Data, Address, All Other Controls)	VIN = 0V	100	pF
COUT	Output Capacitance (Data)	VOUT = 0V	100	pF

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NOTE:
1 This parameter is guaranteed by design but not tested

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5 0V ± 10%

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4 5	5 0	5 5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2 2	-	6 0	V
VIL	Input Low Voltage	–0 5(1)	-	0 8	V

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NOTE:
1 VIL (min) = –3.0V for pulse width less than 20ns

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Commercial			Military			Unit
			Min.	Max.(1)	Max.(2)	Min.	Max.(1)	Max.(2)	
ICC2	Dynamic Operating Current (Both Ports Active)	Vcc = Max , $\overline{CS}$ ≤ VIL, $\overline{SEM}$ ≥ VIH Outputs Open, f = fMAX	—	940	660	—	1130	790	mA
ICC1	Standby Supply Current (One Port Active)	Vcc = Max , L_$\overline{CS}$ or R_$\overline{CS}$ ≥ VIH Outputs Open, f = fMAX	—	750	470	—	905	565	mA
ISB1	Standby Supply Current (TTL Levels)	Vcc = Max , L_$\overline{CS}$ and R_$\overline{CS}$ ≥ VIH Outputs Open, f = fMAX L_$\overline{SEM}$ and R_$\overline{SEM}$ ≥ Vcc –0 2V	—	565	285	—	685	345	mA
ISB2	Full Standby Supply Current (CMOS Levels)	L_$\overline{CS}$ and R_$\overline{CS}$ ≥ Vcc –0 2V VIN > Vcc 0 2V or < 0 2V L_$\overline{SEM}$ and R_$\overline{SEM}$ ≥ Vcc –0 2V	—	125	65	—	245	125	mA

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NOTES:
1 IDT7M1001 (128K x 8) version only
2 IDT7M1003 (64K x 8) version only

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DC ELECTRICAL CHARACTERISTICS

INTEGRATED DEVICE

(V_{CC}=5.0V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1001 Min.	IDT7M1001 Max.	IDT7M1003 Min.	IDT7M1003 Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address, Data & Other Controls)	V_{CC} = Max V_{IN} = GND to V_{CC}	—	80	—	40	µA
$\|I_{LI}\|$	Input Leakage ($\overline{CS}$ and $\overline{SEM}$)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	80	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min I_{OH} = −4mA	2.4	—	2.4	—	V

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2804 tbl 08

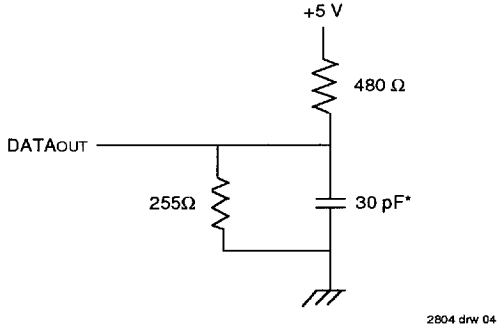

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Figure 1. Output Load

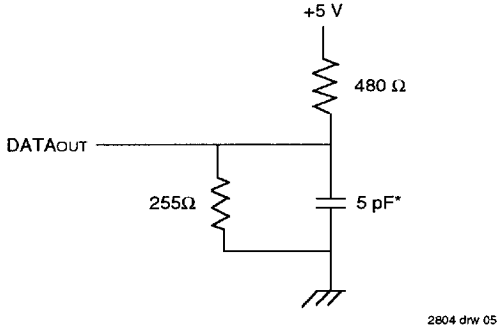

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Figure 2. Output Load
(for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

INTEGRATED DEVICE

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-35[5] Min.	-35[5] Max.	-40 Min.	-40 Max.	-50 Min.	-50 Max.	-65 Min.	-65 Max.	-80 Min.	-80 Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	35	—	40	—	50	—	65	—	80	—	ns
t_{AA}	Address Access Time	—	35	—	40	—	50	—	65	—	80	ns
t_{ACS}[2]	Chip Select Access Time	—	35	—	40	—	50	—	65	—	80	ns
t_{OE}	Output Enable Access Time	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	3	—	3	—	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	—	20	—	20	—	25	—	30	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	3	—	3	—	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	20	—	20	—	25	—	30	—	35	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power-Down Time	—	50	—	50	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	20	—	20	—	ns
Write Cycle												
t_{WC}	Write Cycle Time	35	—	40	—	50	—	65	—	80	—	ns
t_{CW}[2]	Chip Select to End-of-Write	30	—	35	—	40	—	50	—	55	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	35	—	40	—	50	—	55	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	40	—	45	—	50	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	25	—	30	—	35	—	40	—	45	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	20	—	20	—	25	—	30	—	35	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	—	20	—	20	—	25	—	30	—	35	ns
t_{OW}[1 4]	Output Active from End-of-Write	0	—	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	15	—	15	—	15	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	15	—	15	—	15	—	15	—	15	—	ns
Port-to-Port Delay Timing												
t_{WDD}[6]	Write Pulse to Data Delay	—	60	—	65	—	70	—	85	—	95	ns
t_{DDD}[6]	Write Data Valid to Read Data Valid	—	45	—	50	—	55	—	70	—	80	ns

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NOTES:

1 This parameter is guaranteed by design but not tested.
2 To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$ To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$
3 t_{AS1}= 0 if R/$\overline{W}$ is asserted LOW simultaneously with or after the $\overline{CS}$ LOW transition.
4 For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns
5 Preliminary specifications only
6 Port-to-Port delay through the RAM cells from the writing port to the reading port

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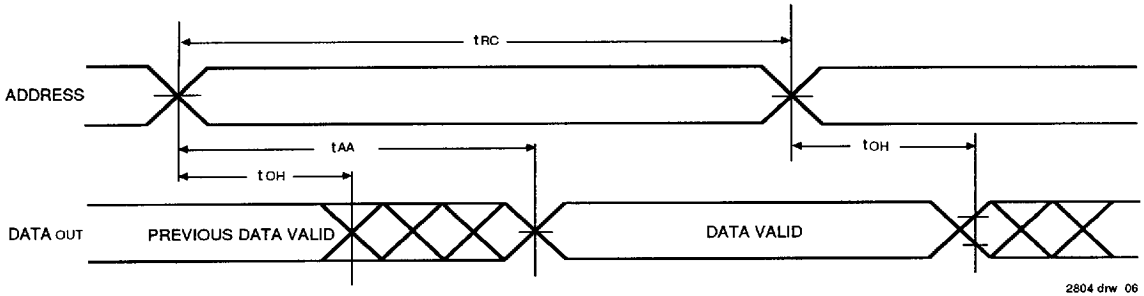
TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)(1,2,4)

INTEGRATED DEVICE



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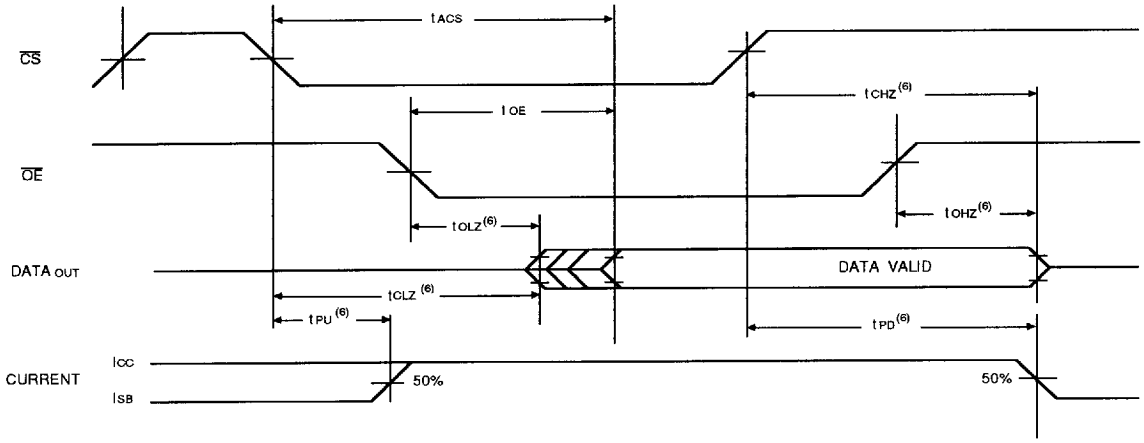
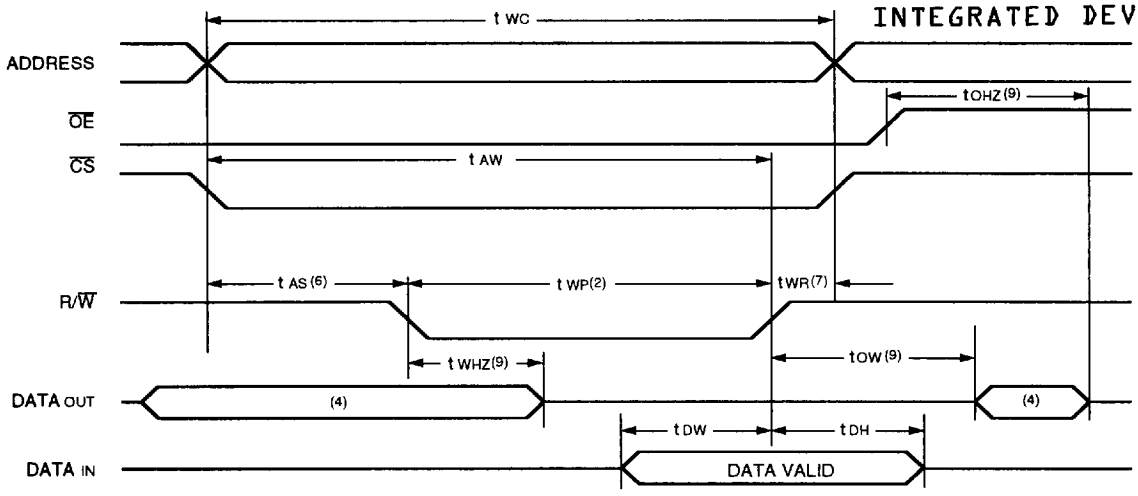
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)(1,3,5)



2804 drw 07

NOTES:
1. R/$\overline{W}$ is HIGH for Read Cycles
2. Device is continuously enabled, $\overline{CS}$ = LOW. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition LOW
4. $\overline{OE}$ = LOW.
5. To access RAM, $\overline{CS}$ = LOW, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = HIGH and $\overline{SEM}$ = LOW.
6. This parameter is guaranteed by design but not tested

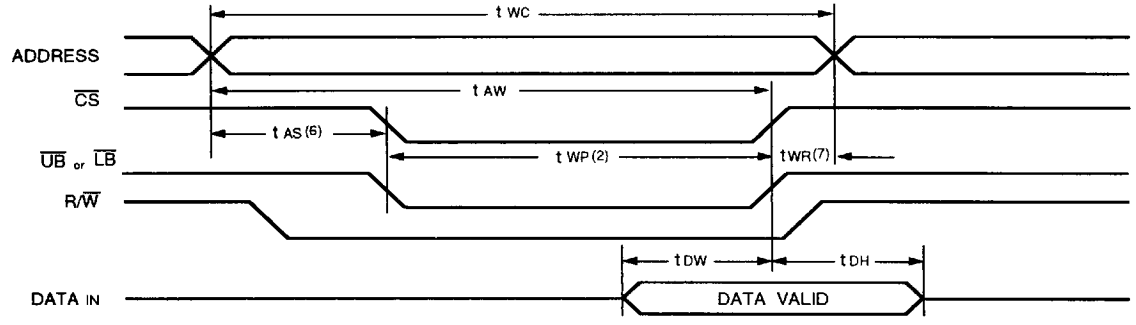
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)[1,3,5,8]



2804 drw 08

NOTES:
1. R/$\overline{W}$ is HIGH for Read Cycles
2. Device is continuously enabled $\overline{CS}$ = LOW, $\overline{UB}$ or $\overline{LB}$ = LOW. This waveform cannot be used for semaphore reads
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = LOW.
5. To access RAM, $\overline{CS}$ = LOW, $\overline{UB}$ or $\overline{LB}$ = LOW, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = HIGH and $\overline{SEM}$ = LOW
6. Timing depends on which enable signal is asserted last
7. Timing depends on which enable signal is de-asserted first
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of twp or (twz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified twp.
9. This parameter is guaranteed by design but not tested

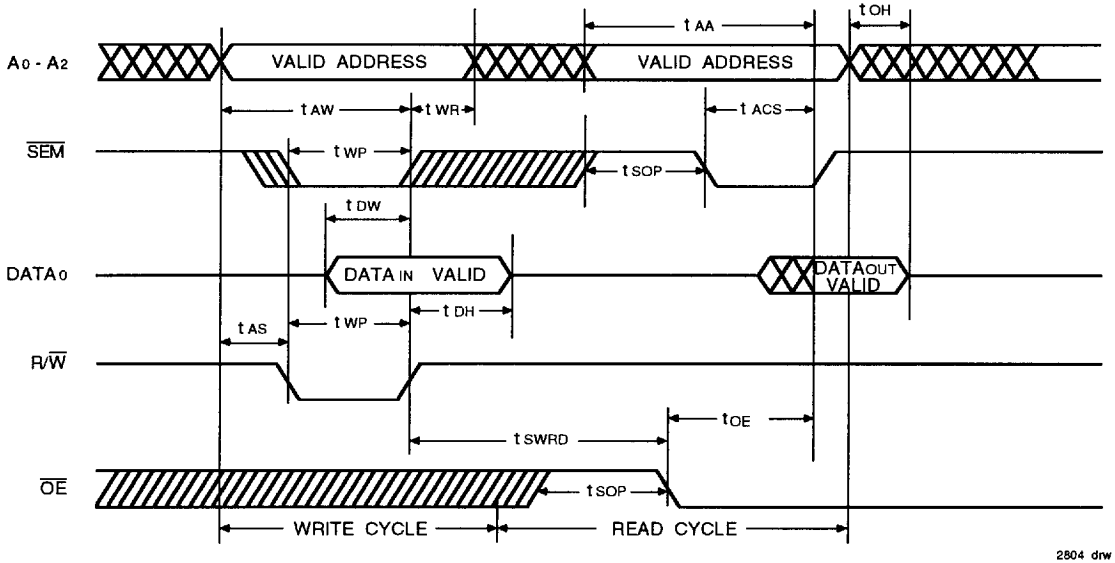
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1,3,5,8]



2804 drw 09

NOTES:
1. R/$\overline{W}$ must be HIGH during all address transitions
2. A write occurs during the overlap (twp) of a LOW $\overline{UB}$ or $\overline{LB}$ and a LOW $\overline{CS}$ and a LOW R/$\overline{W}$ for memory array writing cycle
3. twr is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle
4. During this period, the I/O pins are in the output state and input signals must not be applied
5. If the $\overline{CS}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp
9. This parameter is guaranteed by design but not tested

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)[1]



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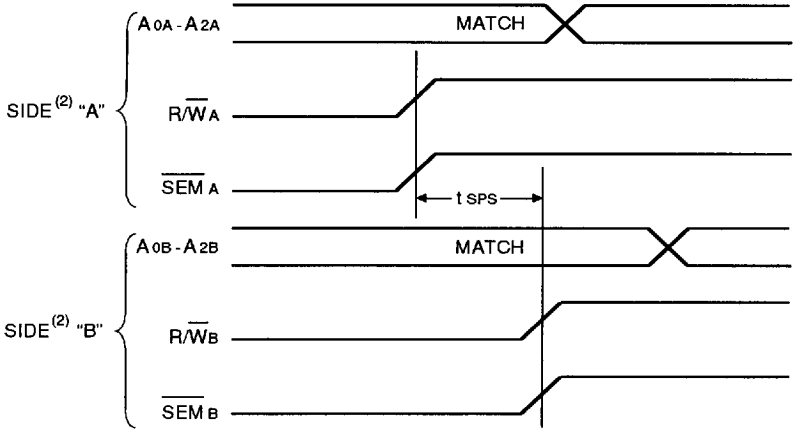
NOTE:
1. $\overline{CS}$ = HIGH for the duration of the above timing (both write and read cycle).

INTEGRATED DEVICE

TIMING WAVEFORM OF SEMAPHORE CONTENTION[1,3,4]



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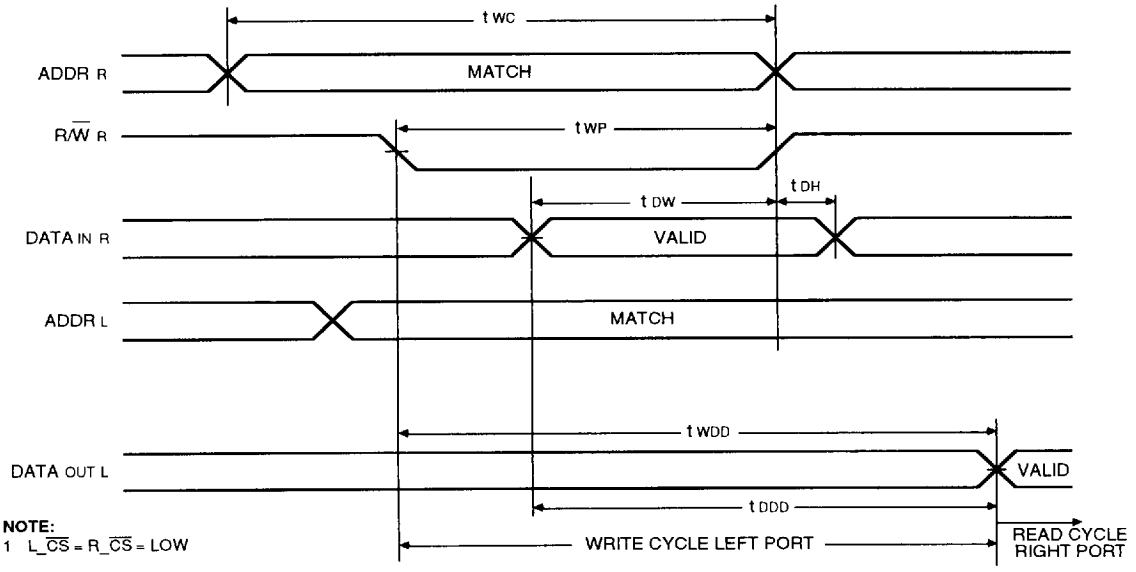
NOTES:
1. D_{0R} = D_{0L} = LOW, L_$\overline{CS}$ = R_$\overline{CS}$ = HIGH. Semaphore Flag is released form both sides (reads as ones from both sides) at cycle start
2. "A" may be either left or right port "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going HIGH to R/$\overline{W}_B$ or $\overline{SEM}_B$ going HIGH.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY(1)

INTEGRATED DEVICE



NOTE:
1 L_CS = R_CS = LOW

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TRUTH TABLES

TABLE I: NON-CONTENTION READ/WRITE CONTROL(1)

Inputs(1)				Outputs	
CS	R/W	OE	SEM	I/O0 - I/O7	Mode
H	X	X	H	High-Z	Deselected Power Down
L	L	X	H	DATAIN	Write to Both Bytes
L	H	L	H	DATAOUT	Read Both Bytes
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1 AOL — A12 ≠ AOR — A12R

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TABLE II: SEMAPHORE READ/WRITE CONTROL(1)

Inputs				Outputs	
CS	R/W	OE	SEM	I/O0 - I/O7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
X	↓	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

NOTE:
1 AOL — A12 ≠ AOR — A12R

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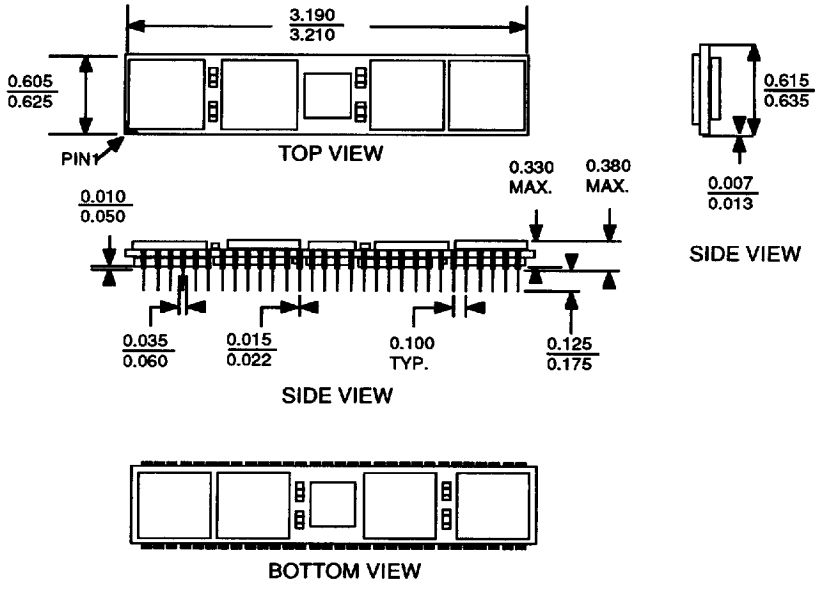
SEMAPHORE OPERATION

For more details regarding semaphores & semaphore operations, please consult the IDT7006 datasheet.

PACKAGE DIMENSIONS

INTEGRATED DEVICE

7M1001



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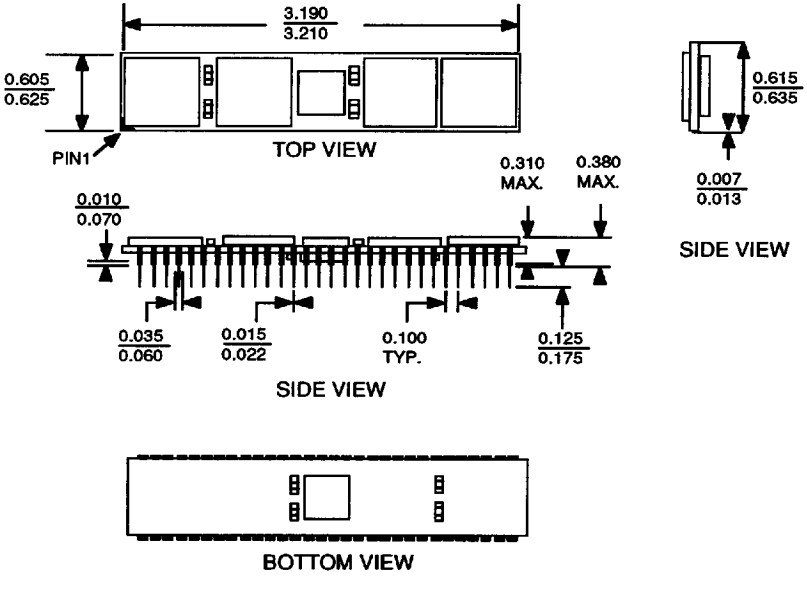
7M1003



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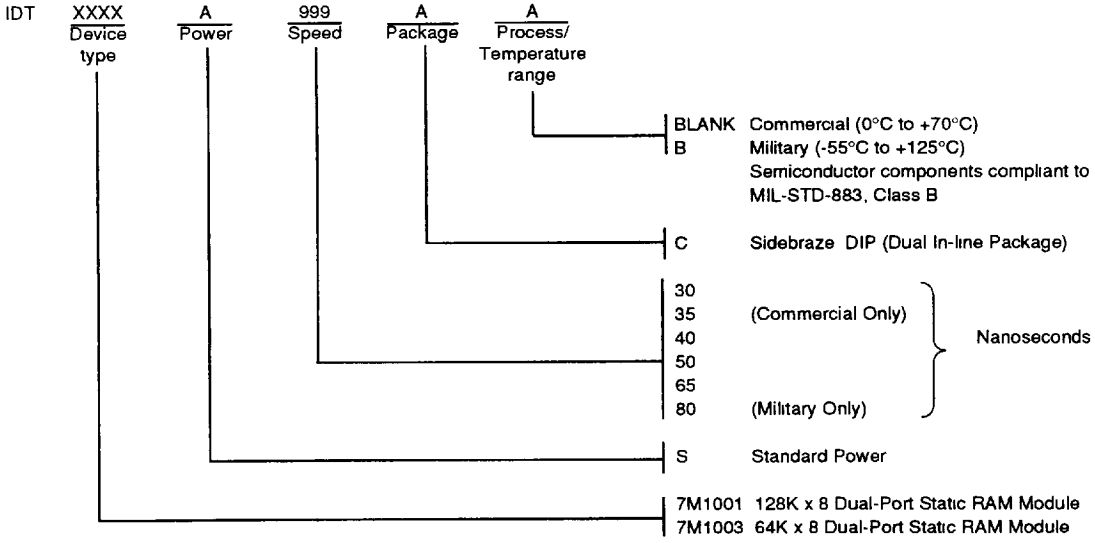
ORDERING INFORMATION

INTEGRATED DEVICE



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