HS-82C12RH

Radiation Hardened 8-Bit Input/Output Port

March 1996

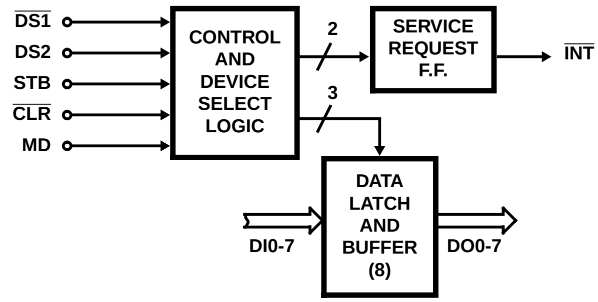
Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-95818 and Intersil' QM Plan
  - Radiation Hardened CMOS Process
  - Total Dose 1 x 10^5 RAD (Si)
  - Transient Upset > 1 x 10^8 RAD (Si)/s
  - Latch-Up Immune EPI-CMOS > 1 x 10^{12} RAD (Si)/s
- Low Power Dissipation
- High Noise Immunity
- Single Power Supply +5V
- Low Input Load Current
- 8-Bit Data Register and Buffer
- Asynchronous Register Clear
- Service Request Flip-Flop for Interrupt Generation
- Three-State Outputs
- Bus-Compatible with HS-80C85RH CPU
- Electrically Equivalent to Sandia SA3026
- Military Temperature Range -55^{o}C to +125^{o}C

Description

The Intersil HS-82C12RH is a radiation hardened 8-bit input/output port designed for use with the HS-80C85RH radiation hardened microprocessor. It is manufactured using a self-aligned, junction-isolated EPI-CMOS process and features three-state output buffers and device selection and control logic. A service request flip-flop is included for the generation and control of interrupts to the microprocessor. The device can be used in implement many of the peripheral and input/output functions of a microcomputer system. The HS-82C12RH is pinout- and function- compatible with industry-standard 8212 devices.

Functional Diagram



Pin Description

PIN	DESCRIPTION
DI0-DI7	Data In
DO0-DO7	Data Out
$\overline{DS1}$, DS2	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt
$\overline{CLR}$	Clear

Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962R9581801QJC	-55^{o}C to +125^{o}C	MIL-PRF-38535 Level Q	24 Lead SBDIP
5962R9581801QXC	-55^{o}C to +125^{o}C	MIL-PRF-38535 Level Q	24 Lead Ceramic Flatpack
5962R9581801VJC	-55^{o}C to +125^{o}C	MIL-PRF-38535 Level V	24 Lead SBDIP
5962R9581801VXC	-55^{o}C to +125^{o}C	MIL-PRF-38535 Level V	24 Lead Ceramic Flatpack
HS1-82C12RH/Sample	+25^{o}C	Sample	24 Lead SBDIP
HS9-82C12RH/Sample	+25^{o}C	Sample	24 Lead Ceramic Flatpack

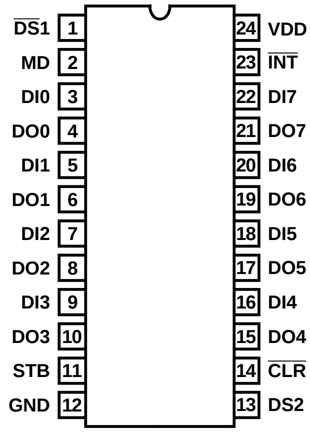
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Spec Number 518063
File Number 3041.2

Pinouts

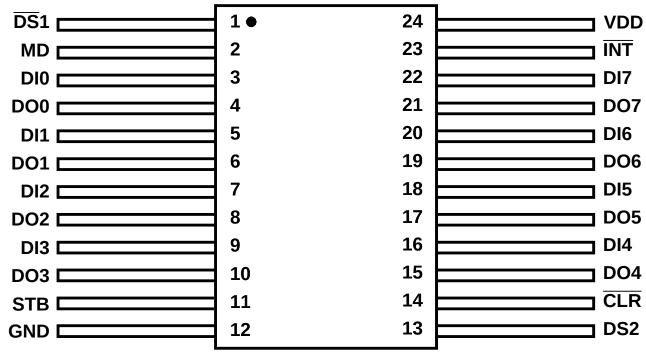
24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T24

TOP VIEW



24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP4-F24

TOP VIEW



Absolute Maximum Ratings

Supply Voltage . . . . +7.0V
Input, Output or I/O Voltage . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . -65^oC to $+150^oC$
Junction Temperature . . . . $+175^oC$
Lead Temperature (Soldering 10s) . . . . $+300^oC$
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	$55^oC/W$	$14^oC/W$
Ceramic Flatpack Package	$74^oC/W$	$13^oC/W$

Maximum Package Power Dissipation at $+125^oC$ Ambient
SBDIP Package 0.91W
Ceramic Flatpack Package 0.68W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package 18.2mW/C
Ceramic Flatpack Package 13.5mW/C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . +4.75V to +5.25V
Operating Temperature Range . . . . -55^oC to $+125^oC$
Input Low Voltage . . . . 0V to +1.0V
Input High Voltage . . . . VDD -1V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Input Leakage Current	IIH	VDD = 5.25V, VIN = 0V, Pin under test = 5.25V	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	-	1	µA
Low Input Leakage Current	IIL	VDD = 5.25V, VIN = 5.25V, Pin under test = 0V	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	-1	-	µA
Low Output Voltage	VOL	VDD = 5.25V, IOL = 2mA	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	-	0.5	V
High Output Voltage	VOH	VDD = 4.75V, IOH = -2mA	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	4.25	-	V
Static Current	SIDD	VDD = 5.25V, VIN = GND	1, 2, 3	-55^oC, $+25^oC$, $+125^oC$	-	100	µA
Functional Tests	FT	VDD = 4.75V and 5.25V, VIH = VDD-1.0V, VIL = 1.0V	7, 8A, 8B	-55^oC, $+25^oC$, $+125^oC$	-	-	-

NOTE: All devices are guaranteed at worst case limits and over radiation.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Data to Output Delay	TPD	9, 10, 11	-55^oC, $+25^oC$, $+125^oC$	-	105	ns
Write Enable to Output Delay	TWE	9, 10, 11	-55^oC, $+25^oC$, $+125^oC$	-	200	ns
Reset to Output Delay	TR	9, 10, 11	-55^oC, $+25^oC$, $+125^oC$	-	145	ns
Set to Output Delay	TS	9, 10, 11	-55^oC, $+25^oC$, $+125^oC$	-	100	ns
Clear to Output Delay	TC	9, 10, 11	-55^oC, $+25^oC$, $+125^oC$	-	135	ns
Output Enable Time	TE	9, 10, 11	-55^oC, $+25^oC$, $+125^oC$	-	125	ns
Output Disable Time	TD	9, 10, 11	-55^oC, $+25^oC$, $+125^oC$	-	85	ns

NOTE:

1. Output Timings are measured with the following conditions: CL = 100pF, VIH = 3.75V, and VIL = 1.0V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground		T_A = +25^{o}C	-	8	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground		T_A = +25^{o}C	-	8	pF
Pulse Width	TPW	VDD = 4.75, VIH = 3.75, VIL = 1.0	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	-	50	ns
Data Set Up Time	TSET	VDD = 4.75, VIH = 3.75, VIL = 1.0	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	-	30	ns
Data Hold Time	TH	VDD = 4.75, VIH = 3.75, VIL = 1.0	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	-	40	ns

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

Timing Waveforms

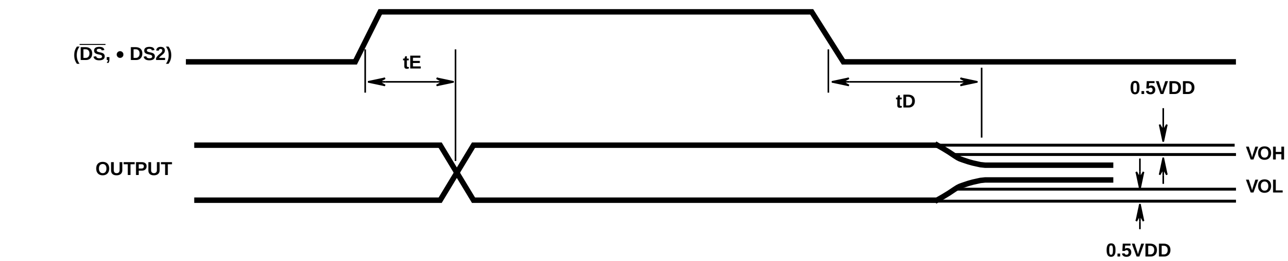


FIGURE 1. READ TIMING

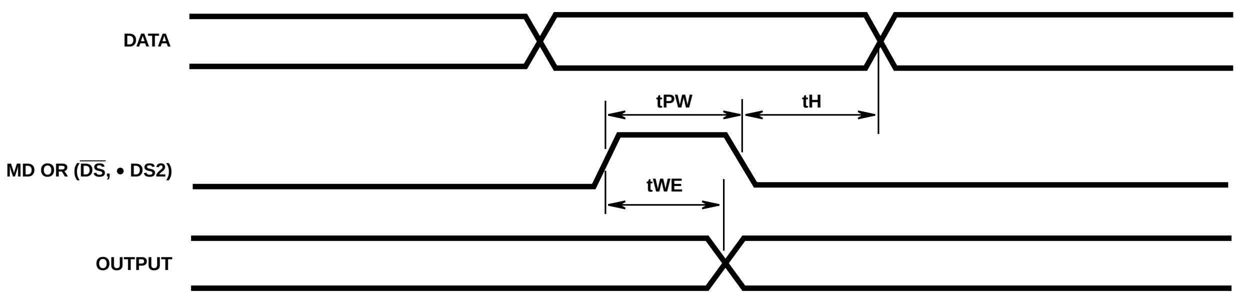


FIGURE 2. WRITE TIMING

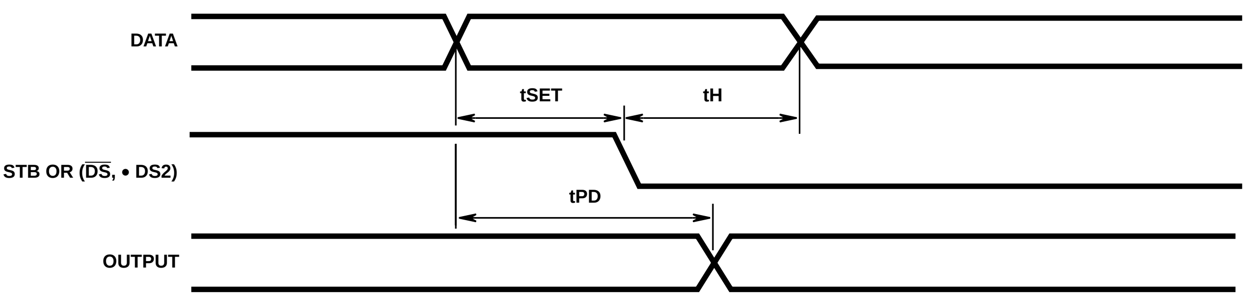


FIGURE 3. DATA SETUP, HOLD, PROPAGATION DELAY TIMING

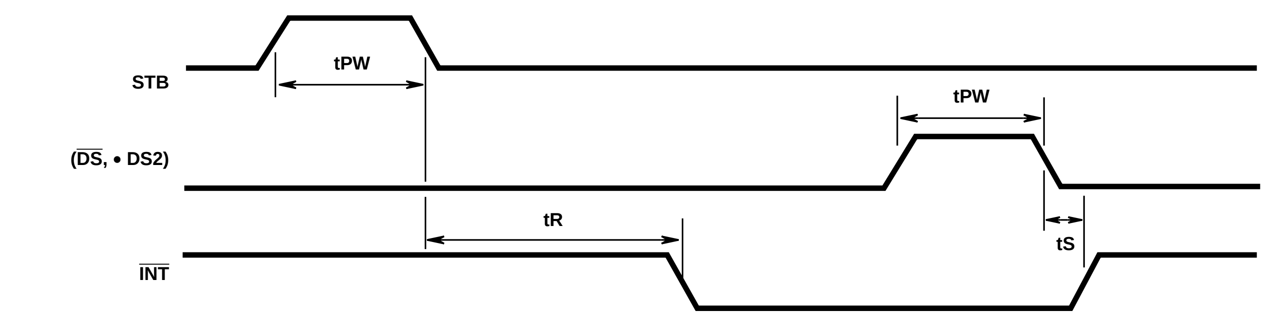


FIGURE 4. INTERRUPT TIMING

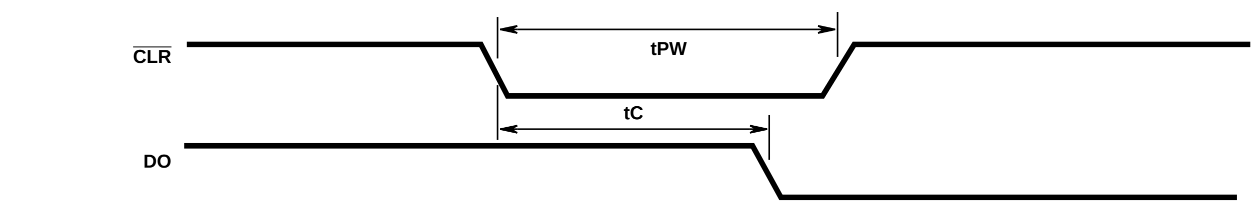


FIGURE 5. CLEAR TIMING

Functional Description

Data Latch

The data latch is comprised of eight “D” type flip-flops. The output of each flip-flop will follow the corresponding data input (DI0 - DI7) when the clock (C) is high. The clock input is level sensitive and the data becomes latched when the clock returns low.

An asynchronous reset ($\overline{\text{CLR}}$) is used to clear the latched data. Since the clock (C) overrides the reset ($\overline{\text{CLR}}$), the data must be in the latched state in order to clear the flip-flops. If the data is not latched (i.e. clock is high) when $\overline{\text{CLR}}$ goes low, then the Q outputs of the data latch will continue to follow the data input, overriding the reset signal.

Output Buffer

Three-state buffers are used to provide output drive for the data latch. A high level on the “output buffer enable” control line enables the buffer outputs. When “output buffer enable” is low the buffer outputs are forced to the high-impedance state.

Device Select Logic

The inputs $\overline{\text{DS}}$1 and DS2 are used for device selection. When $\overline{\text{DS}}$1 is low and DS2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously cleared when the device is selected.

Mode

the mode input (MD) is used to control the state of the output buffer and to determine the source of the data latch clock (C). When MD is high, the output buffers are enabled and the source of the data latch clock (C) is the device select logic ($\overline{\text{DS}}$1 • DS2).

When MD is low, the state of the output buffer is controlled by the device select logic ($\overline{\text{DS}}$1 • DS2) and the source of the data latch clock is the strobe (STB) input.

Strobe

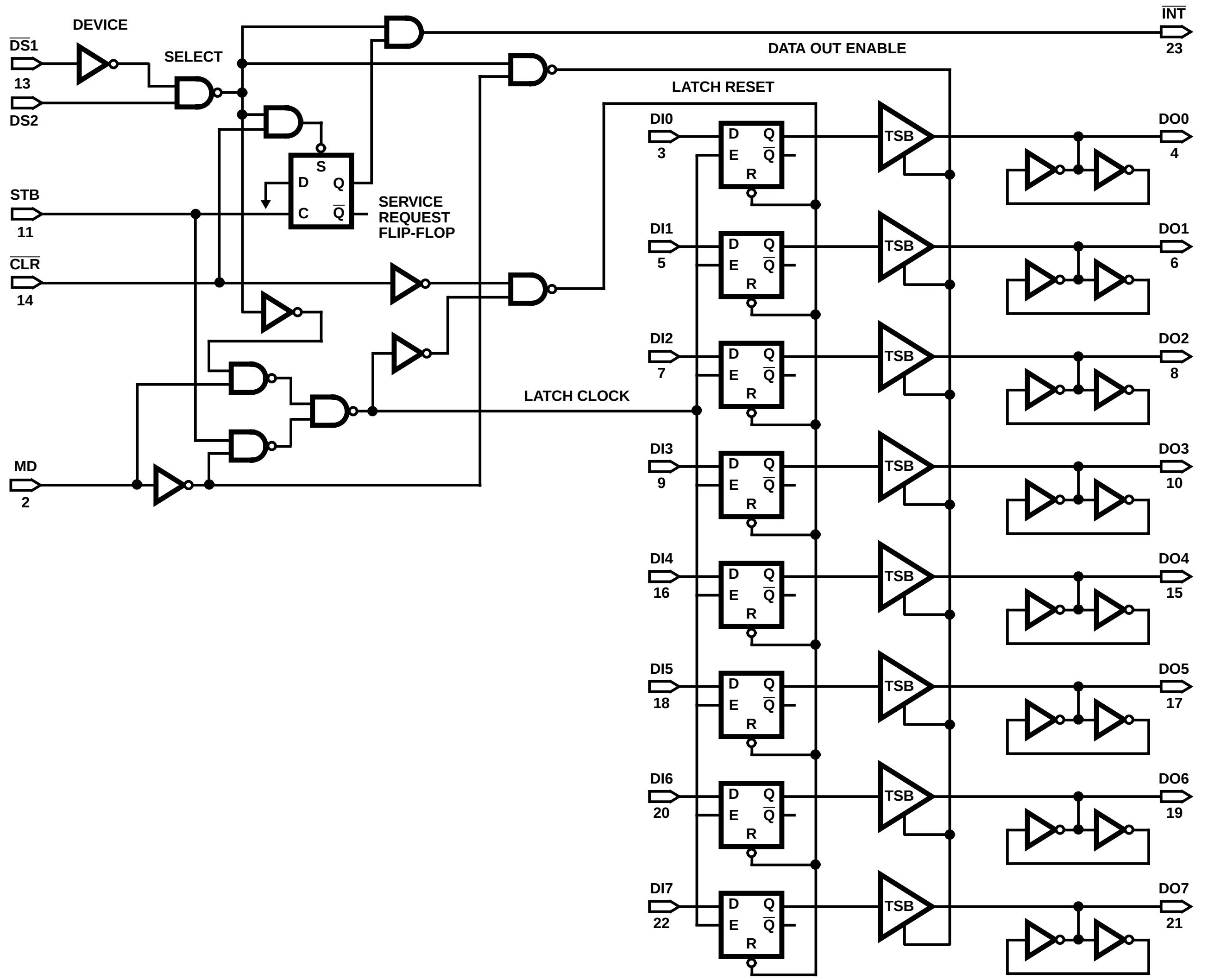
The strobe input (STB) is used as the data latch clock (C) when the mode input (MD) is low. The service request flip-flop is synchronously set on the negative going edge of STB.

Service Request Flip-Flop

The service request flip-flop is to generate interrupts to microcomputer systems. It is negative edge triggered and asynchronously cleared (reset).

The output of the service request flip-flop is AND-gated with the device select logic ($\overline{\text{DS}}$1 • DS2). The output of the AND gate is the active low interrupt ($\overline{\text{INT}}$) signal.

Logic Diagram



TRUTH TABLE 1. DATA OUT

STB	MD	$\overline{DS1}$ • DS2	DATA OUT EQUALS
0	0	0	High Z State
1	0	0	High Z State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

TRUTH TABLE 2. $\overline{INT}$

$\overline{CLR}$	$\overline{DS1}$ • DS2	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	‾|_	1	0
1	1 RESET	0	0	0
1	0	0	0	1

* Internal Service Request Flip-Flop

Metallization Topology

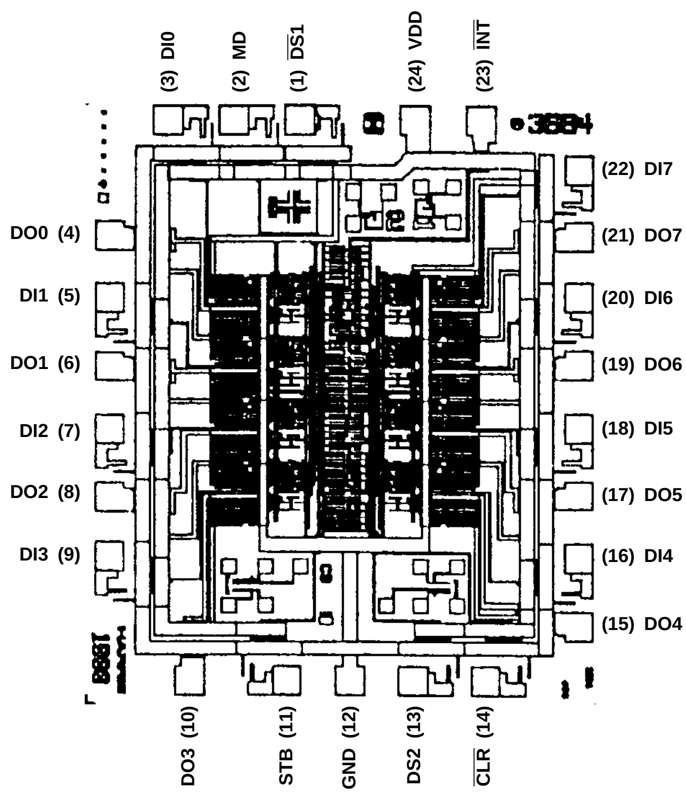
DIE DIMENSIONS:
90 x 76 x 14 ± 1mils

METALLIZATION:
Type: AlSi
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

Metallization Mask Layout

HS-82C12RH



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