ANALOG DEVICES

AN-1177
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

LVDS and M-LVDS Circuit Implementation Guide

by Dr. Conal Watterson

INTRODUCTION

Low voltage differential signaling (LVDS) is a standard for communicating at high speed in point-to-point applications. Multipoint LVDS (M-LVDS) is a similar standard for multipoint applications. Both LVDS and M-LVDS use differential signaling, a two-wire communication method where receivers detect data based on the voltage difference between two complementary electrical signals. This greatly improves noise immunity and minimizes emissions.

LVDS

LVDS is a lower power alternative to emitter-coupled logic (ECL) or positive emitter-coupled logic (PECL).The primary standard for LVDS is TIA/EIA-644. An alternative standard sometimes used for LVDS is IEEE 1596.3—SCI, scalable coherent interface. LVDS has been widely adopted for high-speed backplane, cabled, and board-to-board data transmission and clock distribution, as well as communication links within a single PCB.

Advantages of LVDS include

- Communication at speeds of up to 1 Gbps or more
- Reduced electromagnetic emissions
- Increased immunity to noise
- Low power operation
- Common-mode range allowing differences of up to ±1 V in ground offset

M-LVDS

The standard TIA/EIA-899 for multipoint low voltage differential signaling (M-LVDS) extends LVDS to address multipoint applications. M-LVDS allows higher speed communication links than TIA/EIA-485 (RS-485) or controller area network (CAN) with lower power. See the References section for a list of the standards referred to in this application note.

Additional features of M-LVDS over LVDS include

- Increased driver output strength
- Controlled transition times
- Extended common-mode range
- Option of failsafe receivers for bus idle condition

LVDS/M-LVDS APPLICATION CONSIDERATIONS

This application note considers the following aspects concerning LVDS/M-LVDS circuit implementation:

- Bus types and topologies
- Clock distribution applications
- Characteristics of LVDS/M-LVDS signaling
- Termination and PCB layout
- Jitter and skew
- Data encoding and synchronization
- Isolation

WHY USE LVDS OR M-LVDS?

LVDS and M-LVDS are compared to other multipoint and point-to-point protocols in Figure 1. Both standards have low power requirements. LVDS and M-LVDS are characterized by differential signaling with a low differential voltage swing. M-LVDS specifies an increased differential output voltage compared to LVDS in order to allow for the increased load from a multipoint bus.

Both protocols are designed for high-speed communication. Typical applications utilize PCB traces or short wired/backplane links. The common mode range of LVDS is designed for these applications. M-LVDS has an extended common mode range compared to LVDS to allow for the additional noise in a multipoint topology.

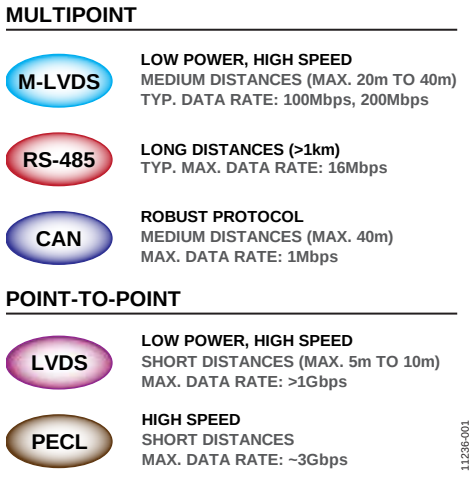

Figure 1. Comparison of Communication Standards

TABLE OF CONTENTS

REVISION HISTORY

3/13—Revision 0: Initial Version

BUS TYPES AND TOPOLOGIES

Standard TIA/EIA-644 LVDS devices allow low power, high speed communication. The advantages of LVDS can also be applied to multipoint applications by using TIA/EIA-899 devices. Bus topology is one of the main factors relating to which LVDS or M-LVDS devices are used in an application.

POINT-TO-POINT

Point-to-point bus topologies consist of a single driver and single receiver connected together using one pair of wires or traces. Figure 2 demonstrates a typical configuration, where the receiving end of the link has a termination resistor. This is the most common application for LVDS devices. Multiple pairs of wires or traces can be used to create additional channels of communication and increase total bandwidth between two points.

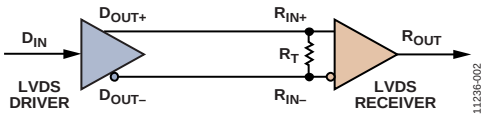

Figure 2. LVDS Point-to-Point Link

Analog Devices, Inc., has a portfolio of LVDS drivers and receivers for one, two or four LVDS channels as shown in Table 1. Unused outputs should be left open circuit.

Table 1. LVDS Drivers and Receivers

Part No.	Tx	Rx	Part No.	Tx	Rx
ADN4661	1	0	ADN4665	4	0
ADN4662	0	1	ADN4666	0	4
ADN4663	2	0	ADN4667	4	0
ADN4664	0	2	ADN4668	0	4

M-LVDS can also be used in a point-to-point topology, where the same transceiver device is used for the driver circuit (with receiver disabled) and the receiving circuit (with driver disabled).

MULTI-DROP

A single driver can be connected to multiple receivers using a multi-drop bus topology as shown in Figure 3. LVDS is designed for point-to-point applications and so in a multi-drop configuration, the number of receivers that can be connected and the signaling distance can be limited. M-LVDS can be used in a multi-drop topology to drive up to 32 nodes across longer distances compared to LVDS.

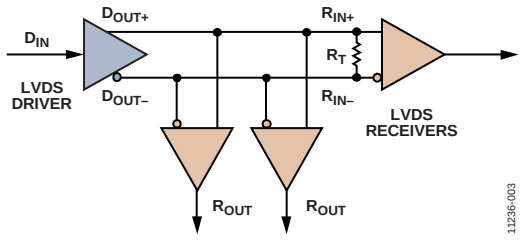

Figure 3. LVDS Multi-Drop Bus

MULTIPOINT

In networks where multiple devices can either send or receive, a multipoint bus topology may be used. M-LVDS is designed for such multi-point applications, allowing up to 32 nodes to be connected to a single bus. There are two types of multipoint buses, half-duplex and full duplex, shown in Figure 4 and Figure 5, respectively. In a half-duplex bus, two wires are used such that one device may transmit, and the other devices can receive. In a full-duplex bus, four wires are used, allowing one node to concurrently transmit back to another transmitting node (that is, slave devices responding as broadcast commands are sent by the master to all nodes).

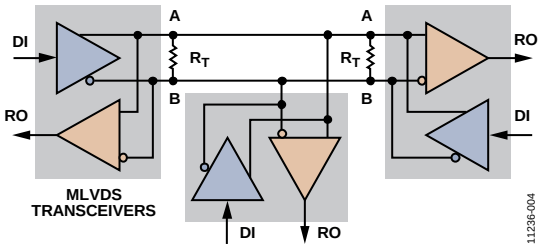

Figure 4. M-LVDS Half-Duplex Bus

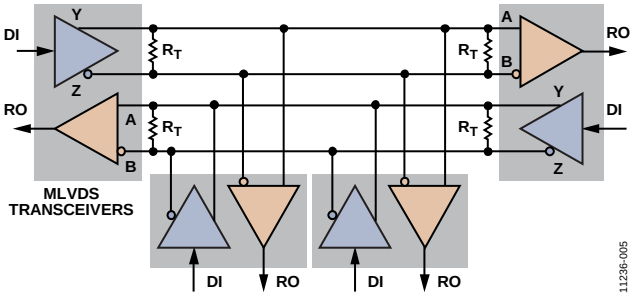

Figure 5. M-LVDS Full-Duplex Bus

Another factor to be considered in multipoint buses is the bus idle condition. When no device is transmitting, the differential voltage on a terminated bus will be close to 0 V. This means that for a standard receiver with symmetrical input thresholds, the receiver output will be undefined. This corresponds to the Type 1 M-LVDS receivers with an input threshold of ±50 mV. In order to provide a guaranteed receiver output state (output low) in the bus idle condition, Type 2 M-LVDS receivers have an offset receiver input threshold of +50 mV to +150 mV.

Table 2. M-LVDS Transceivers

Part No.	Rx Type	Duplex	Data Rate
ADN4690E	1	Half	100
ADN4691E	1	Half	200
ADN4692E	1	Full	100
ADN4693E	1	Full	200
ADN4694E	2	Half	100
ADN4695E	2	Full	100
ADN4696E	2	Half	200
ADN4697E	2	Full	200

CLOCK DISTRIBUTION APPLICATIONS

Differential signaling, such as LVDS, is a good choice for distributing clock signals around a circuit board. In addition to the benefits of the common-mode noise immunity of LVDS, a particular advantage for clock distribution applications is that radiated emissions are reduced due to the coupling between the two opposing signals.

MULTI-DROP CLOCK DISTRIBUTION

In many applications, multiple nodes in a circuit may depend on a single clock source. A simple approach to distributing a single clock source to multiple nodes using LVDS, is to use a multi-drop bus topology as shown in Figure 6. The LVDS outputs of a clock source are connected to a pair of signal traces that have short stubs to the various nodes relying on the clock.

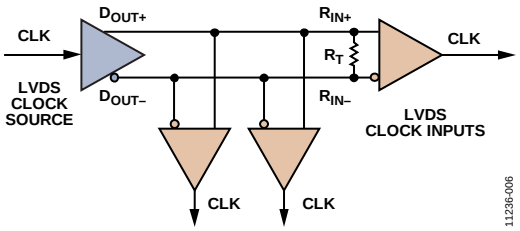

Figure 6. Multi-Drop LVDS Clock Distribution

The disadvantages of this approach are that the number of nodes that can be connected is limited and stubs contribute to degradation of the signal integrity (that is, adding jitter). Stub lengths and impedances must be carefully controlled.

POINT-TO-POINT CLOCK DISTRIBUTION

A single clock source can be connected to a single node requiring an LVDS clock input using a point-to-point link. This can be extended to supply multiple nodes by means of an LVDS buffer acting as a fan-out device. This separate component receives the LVDS clock output from the clock source, and in turn provides this clock signal to multiple LVDS drivers in the device to drive multiple point-to-point links to receiving nodes. The advantage of this approach is that timing on the clock signal can remain unaffected by stubs.

An example of such a device is the ADN4670 clock distribution buffer. This allows one of two clock sources to be distributed on up to 10 outputs as shown in Figure 7. The outputs can be enabled and disabled by means of a serially programmable register, which is also used to select the clock source.

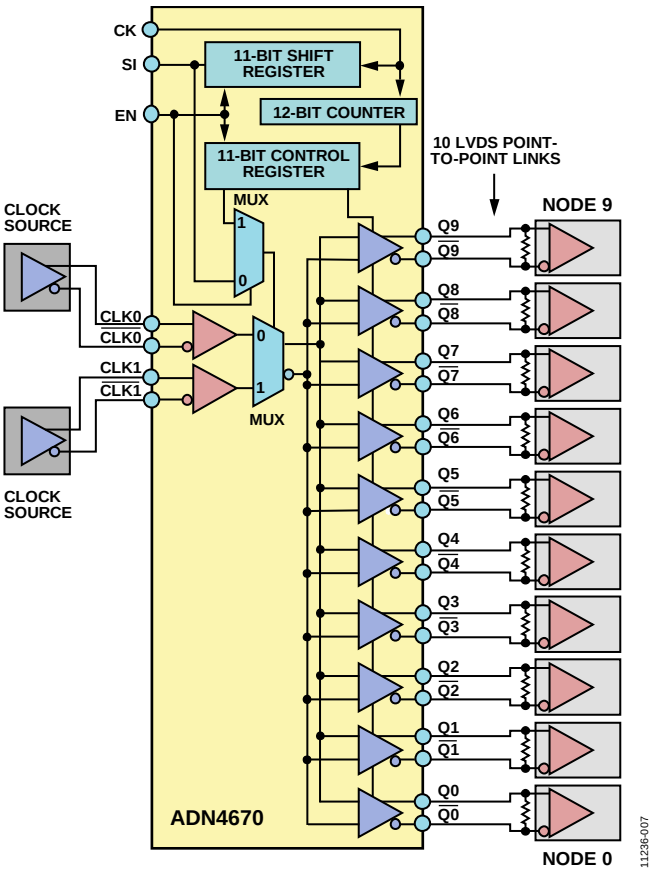

Figure 7. ADN4670 Application Distributing a Clock Source to 10 Nodes via Point-To-Point LVDS Connections

Any buffer adds a small amount of jitter when inserted between the initial LVDS output and the eventual LVDS input, but the ADN4670 has been designed to have low additive jitter of <300 fs. Skew between the 10 outputs is kept to less than 30 ps with clock signals of up to 1.1 GHz.

CLOCK DISTRIBUTION USING M-LVDS

Another option for clock distribution is using M-LVDS transceivers to distribute the clock to up to 32 nodes in a multi-drop (or multipoint) topology. Type 1 M-LVDS receivers (such as in the ADN4690E to ADN4693E) are suited to such applications because there is no offset in the receiver threshold (this offset can result in duty cycle distortion for a clock signal).

The ADN4690E to ADN4693E M-LVDS transceivers with Type 1 receivers also have additional slew-rate limiting of the edges from the driver outputs, which further limits radiated emissions and the effect of reflections from stubs.

DIFFERENTIAL SIGNALLING AND LVDS/M-LVDS

Differential transmission is communication where two complementary signals are transmitted, with the received signal comprising the difference between the two signal lines. This form of communication, used by both LVDS and M-LVDS, has two distinct advantages, high noise immunity and low emissions.

The high noise immunity arises because typically a noise source couples equally onto both signal lines, leaving the differential signal unaffected. Emissions from differential signaling are low due to the tight coupling between the two complementary signal lines when using a typical medium (twisted pair cable, or closely placed strip line).

DEFINITIONS AND OUTPUT LEVELS

For LVDS and M-LVDS, one signal line is noninverting (that is, high for a Logic 1 and low for a Logic 0) and the other signal line is inverting (that is, the complement of the noninverting signal). The difference in voltage between the two signal lines is termed the differential voltage, V_{OD}. V_{OD} is also shorthand for the magnitude of the differential voltage (positive or negative), or $|V_{OD}|$. The two signal lines each have a maximum voltage swing of $|V_{OD}|$, centered on the common-mode voltage, V_{OC} (also referred to as the offset voltage, V_{OS}). The differential voltage swings around 0 V. Typical LVDS signal levels are shown in Figure 8, together with the differential signal V_{OD} and common-mode voltage V_{OC}. In this figure, V_{OUT+} is the noninverting signal and V_{OUT-} is the inverting signal.

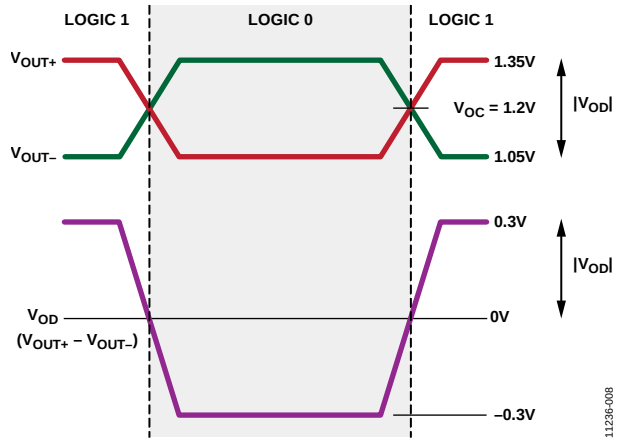

Figure 8. LVDS Output Levels

The differential voltage on an LVDS or M-LVDS bus is generated by a driver current source. Noninverting LVDS driver outputs or receiver inputs are generally denoted with a + and inverting driver outputs or receiver inputs with a –.

Pin names are shown for the ADN4663 2-channel LVDS driver and ADN4664 2-channel LVDS receiver in Figure 9. M-LVDS follows the convention of RS-485 physical layer transceivers in naming the bus lines A for the noninverting signal and B for the inverting signal, or Y and Z for driver outputs on a full-duplex transceiver.

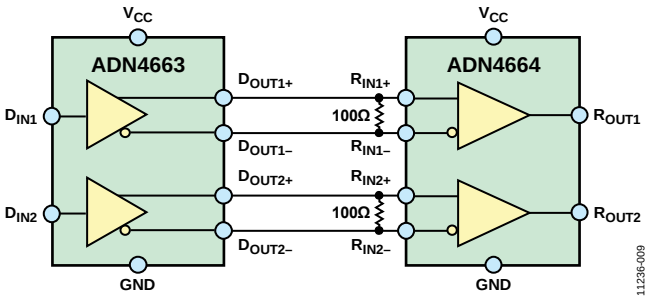

Figure 9. ADN4663 and ADN4664 2-Channel LVDS Point-to-Point

The distinction between LVDS and M-LVDS and other differential signaling standards is that they have a low output swing. The differential output voltage and common mode range specifications of LVDS and M-LVDS are shown in Figure 10. For LVDS, the output voltage swing, $|V_{OD}|$, is a minimum of 250 mV and a maximum of 450 mV with a load of 100 Ω. This allows low power operation and ensures that while transitions are fast, to allow high data rates, the reduced output swing means that the slew rate is not too severe. Rise and fall times are generally in the region of hundreds of picoseconds, resulting in slew rates of around 0.5 V/ns to 2.5 V/ns.

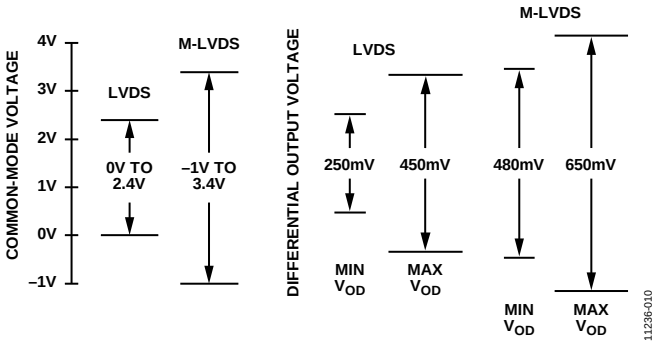

Figure 10. LVDS and M-LVDS Signaling Levels

M-LVDS has slew-rate limited drivers to enhance the robustness of the signaling when there are additional impedance discontinuities from multiple drivers/receivers and stubs. This means that M-LVDS is limited to lower data rates compared to LVDS. The ADN4690E through ADN4697E are available with options for 100 Mbps or higher speed 200 Mbps. Another characteristic of M-LVDS is increased driver strength, resulting in a minimum output voltage swing $|V_{OD}|$ of 480 mV and a maximum of 650 mV with a load of 50 Ω (two termination resistors of 100 Ω, one either end of the bus).

RECEIVER THRESHOLDS

The receiver thresholds are the differential voltage levels above or below which the received signal is considered a Logic 1 or a Logic 0. For LVDS, a positive V_{OD} >= +100 mV corresponds to a Logic 1 and a negative V_{OD} <= -100 mV corresponds to a Logic 0.

For Type 1 M-LVDS receivers, a positive $V_{OD} \geq +50$ mV corresponds to a Logic 1 and a negative $V_{OD} \leq -50$ mV corresponds to a Logic 0.

In between these voltage thresholds is the transition region. If an input signal remains at a voltage level between the thresholds, the receiver output is undefined under LVDS; it can be high or low. This can occur if no active LVDS driver is connected to the receiver, or if there is a short circuit. Analog Devices LVDS receivers incorporate a failsafe feature, so that in these cases, the receiver output is high.

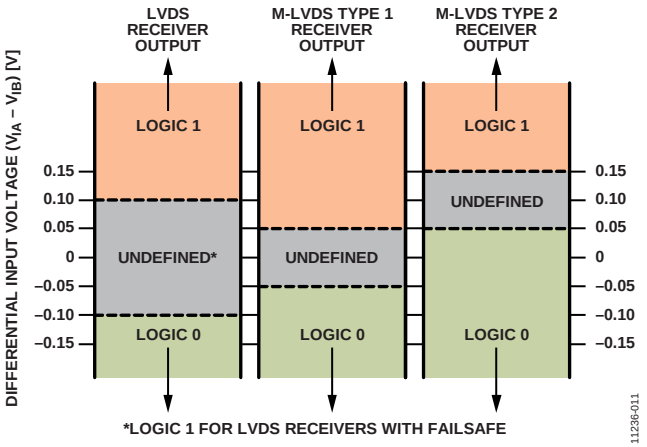

Figure 11. Receiver Thresholds for LVDS and M-LVDS

With M-LVDS, any node on the bus can transmit, but when no node is active, all driver outputs are disabled. As with LVDS, this results in a differential output voltage in the undefined region for Type 1 receivers. In order to provide a failsafe condition, M-LVDS defines Type 2 receivers that have an offset receiver threshold of >= +150 mV for a logic high and <= +50 mV for a logic low. This means that the failsafe output from Type 2 M-LVDS receivers is a logic low. Receiver thresholds are shown in Figure 11 for LVDS receivers, M-LVDS Type 1 receivers and M-LVDS Type 2 receivers.

TRANSMISSION DISTANCE

Both LVDS and M-LVDS transmission distances are affected by two main factors: the transmission medium and the data rate. The standard deciding factor of whether a given transmission distance is practical, is how much jitter is observed by receiving nodes. This is application dependent; some applications require 5% or less jitter, whereas others tolerate up to 20%.

PCB traces typically allow transmission distances on the order of tens of centimeters, whereas twisted pair cable allows transmission on the order of meters for LVDS or tens of meters for M-LVDS. Different specifications of PCB construction or cable types affect the signal differently and thus have an impact on the maximum transmission distance.

Higher data rates greatly constrain the transmission distance; LVDS at 1 Gbps might only be transmitted across high-quality cables of 1 meter (possibly with additional signal conditioning), but at 100 Mbps may be transmitted across 10 meters (depending on the cable type). M-LVDS can generally be transmitted across longer cables due to the increased driver strength, but data rates of hundreds of Mbps require shorter cables than data rates of only tens of Mbps. Figure 12 provides a general indication of the combinations of LVDS and M-LVDS data rates and cable lengths typical for some applications.

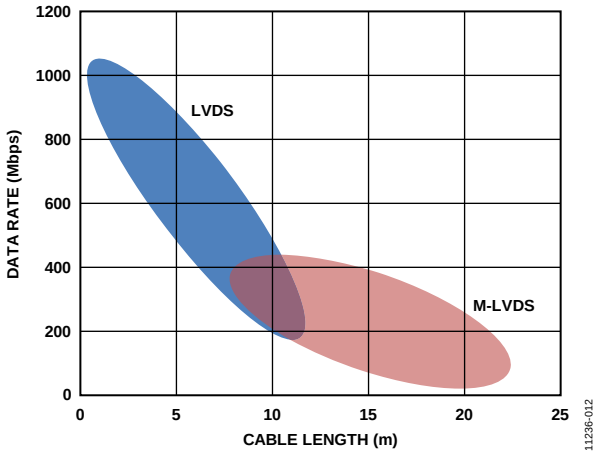

Figure 12. Cable Length (Twisted-Pair) vs. Data Rate for Some Typical LVDS and M-LVDS Applications

Other factors influencing the maximum distance include:

- The transmitter specifications.
- Other transmission medium components, such as vias (on PCB traces) or connectors for cables.
- For M-LVDS or multi-drop LVDS, the number of nodes on the bus and the stub lengths.

TIA/EIA-644 (LVDS) and TIA/EIA-899 (M-LVDS) recommend testing intended cable lengths in the application if possible, due to the multiple factors involved that affect the possible cable length. This allows the jitter on the received signal to be measured, providing a guide as to how practical a given cable type and length is. Measurements can be taken using an eye diagram; the ADN4696E driver output is shown in Figure 13.

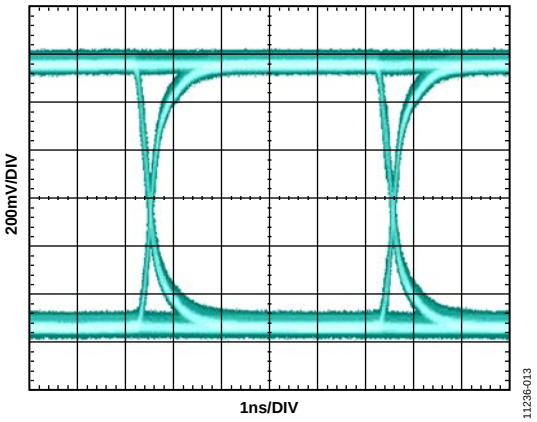

Figure 13. ADN4696E Driver Output Eye Diagram

TERMINATION AND PCB LAYOUT

High speed communication links, such as those used for LVDS and M-LVDS, should be considered in the context of transmission line theory, whether cables or PCB traces are used. The high data rates of LVDS and M-LVDS require fast rise times, meaning that impedance discontinuities and the end of the communication link can significantly affect the transmitted signal as it propagates from the driver to the far ends of the bus. To avoid degradation of the signal, controlled impedances along the communication medium, as well as proper termination, are required.

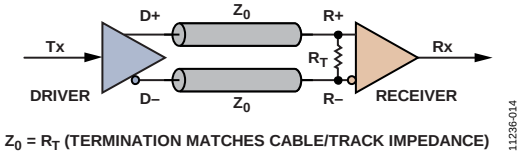

Figure 14. Point-to-Point Termination

The termination resistor should match the impedance of the communication medium; for LVDS, this is usually 100 Ω. For a simple point-to-point link, it is only necessary to terminate the end of the bus furthest from the driver, as shown in Figure 14. For multi-drop buses, the same termination can be used if the driver is at one end of the bus. Otherwise, both ends of the bus need to be terminated.

With M-LVDS, both ends of the bus are terminated, and the drivers are designed with increased drive strength, partly to accommodate the double termination (the effective load is 50 Ω rather than 100 Ω).

Some devices have built-in termination. This termination may need to be disabled if the device is located at the wrong point on the bus for termination, or if there is already proper termination on the bus. If there are two or more 100 Ω resistors for LVDS, or more than two for M-LVDS, then the bus is overterminated. This results in reduced signal amplitude and increased reflections, combining to decrease noise immunity, degrade timing accuracy and reducing the maximum transmission distance.

CONTROLLED IMPEDANCES

One difficulty in LVDS and M-LVDS links is providing a consistent controlled impedance across the bus. For links across a single PCB, impedance discontinuities can easily arise from vias, mismatches in trace lengths between each signal in a differential pair, and changes in the spacing between tracks, or the size of tracks.

For differential signaling on a PCB, the two signal traces are usually placed close together and tightly coupled. This means that the signals have a common field, cancelling emissions and reducing susceptibility to common-mode noise. One difficulty that arises is that if the traces need to move apart, for example, to reach a connector, then a change in impedance between the signals is introduced. It can be preferable to relax how closely the signals are coupled, but maintain consistent spacing and track thickness across the entire link.

Sharp turns or a series of bends in the PCB traces can also affect the signal quality. Generally, turns in the PCB traces should be minimized and kept to 45-degree angles (ideally with curves rather than sharp angles).

Skew can be introduced between the two signals in a differential pair if one signal follows a longer trace than the other does. It may not always be possible to have traces exactly the same length, but PCB layout should attempt to keep the trace lengths matched.

Connectors should be chosen to minimize any difference in impedance that they present on a bus, and cables or backplanes should also match the impedance of PCB traces where possible. Backplane connections can add significant capacitance to the bus and it may be necessary to reduce the data rate or PCB trace distances to allow for any degradation of the data signal that occurs.

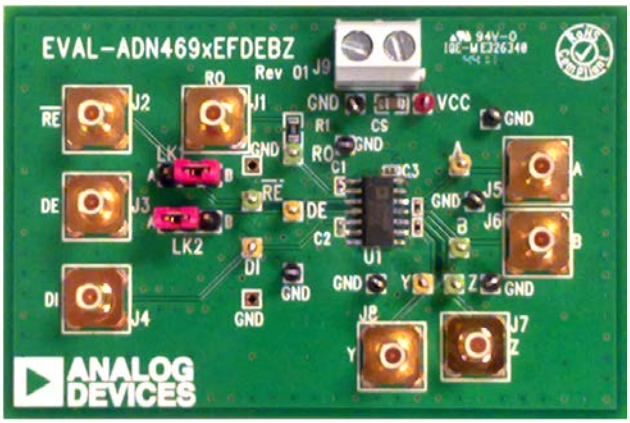

Figure 15. EVAL-ADN469xEFDEBZ Customer Evaluation Board

An example high speed PCB layout for M-LVDS is shown in Figure 15, the EVAL-ADN469xEFDEBZ evaluation board for full-duplex ADN469xE family M-LVDS transceivers. Track lengths on A, B, Y, and Z are matched and have a 50 Ω impedance created using a 4-layer board layout. The termination resistor placement is next to the device pins. The circuit does not fully correspond to an application layout because there are additional components, such as test points and jumper options.

JITTER, SKEW, DATA ENCODING, AND SYNCHRONIZATION

With high speed differential signaling, such as LVDS and M-LVDS, accurate timing is critical to the performance of a system. PCB traces, connectors, and cabling can degrade the performance of data and clock signals, requiring that a margin for error is also present in system timing. This means that careful timing analysis may be required to achieve the maximum throughput on an LVDS or M-LVDS communication link. Modern FPGAs and processors also have built-in capabilities to correct for timing errors, although there may be clearly defined limits to the amount of jitter tolerated, for example.

WHAT IS JITTER?

Jitter refers to the apparent movement of a signal edge with respect to the ideal time position of that signal edge. If a periodic signal is observed on an oscilloscope, the edges literally jitter back and forth with respect to the reference point.

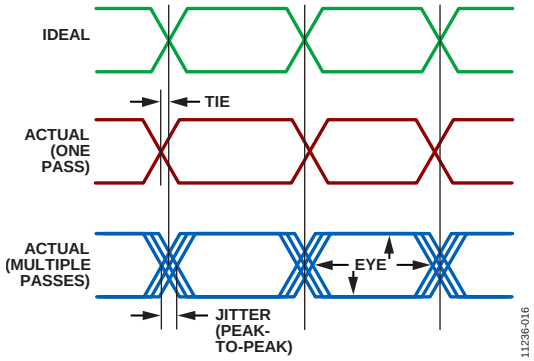

Figure 16. Waveforms Showing Time Interval Error, Jitter and Eye

Jitter can be quantified simply as time interval error, the time difference between when a signal edge occurs, and when it should occur. Usually in order to determine the sources of jitter, a large number of TIE samples are recorded to build a histogram, from which deterministic jitter can be separated from random jitter. Total jitter can be quantified as a peak-to-peak value when bounded to a specific quantity of samples. The peak-to-peak value means the time difference between the earliest and latest edge observed during sampling.

Peak-to-peak jitter can be seen visually if multiple waveform samples are overlaid on an oscilloscope display (infinite persistence), as shown in Figure 16. The width of the overlaid transitions is the peak-to-peak jitter, with the clear area in-between referred to as the eye. This eye is the area available for sampling by a receiver.

Random jitter occurs due to noise, both electrical and thermal. The result is a Gaussian distribution to the time error, with this error introduced as random jitter. The jitter is unbounded; when more samples are recorded, the probability function continues to grow.

Deterministic jitter is, by contrast, bounded. There is a fixed amount of this jitter in the system due to specific factors, such as the board layout and driver performance. Periodic jitter is one type of deterministic jitter and refers to the time difference between each cycle compared to the ideal. Periodic jitter is also recorded as a peak-to-peak value, that is, the difference between the longest and shortest periods observed

WHAT IS SKEW?

There are different definitions for skew, several of which are typically considered in designing high speed LVDS links. The most basic definition of skew is the difference in propagation time between the two signals in a differential pair. This means that edge transitions on one signal in a pair will not match up exactly with transitions on the complementary signal (the crossover will be asymmetric).

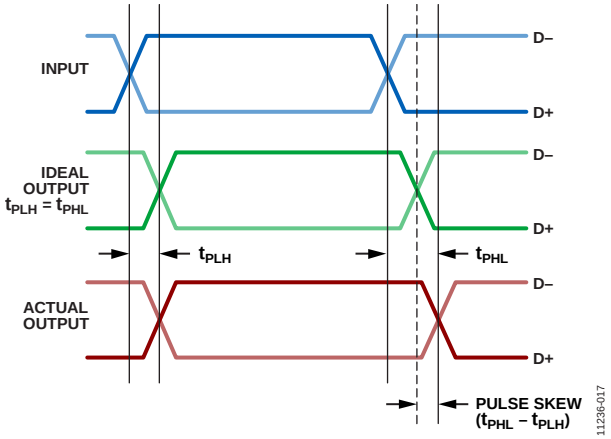

Figure 17. Waveforms Illustrating Pulse Skew Calculation

Pulse skew on a differential signal refers to the difference between the low-to-high transition time (t_{PLH}) and the high-to-low transition time (t_{PHL}). This results in duty cycle distortion, that is, the bit period is longer or shorter for a Logic 1 or Logic 0. Pulse skew is illustrated in Figure 17. The blue waveform corresponds to an input signal, the green waveform to an ideal output (where propagation times on high-to-low and low-to-high transitions are matched), and the red waveform to an actual output, where the difference between t_{PLH} and t_{PHL} results in pulse skew.

Channel-to-channel skew and part-to-part skew are some of the most important parameters in typical LVDS applications because they have multiple data channels that need to remain synchronized. Channel-to-channel skew refers to the difference, across all channels in a part, between the fastest and slowest low-to-high transition, or the fastest and slowest high-to-low transition (whichever is larger). Part-to-part skew extends this concept to channels across multiple parts.

Skew across multiple channels (on one or multiple parts) is illustrated in Figure 18. The blue waveform corresponds to an input signal, with the four red waveforms comprising output channels on one or more parts. The difference between the fastest and slowest t_{PLH} is calculated, along with the difference between the fastest and slowest t_{PHL}. The channel-to-channel or

part-to-part skew is the greater of these differences (in the case of Figure 18, the difference between the fastest and slowest t_{PHL}).

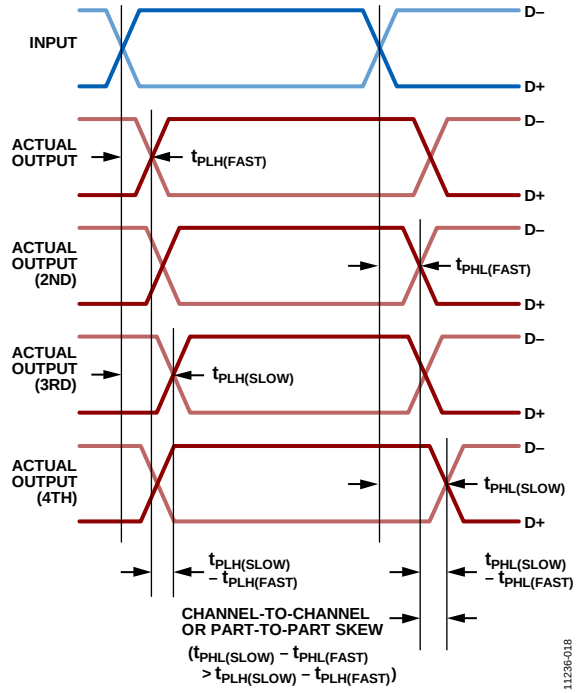

Figure 18. Waveforms Illustrating Channel-to-Channel or Part-to-Part Skew

Both channel-to-channel skew and part-to-part skew result in parallel data channels received out of phase relative to each other, even if they were synchronized at the transmitting end. This can cause difficulties in sampling across multiple channels.

DATA ENCODING AND SYNCHRONIZATION

The challenges for LVDS timing stem not only from the high speed transmission, but also from the data encoding. In many LVDS applications, in order to increase bandwidth, multiple parallel LVDS channels are used to transmit data. The transmitter must synchronize data transmitted on these channels and the receiver needs to sample each channel at the appropriate point so that data can be received at the same time across channels.

In LVDS applications using few channels, serial data is typically transmitted and at higher speeds. The high speed requires the receiving device to synchronize quickly with the incoming data stream, and, in addition to accurately sampling each bit, the receiving device needs to detect frames of data in the incoming bit stream.

To help the receiving device synchronize with the received data, a clock may be transmitted with the data channels. This is described as source-synchronous data transmission. There are several methods of transmitting the clock with the data. The clock may be transmitted as a parallel channel, with the clock period corresponding to one data bit (single data rate, SDR) or two data bits (double data rate, DDR). For serial LVDS transmission, a frame clock may also be transmitted. An example of ADC source-synchronous LVDS outputs for SDR and DDR is shown in Figure 19.

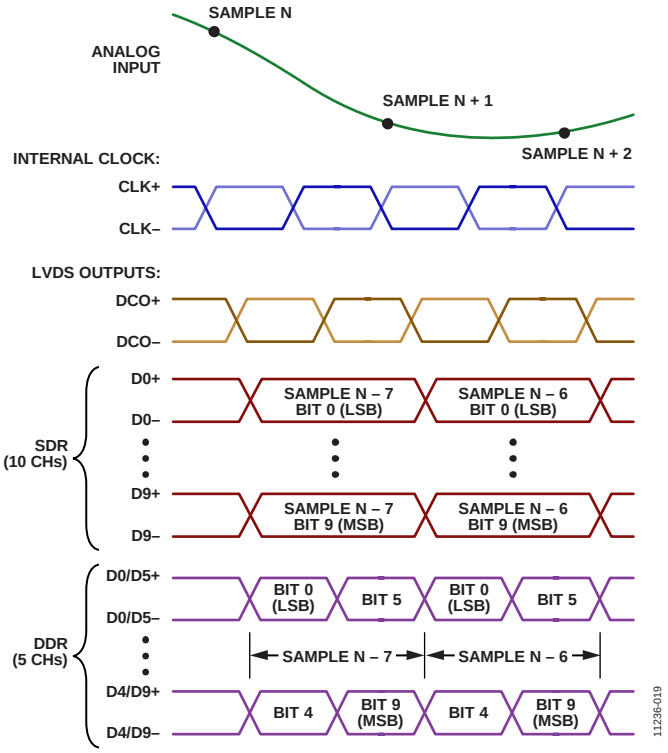

Figure 19. ADC input and Source-Synchronous LVDS Output Waveforms

An alternative to dedicated clock channels is to embed the clock with the data. With the embedded clock method, fixed bits are inserted into the data stream, allowing a receiving node to detect these bits and synchronize with the incoming data.

Channel-to-channel and part-to-part skew can be compensated for when received by modern FPGAs, using a scheme termed dynamic phase adjustment (DPA). The FPGA generates multiple phases of the received source-synchronous clock and matches each data channel to the best clock phase for sampling.

If DPA is not available, then a strict timing budget must be adhered to. There must be a time interval remaining after transmitter channel-to-channel skew and the sampling time are subtracted from the bit period. This interval is termed the receiver skew margin. The transmitter channel-to-channel skew includes the skew across channels due to the transmitting node, the skew due to the medium and the clock skew relative to the data.

ISOLATION

External interfaces can be isolated from logic circuits to prevent unwanted current flow that may damage or degrade the operation of electronic components. Galvanic isolation, shown in Figure 20, allows information flow, but prevents current flow. Complete isolation of data signals and power is possible using *i*Coupler® digital isolation and *iso*Power® power isolation.

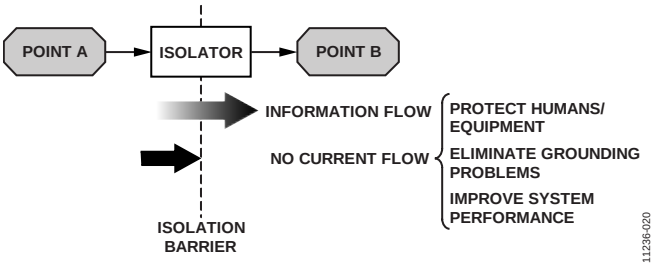

Figure 20. Galvanic Isolation Allows Information Flow While Preventing Ground Current Flow

Applications of isolation for LVDS and M-LVDS are safety isolation and/or functional isolation of board-to-board, back-plane, and PCB communication links.

An example of safety isolation is a system with an M-LVDS backplane where one or more plug-in cards are at risk from high voltage transients. Isolating the M-LVDS interface ensures that such fault conditions do not affect other circuits in the system. An example of an application where functional isolation is beneficial is measurement equipment. Isolating LVDS links, for example, between an ADC and FPGA, can provide a floating ground plane to boost the integrity of measurement data, minimizing interference from the rest of the application.

The circuit shown in Figure 21 is an isolated LVDS Interface Circuit from the Lab (CFTL), demonstrating complete isolation of an LVDS interface (see the References section). The ADuM3442 provides digital isolation of the logic inputs to the ADN4663 LVDS driver and the logic outputs from the ADN4664 LVDS receiver.

Together with provision of isolated power using the ADuM5000, a number of challenges to isolating LVDS links in industrial and instrumentation applications are met that include the following:

- Isolation of the logic signals to/from the LVDS drivers/ receivers, ensuring standard LVDS communication on the bus side of the circuit.
- Highly integrated isolation using just two additional wide-body SOIC devices, the ADuM3442 and ADuM5000, to isolate the standard LVDS devices, the ADN4663 and ADN4664.
- Low power consumption compared to traditional isolation (opto-couplers).
- Multiple channels of isolation. This circuit demonstrates quad-channel isolation (in this case, two transmit and two receive channels).
- High speed operation; the isolation can operate at up to 150 Mbps, facilitating basic LVDS speed requirements.

The circuit shown in Figure 21 isolates a dual-channel LVDS line driver and a dual-channel LVDS receiver. This allows demonstration of two complete transmit and receive paths on a single board.

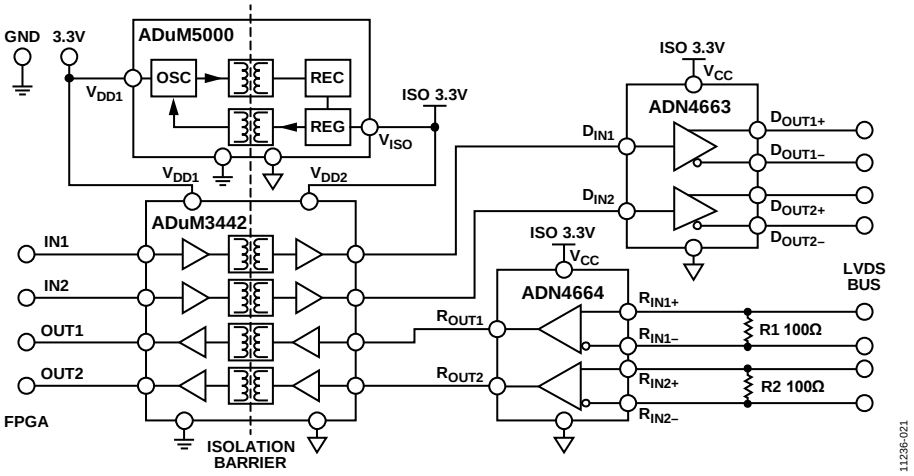

Figure 21. Isolated LVDS Interface Circuit (Simplified Schematic, All Connections Not Shown)

REFERENCES

Chen, Boaxing. 2006. "*i*Coupler® Products with isoPower™ Technology: Signal and Power Transfer Across Isolation Barrier Using Micro-Transformers," Technical Article, (Analog Devices).

IEEE Standard 1596.3-1996, "IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)".

Marais, Hein. 2009. "RS-485/RS-422 Circuit Implementation Guide," Application Note AN-960, Analog Devices, Inc.

TIA/EIA-485-A Standard, "Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems".

TIA/EIA-644 Standard, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits".

TIA/EIA-899 Standard, "Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M-LVDS) Interface Circuits for Multipoint Data Interchange".

Watterson, Conal. 2012. "Controller Area Network (CAN) Implementation Guide," Application Note AN-1123, Analog Devices, Inc.

Watterson, Conal. 2012. Circuit Note CN-0256, "Isolated LVDS Interface Circuit," (Analog Devices, Inc.

RELATED LINKS

Resource	Description
LVDS/M-LVDS web page	Links to product pages and resources for LVDS drivers, LVDS receivers and M-LVDS transceivers
M-LVDS web page	Introduction to and resources for the ADN4690E to ADN4697E family of M-LVDS transceivers
CN-0256	Circuit Note for Isolated LVDS Interface Circuit
AN-960	Application Note for RS-485/RS-422 Circuit Implementation Guide

NOTES

AN11236-0-3/13(0)